Implementation of Asymmetrical Multi-Level Inverter Configuration using Extended Hexagonal Switched Cell in MATLAB/Simulink

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Abstract: - This paper critically examines a novel extended HSC-based configuration capable of supporting both symmetrical and asymmetrical operations. The quest for optimizing classical multilevel inverter (MLI) topologies to minimize switch count has led to the emergence of various configurations known as reduced switch count (RSC) MLIs. Among these, the simplest are the T-type configurations. However, due to their limited asymmetric capability and absence of redundancies, researchers have endeavored to devise novel configurations employing the highly modular H-bridge structure. One such configuration is the hexagonal switched cell (HSC), comprising six switches interconnected in an anti-parallel manner using two unidirectional switches. Each HSC can independently function as a seven-level inverter with binary voltage ratios. Inspired by the HSC, several novel symmetrical and asymmetrical topologies have been developed to extend its capabilities to higher levels. The primary objective of this paper is to scrutinize the extended asymmetrical multilevel inverter topology based on HSC and implement it utilizing low-frequency-based PWM. To validate the operation of the proposed configuration with PWM, simulations are conducted in the Simulink environment using MATLAB.

Key-Words: - Hexagonal switched cell (HSC), Low-frequency PWM, Switching function PWM, T-type, Reduced switch count (RSC), Multilevel inverter (MLI).

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1 Introduction

The growing importance of power electronics across various applications necessitates multiple transformation stages, notably the conversion of AC to DC. Within this spectrum of transformations, inverters play a crucial role, serving essential functions across a wide power range, [1], [2]. The adoption of Multi-Level Inverters (MLIs) utilizing low-rated semiconductor devices has expanded their utility in high and medium-voltage applications. MLIs have gained popularity in electric power systems due to their promise of low Total Harmonic Distortion (THD) and their ability to operate with multiple switching combinations and frequencies. Moreover, a key advantage of multi-level inverters is their capacity to integrate renewable energy sources. In a multilevel inverter, output levels are adjusted to closely approximate a sinusoidal waveform, [3].

Increasing the number of levels in multilevel inverters enables the staircase waveform to closely approximate a sinusoidal waveform. While various topologies have been proposed to achieve more levels, circuit complexity and device cost often impose limitations, [4]. The objective of this paper is to simplify circuit design by reducing complexity and minimizing the count of switching devices. Multilevel inverters (MLIs) provide an effective means of generating output voltage tailored to meet product requirements. They are suitable for high-voltage applications without exceeding voltage limits, offering advantages such as enhanced energy quality, reduced electromagnetic interference (EMI), low switching and conduction losses, and increased voltage-blocking capability, [5].

Multilevel Inverters (MLIs) can be classified into four groups based on the number and voltage levels of DC voltage sources: asymmetrical, symmetrical, hybrid, and single DC supply MLIs, [6]. Among these, traditional multilevel converters include well-established types such as the Cascaded H-Bridge (CHB), Neutral Point Clamped (NPC), and Flying Capacitor (FC) converters. Modern multilevel converters, as discussed in recent literature, often derive from or integrate aspects of these traditional converters. These converters consist of basic units that serve as building blocks. By connecting these basic units sequentially, the

resulting converter can achieve higher output voltage levels.

Standard multilevel inverter configurations like NPC and FC utilize a single DC supply, whereas the CHB topology employs multiple isolated DC sources. The diode-clamped design relies on a single DC supply but necessitates a significant number of clamping diodes. Conversely, the flying capacitor topology replaces clamping diodes with capacitors, introducing complexity and enlarging the inverter's size, [7].

The CHB topology distinguishes itself through its integrated design, versatility, and scalability. At the core of cascaded multilevel inverters (CMLIs) lies the H-bridge, with each unit comprising four unidirectional switches. In traditional CMLI setups, the number of cascaded H-bridge units is determined by the required voltage levels. With an increase in the number of voltage steps, there arises a need for additional isolated voltage sources, controlled devices, and supplementary circuit components. This leads to heightened control complexity, larger physical size, higher device costs, and reduced reliability.

It is highly recommended to employ a single-phase seven-level series-connected Hexagonal Switched Cell (HSC), powered by photovoltaic Maximum Power Point Tracking (MPPT) and controlled by a critical controller. The synchronous reference frame is used to generate reference currents required by the shunt active filter (SHAF). The main function of the active filter is to reduce the harmonics injected by the nonlinear loads into the source. The control approach proposed for active filters converts the measured nonlinear load current into positive reference points and from these values maximum load current values can be calculated, and unit templates are extracted. For the best performance by SHAPF, the controller adopted for capacitor voltage regulation can be finetuned to achieve better performance during dynamic conditions, [8].

In [9], a Nine-Level Cascaded H-Bridge (CHB) based SHAF for harmonic compensation is proposed. SRF concept is adopted to generate reference currents which should be injected into the line to reduce harmonics produced by switching operation of nonlinear loads. Power factor improvement and reactive power compensation are the other objectives achieved by SHAF in this paper.

In [10], SHAF using a novel single-phase 9-level series-connected Hexagonal Switched Cell (HSC) is proposed. DC link is connected to the PV generation system and MPPT is adopted to regulate the voltage across the DC link while extracting maximum power, [11], in addition to the harmonics compensation, it is possible to provide active power support to the load by the proposed system in this paper.

In [12], switching pulses required by a diode-clamped multilevel inverter are generated by a non-zero triangular-based unipolar pulse width modulation. This scheme aims to reduce the number of carrier waves, simplify the modulation circuitry, and achieve stable output voltage waveforms. The non-zero triangular-based unipolar modulation scheme utilizes two triangular wave carriers devoid of zero crossings and two modulating sinewaves to generate line-to-line five-level output voltage waveforms in a single-phase full bridge diode-clamped multilevel inverter. This is a departure from conventional multicarrier sinusoidal pulse width modulation techniques, which typically employ four triangular waves and one modulating sinewave for the same type of inverter.

In [13], proposed a hybrid PWM technique aimed at reducing Total Harmonic Distortion (THD) and power losses in Voltage Source Inverters (VSI), incorporating advantages from both level-shift PWM and Phase-shift PWM. The proposed hybrid PWM technique utilizes a novel form of carrier signals. Unlike conventional PWM techniques, this hybrid approach minimizes both switching and conduction power losses. The research employs this PWM scheme specifically for an asymmetric multilevel inverter.

DC-DC converters with enhanced voltage conversion ratios play a vital role in diverse nonconventional energy applications, Including solar systems, Uninterrupted Power Supply (UPS), automotive frameworks, fuel-cell power systems, healthcare systems, and more. In this study, we strongly recommend the use of a conventional single-switch high-voltage gain boost converter topology.

The suggested converter framework presents notable benefits, including heightened efficiency, diminished conduction loss, and the capability to manage high-duty cycles. Additionally, a boost converter is employed to address tasks like increased voltage stress and complex controlling methods within the recommended system. This development leads to a significant increase in voltage gain, resulting in an environmentally friendly increased voltage conversion ratio achieved with just a single switch. The paper presents the application and methodology of the DC/DC boost converter, [14].

In [15], a method for implementing a well-balanced power distribution a transformer-based cascaded multilevel inverter is proposed. The method involves using specific unequal ratios (6:7:8:9) among the levels to achieve a balanced power flow. The approach relies on offline identification of optimal switching patterns to minimize discrepancy errors. These patterns are then stored as lookup tables in the digital device that controls the inverter. By precisely reproducing the selected switching patterns, the power flow is effectively balanced. The output voltage is controlled and regulated by taking its RMS value as feedback.

By enhancing the conventional multilevel inverters in literature several topologies with a smaller number of switches are proposed. T-type MLIs are simple asymmetric capabilities are limited. The highly modular H-bridge structure has been investigated as a source for creating advanced MLIs.

The motivation behind this research addresses the limitations of existing T-type configurations and proposes a novel extended HSC-based configuration. The objective is to adopt the highly modular H-bridge structure to initiate an asymmetrical MLI that exceeds the constraints of traditional configurations.

Objectives:

- Design an extended HSC-based MLI for symmetrical and asymmetrical operations.
- Investigate the proposed topology performance as an asymmetrical multilevel inverter.
- Simulation of the topologies using the Pulse Width Modulation (PWM) technique.

This paper explores the possibility of the hexagonal switched cell (HSC) to generate higher levels. The proposed configuration is designed to support both symmetrical and asymmetrical DC sources. Simulation of proposed configurations is performed in MATLAB/SIMULINK.

The topology presented in this work contains two parts: The first part is the level generator, to produce the stepped voltage waveform. The second part is the polarity generator, which determines the polarity of the load voltage. A number of levels increases complexity of the circuit and control strategy also increases

The paper is organized as follows: Section II introduces the asymmetrical CHB MLI, and it includes an analysis of conduction and switching losses. In Section III, the proposed CHB-MLI circuit is described, along with switching states analysis and a comparison of the operating modes of the converter. Section IV validates the model results, and ultimately, Section V concludes the proposed CHB-MLI along with the references.

2 Conventional MLI Topologies

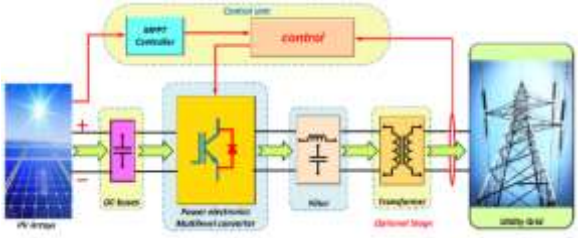

Fig. 1: Block Diagram of Multi level inverter with RES.

In modern industries, there is a significant and rapidly growing demand for high-power applications. However, certain industrial operations require lower or medium power levels. To address the voltage requirements of such applications, multi-level inverters have emerged as effective power devices. These inverters not only accommodate substantial power capacities but also provide the flexibility to integrate sustainable power sources such as solar, wind, and tidal energy. Recent research has shifted its focus towards applications involving variable AC, frequency, and speed regulations, thereby driving advancements in multi-level inverter technology. Figure 1 illustrates the renewable energy sources integrated to grid through a multilevel inverter.

With technological progress, multi-level inverters are now capable of operating at high switching frequencies, leading to reduced generation of harmonic components. As the voltage levels in these inverters increase, the output waveforms gradually approach sinusoidal shapes with lower harmonic content. The classification of multi-level inverters is based on their voltage output levels and switching configurations.

a) Diode clamped MLI
b) Flying capacitors MLI
c) CHB MLI

2.1 Diode Clamped Multilevel Inverter

The fundamental concept behind this inverter is to utilize diodes to create multiple voltage levels across various stages by employing series-connected capacitor banks. Diodes serve as voltage carriers, alleviating the load on other electrical components. However, a significant drawback of the diode-clamped inverter is that the maximum achievable resultant voltage is capped at half of the supplied DC voltage. To overcome this limitation, increasing

the number of switches, diodes, and capacitors is an option. Nevertheless, the balancing of capacitors presents a challenge, restricting these inverters to three levels. Despite this limitation, they offer high efficiency by employing a fundamental frequency for all switching patterns and provide a straightforward approach for power transfer in systems.

The 5-level and 9-level diode-clamped inverters utilize diodes as clamping devices connected to a common DC bus. The DC voltage is divided into multiple levels through switch pairs and capacitors. These inverters are commonly used in high-power motors with medium-speed drives, static VAR compensators, and for interfacing high-power DC and AC lines. However, their operation becomes complex due to the presence of numerous clamping diodes when generating multiple levels. The number of required diodes increases quadratically with the number of voltage levels. One of the main drawbacks of this topology is that in the event of a fault, the system cannot be reconfigured, resulting in a complete network shutdown, and reducing the reliability of the topology.

2.2 Flying Capacitor Type MLI

This type of multilevel inverter (MLI) resembles the diode-clamped type, but with a notable difference: capacitors are used instead of diodes, and they require recharging. The theoretical advantage of this topology is its ability to generate numerous voltage levels closer to a sine wave. However, practical implementations often limit these MLIs to generating only six voltage levels due to various constraints. In this configuration of MLI, capacitors on the DC side are arranged in a ladder-like structure, where the voltage across each capacitor differs from that across the adjacent capacitor. The magnitude of the voltage levels in the resulting waveform is influenced by the voltage difference between two adjacent capacitor legs. However, implementing numerous capacitors can be both expensive and complex compared to diode clamping, which is commonly used in MLI designs.
The advantages of flying capacitor MLIs over diode-clamped MLIs are:

- This type of MLI needs a smaller quantity of switches for the same output levels in contrast to diode-clamped MLI.
- The inverter can ride through brief-term blackouts and profound voltage sags because of a number of inverters being used in its design.
- The control of power flow is easier.
- To balance the voltage levels of the capacitors, Phase redundancies can be adopted.

2.3 CHB-MLI

The cascaded H-bridge MLI is the most widely adopted and straightforward design of multi-level inverters, applicable in both single-phase and three-phase transformation scenarios.

This design involves structuring the circuit into H-bridge cells, where each cell consists of four switches and four diodes connected. Each cell generates three outputs: positive voltage, negative voltage, and zero. In this type of MLI, multiple modules are cascaded in series to combine the voltages of different levels, resulting in a resultant voltage with various levels closer to a sine wave. This capability in waveform generation helps to reduce Total Harmonic Distortion (THD), offering an advantage over other inverters. Cascaded H-bridge MLIs have found numerous applications in industrial and domestic utility areas and are increasingly used in renewable energy sources, VAR compensation techniques, voltage regulation, and filtering applications in power stabilization processes.

The CHB inverter is particularly suitable for applications requiring higher power due to its capability to synthesize improved waveforms with reduced harmonic content compared to diode-clamped and flying capacitor models. Additionally, it eliminates the necessity for bulky transformers in conventional converter topologies, as well as clamping diodes in diode-clamped converters and flying capacitors in the FLC model. This simplification streamlines the construction and output generation of the MLI. A comprehensive comparison of MLIs under various aspects is presented in Table 1. The output voltage levels generated, in contrast to previous MLIs, are twice that of the DC sources. The individual utilization of DC sources ensures isolation between each module.

Table 1. Comparison of the regular MLI topologies with n level

S. No	Characteristics	CHB-MLI	FC-MLI	DC-MLI
1	Primary Diodes	2(n-1)	2(n-1)	2(n-1)
2	Clamping Diodes	0	(n-1) (n-2)	0
3	Main Capacitor	(n-1)/2	(n-1)	(n-1)
4	Equalizing Capacitor	0	0	(n-1) (n-2)/2
6	Constant Source	Separate DC source	No separate DC source	No separate DC source
7	Construction	Simple	Complex	Complex
8	Flexibility	Flexible	Not flexible	Not flexible

Moreover, by incorporating modular voltages to produce the resultant voltage, the stress experienced on the legs and modules is notably diminished compared to the flying capacitor model. The cascaded H-bridge MLI presents several advantages over diode-clamped and flying capacitor models, rendering it a more flexible and readily adaptable structure for various applications.

3 Extended Topologies

The fundamental unit of the HSC topologies, known as the basic HSC, is illustrated in Figure 2. This configuration is formed by an anti-parallel connection of two half-legs (H1-H6 & H3-H4) through a pair of unidirectional switches (H2 and H5). It's important to note that when ES equals ER, the basic HSC unit can function as a simple five-level inverter, with voltage magnitudes of ±ES/ER and ±(ES+ER). However, when ES equals 2ER, this HSC module operates as a seven-level inverter. Furthermore, the device voltage rating of H1 & H6 is ES; H3 & H4 is ER; and H2, H5 is ES+ER.

3.1 HSC Structure of the Considered Topology

The HSC module depicted in Figure 2 is reconfigured in Figure 3, where H1, H4, and ES are replaced by S1, S2, and V2, respectively; and H3, H4, and ER are replaced by S5, S6, and V1, respectively, while H2 and H5 are replaced by S3 and S4. The different possible switching combinations of the module depicted in Figure 3 are illustrated in Table 2.

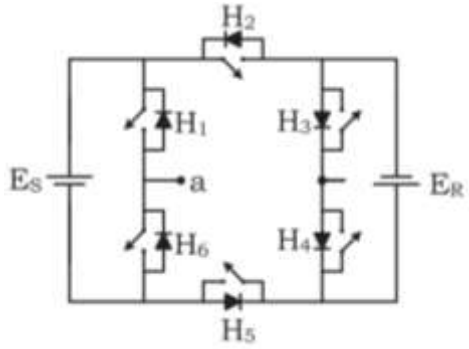

Fig. 2: Primary unit of the HSC topologies

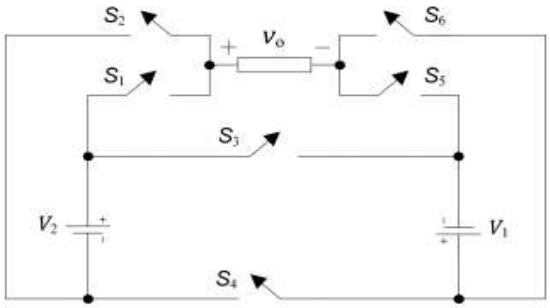

Fig. 3: Basic HSC module

Table 2. Switching Operation of Figure 2

Mode	S1	S2	S3	S4	S5	S6	Vo
1	0	0	1	1	1	0	0
	0	1	0	1	0	1	
2	1	0	0	0	1	1	V1- V2
3	0	1	1	1	0	0	V2
4	1	0	1	0	1	0	V1
5	1	1	1	0	0	0	V1+ V2

The unique configuration of the devices is analyzed concerning the output voltage in the proposed Multilevel Inverter (MLI) connection, where 1 and 0 respectively denote the ON and OFF states of the switching devices. The switching operation clearly illustrates the capability of the basic module to generate multiple voltage levels with different switching combinations. It should be noted that the polarity of the levels in Table 2 is depicted concerning one polarity, but it can be reversed as well. By utilizing appropriate combinations (trinary voltages), the MLI can function as a 9-level inverter, although this requires support from suitable PWM techniques. To simplify the analysis, a straightforward low-frequency PWM followed by a lookup table can be employed to achieve the required output voltages. Furthermore, the potential for Figure 3 to scale to higher levels by incorporating additional DC sources is demonstrated next.

3.2 HSC Structure

An essential consideration in the design of MLI topology is the total line-to-line voltage. The extended HSC, illustrated in Figure 3 for multiple levels, is depicted in Figure 4, Figure 5 and Figure 6. For the primary unit of Topology-I, the maximum voltage stress during each switch operation is presented as follows: Assuming V1: V2: V3 = 1:2:3.

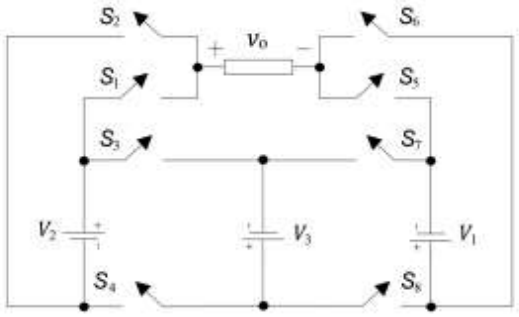

Fig. 4: Extended HSC: Topology-I

For the primary unit of Topology-I, the maximum voltage stress during each switch operation is presented as follows: Assuming V1: V2: V3 = 1:2:3.

$$V_{S1} = V_{S2} = 2V_{dc} \quad (1)$$

$$V_{S5} = V_{S6} = V_{dc} \quad (2)$$

$$V_{S3} = V_{S4} = V_3 + V_2 = 3V_{dc} + 2V_{dc} = 5V_{dc} \quad (3)$$

$$V_{S7} = V_{S8} = V_1 + V_3 = V_{dc} + 3V_{dc} = 4V_{dc} \quad (4)$$

where V_s is the voltage stress on the respective switch s. Following the incorporation of additional DC sources, Topology-I, as depicted in Figure 3, is presented as Topology-II in Figure 4. This extension augments the ladder or intermediate stages between the outer wings of the basic HSC module. Moreover, the extension or scaling of Topology-II for a generalized level is illustrated in Figure 5. To simplify real-time execution, it is imperative to minimize the number of switches required to generate all desired voltage levels at the output. This research introduces an innovative MLI topology centred around a basic unit that integrates a reduced number of power electronic switches and DC voltage sources. The approach involves extending this basic unit by incorporating additional switches and DC voltage sources. The aim is to reduce the overall number of power switches and associated driver circuits while simultaneously increasing the number of levels in the output voltage waveform.

This innovative topology is introduced as a generalized MLI. It undergoes a comparative analysis against various established multilevel inverter configurations to determine its superiority. Subsequently, the overall performance of the proposed topology in generating all voltage levels is validated through experimental results using a 15-level inverter setup. These experiments confirm the effectiveness and feasibility of the proposed topology in achieving the targeted voltage levels, demonstrating reduced complexity and improved performance.

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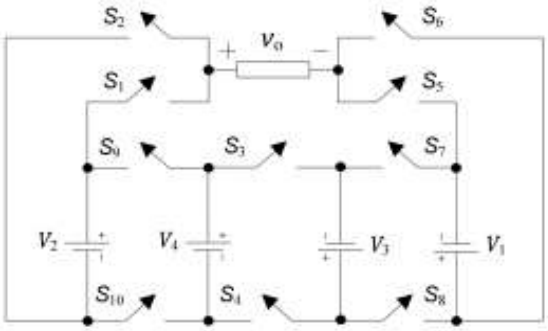


Fig. 5: Novel Extended HSC: Topology-II

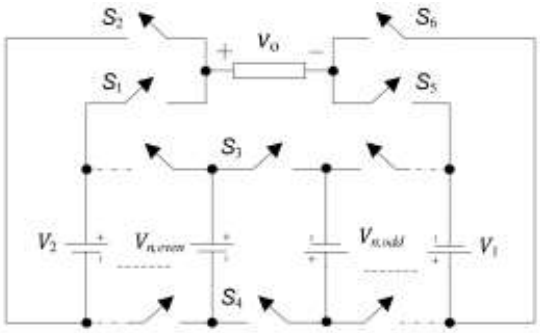


Fig. 6: Extended HSC: Scaling Topology-II for higher levels

4 Simulink Implementation

In symmetrical multilevel inverter configurations, the DC voltage resources within the H-bridges share identical values.

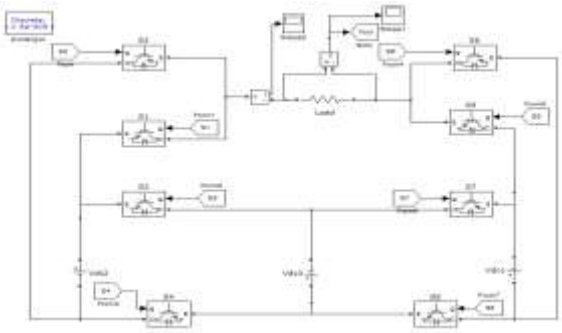


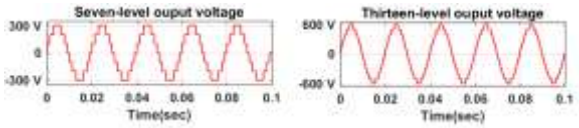
Fig. 7: Simulation model of Topology-I

Table 3. Simulation Parameters

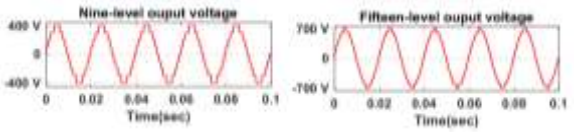
DC voltage (V_{dc})	100 V
Modulation index (m_a)	0.95
Carrier Switching frequency (F_{sw})	100 Hz; 2000 Hz
Sampling time (T_s)	1 µS

Conversely, asymmetrical multilevel inverters feature DC voltage resources with differing values. The considered HSC serves as an asymmetrical Reduced Switch Count Multilevel Inverter (RSC-MLI), capable of producing a higher number of output levels with significantly fewer switches. Two methods are employed to determine the values of the DC voltage sources in the CHB asymmetrical multilevel inverter: binary and trinary configurations. The trinary configuration surpasses the binary configuration in generating a greater number of levels. The primary factors influencing the cost and size of the multilevel inverter are simple control techniques, a reduced number of semiconductor switches, a lower count of DC voltage resources, and simplified driver circuits, [16], [17], [18].

The simulation circuit for the considered RSC-MLI topology, as depicted in Figure 3, is illustrated in Figure 6. The basic module of the Hexagonal Switched Cell (HSC), shown in Figure 2, generates a 5- level output with symmetrical voltage ratios and can produce 7 and 9-level outputs with asymmetrical voltage ratios. Conversely, the extended HSC topology-I in Figure 3 can yield a 7-level output with symmetrical voltage ratios and can generate 11 and 15-level outputs with asymmetrical voltage ratios. Similarly, Figure 4 employs four DC sources with 10 switches and can synthesize a 9-level output voltage with symmetrical voltage ratios, and up to 31-level outputs with asymmetrical voltage ratios. However, it's important to highlight that an increase in the number of asymmetrical DC voltages leads to a corresponding increase in stress on the device voltage. Table 3 presents the simulation parameters involved in the study, while Table 4 provides a summarized view of the Total Harmonic Distortion (THD) performance of Topology-I and Topology-II.



(a) Output voltage of Topology-I for symmetrical and asymmetrical



(b) Output voltage of Topology-II for symmetrical and asymmetrical

Fig. 8: Out voltage wave forms of Topology-I and II for symmetrical and asymmetrical voltage ratios, for low frequency PWM

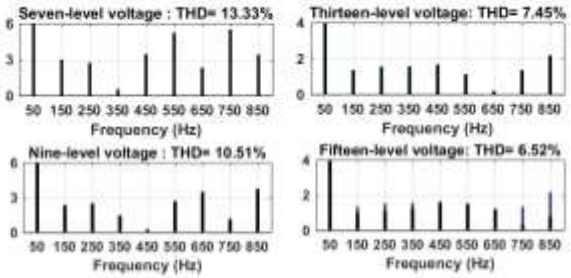


Fig. 9: Output voltage harmonic performance of Topology-I and II for symmetrical and asymmetrical voltage ratios, for low frequency PWM

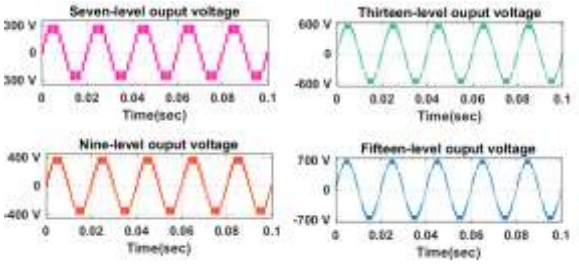


Fig. 10: Output voltage wave forms of Topology-I and II for symmetrical and asymmetrical voltage ratios, for carrier frequency PWM

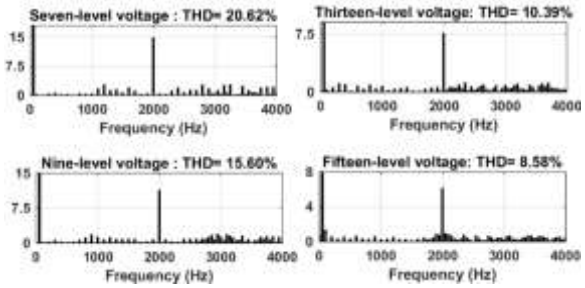


Fig. 11: Output voltage harmonic performance of Topology-I and II for symmetrical and asymmetrical voltage ratios, for carrier frequency PWM

In Figure 3, the configuration with symmetrical and asymmetrical voltage ratios of 1:2:3 can generate 7-level and 13-level output voltages, as depicted in Figure 7(a) and Figure 7(b) respectively. Similarly, when operating Figure 4 with symmetrical and asymmetrical voltage ratios of (1:2:3:1), it generates 9-level and 15-level output voltages, as shown in Figure 7(c) and Figure 7(d). The corresponding harmonic spectra of Figure 7(a) and Figure 7(b) are also demonstrated. Figure 7(b) is displayed in Figure 8. Moreover, selecting an increased carrier frequency of 2000 Hz reveals the achieved output voltages in Figure 9(a) and Figure 9(b) respectively. The corresponding FFT analysis of the output voltages in Figure 9 is depicted in Figure 10(a) and Figure 10(b). FFT analysis of seven, nine thirteen and fifteen level voltage waveforms presented in Figure 10 are shown in Figure 11. Increase in number of levels increases the fundamental quantity in waveform and hence reduces the THD.

Table 4. Output voltage harmonic performance comparison of Topology-1 and Topology-II

	Phase Voltage THD			
			Carrier frequency	
	Level	Nature	50Hz	2000 Hz
Topology-I	7-level	Symm	13.33%	20.62%
Topology-I	13-level	Asymm	7.45%	10.39%
Topology-II	9-level	Symm	10.51%	15.60%
Topology-II	15-level	Asymm	6.52%	8.58%

4.1 Results and Discussion

The results presented in Table 4 confirm an improvement in harmonic performance with the use of a low-frequency carrier. However, it is important to recognize that increasing the carrier frequency helps suppress low-order harmonics by shifting them to higher frequencies. Consequently, all carriers surrounding the fundamental frequency undergo this shift, leading to a higher cutoff frequency and consequently reducing the size of the required filters.

The results indicate that the blocked voltage values are either acceptable or zero, with the absence of negative voltage. This observation reinforces the necessity for unidirectional switches in the recommended topology. The specific details of the switching operation are outlined in Table 2. For a more comprehensive demonstration of the inverter's performance, Figure 7, Figure 8, Figure 9 and Figure 10 visually represent the output voltage. Assessing the output power quality involves quantifying the THD levels for both voltage and current. The Fast Fourier Transform (FFT) tool in MATLAB is utilized for the thorough analysis and execution of this assessment.

The results of output voltage in Figure 7, Figure 8, Figure 9 and Figure 10 provide actual insight into the inverter's operational behavior. Overall, the results discussion aims to provide a comprehensive understanding of the implications and performance metrics associated with the proposed inverter topology.

5 Conclusion

This study, proposed a novel asymmetrical multilevel inverter topology with a reduced number of switches. Through simulation by MATLAB/SIMULINK, compared the proposed inverter with conventional MLI configurations. Our findings highlight a substantial decrease in the number of components, including DC sources, IGBTs, and associated drive circuitry. The proposed inverter achieves an acceptable ratio of voltage levels by a reduced number of IGBTs, compared to other multilevel inverters reported in the literature. The proposed inverter exhibits significant advantages such as less voltage stress and reduced switching losses when compared with conventional multilevel converters. The utilization of DC sources in every primary unit significantly contributes to the topological advantages of our proposed inverter. The proposed novel asymmetrical multilevel inverter achieves enhanced power quality and increased efficiency with reduced components. Comparative analyses highlight its superiority in terms of the number of switches, diodes, and resources needed for generating different voltage levels compared to existing topologies. Considering these promising outcomes, our proposed asymmetrical multilevel inverter represents a substantial advancement in multilevel inverter technology, emphasizing efficiency and component reduction.

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