Enabling of CMOS Circuit using Dual Material Gate Germanium Pocket Induced FDSOI MOSFET

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Abstract: - This research presents a comparison of the electrical performance of a double-side induced germanium-pocket (IGP) FD-SOI MOSFET and a dual material gate IGPFDSOI (DIGPFDSOI). The electrical performance is reviewed by comparing the device parameters like drain current, band diagram, lateral electric field, surface potential, and work function of the gate material. The proposed structure exhibits excellent characteristics compared to the IGPFDSOI MOSFET. The proposed structure has a greater I_{on}/I_{off} ratio, a lower subthreshold slope, reduced capacitance, and an elevated cut-off frequency. The implementation of a dual metal gate is considered a superior method in comparison to FD-SOI technology because it effectively reduces the negative effects of scaling. A study is being done to analyze the differences in the work functions of metal gates to evaluate the effectiveness of the proposed construction. The comparison evaluation shows that the suggested design can be used for both digital and analog tasks because it has a higher switching frequency and a better cut-off frequency. Apart from this, the proposed structure can also be implemented without making substantial changes to the conventional FD-SOI MOSFET fabrication process flow. Here, we are using n-type and p-type DIGPFDSOI MOSFETs to make a CMOS converter circuit. Sentaurus TCAD is used to simulate and analyze the performance of the proposed structure.

Key-Words: - Dual Material gate, Transconductance, FDSOI, CMOS, Inverter, Work function and Cutoff frequency.

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1 Introduction

The MOS technology, predominantly dependent on silicon, is continuously advancing, facilitating the sustained growth trajectory of the electronic, information technology (IT), internet of Things (IOT), and communications industries. The sustained expansion has been enabled through the reduction of component dimensions on a microchip and the minimization of component count while maintaining the same degree of electrical capability. As technology advances, the cost of gadgets consistently drops, which promotes economic growth. The present contemporary MOS (CMOS) technology is making a substantial contribution to the expansion of the market due to its remarkable electrical performance. These components have become the fundamental elements of modern integrated circuits because they can be adjusted in both the analog and digital domains, possess characteristics such as high switching, high conductance, high transconductance, low static and dynamic power consumption, have a simple design, and can be efficiently produced. Presently, MOS-integrated circuits possess a wide array of applications, encompassing portable electronic gadgets and equipment, for example, mobile phones, wearable biomedical devices, and high-speed communication systems like 5G technology, [1], [2], [3], [4]. Apart from these, these are also used as tunable active inductors for high-frequency applications, [5]. As CMOS devices reduce in size, various scaling factors must be minimized. The mentioned factors include the subthreshold slope for effective switching, drain and gate-induced barrier lowering, threshold voltage roll-off, minimal off-state leakage current, and minimal parasitic capacitances and resistances for maximum electrical performance, [6], [7]. Conventional downsizing MOSFETs are anticipated to face certain limitations, such as a decrease in the supply voltage, an increase in I_{off} (off-state current), and a fall in the I_{on}/I_{off} ratio and many more short-channel-effects (SCEs), [8]. To tackle these problems, certain scholars have suggested inventive device configurations employing diverse forms of multiple-gate MOSFETs, such as FinFETs, dual gate MOSFETs, gate-all-around FETs, tunnel FET SOI FETs, junction-less FETs, and other analogous

structures, [9], [10], [11]. The FDSOI MOSFET is a potential choice because it follows Moore's law and the customary structure of classic CMOS technology, as discussed above. Furthermore, it has significant benefits like as minimal energy usage, immunity to radiation, and adaptability for circuit design purposes like memory storage. The reduction in size of the conventional FD-SOI MOS resulted in the emergence of short-channel effects (SCE). To reduce the effect of SCE, the structure in consideration must have a carefully crafted design. Scientists consistently propose innovative concepts for designing technologies to overcome these challenges. To resolve these challenges, scientists came up with a unique configuration for the FDSOI MOSFET. This configuration modifies the source and drain regions by creating pockets within the FDSOI MOSFET, [12], [13]. In addition to this, the dual material gate (DMG) MOSFET is gaining significant attention in VLSI research. This is because as CMOS scaling reaches its limit due to gate oxide tunneling, the DMG MOSFET offers the advantage of being scalable to the minimal channel length achievable for a specific gate oxide thickness. This advantage we observed due to the proposed device offering better immunity from short channel effects (SCE), [14], [15], [16], [17]. As we know, as the miniaturization of MOSFET goes on, the effect of SCE is increasing, so we have to consider the effect of more parameters in the simulation process. The simulation time associated with it also increases because of the increase in parameters. So, if we want to follow Moore's law and have a development pace, the time for the simulation process and its reliability must improve. To achieve this, researchers are using modern machine learning approaches, which show sufficient improvement in this process, [18], [19], [20]. This work presents a novel design in the FDSOI technology as compared to the available literature. It efficiently reduces the current while the device is in the off state and improves the slope at sub-threshold levels. This enhancement is accomplished by using germanium in the source and drain pockets, together with a dual metal gate, instead of employing a typical fully depleted SOI (FD-SOI) structure. This leads to a reduction in the tunneling current that passes from the substrate to the body level. The analysis employs various electrical parameters, including current-voltage characteristics, electron and hole mobility, electric field towards the channel, potential at the channel, and the energy band diagram in terms of valance band and conduction band. The main objective of this study is to provide evidence that the suggested design has superior electrical performance as compared to the available literature on FD-SOI MOSFET. The suggested construction was subjected to simulation and study using the TCAD device simulator.

2 Device Structure, Simulation Parameter and Methodology

The cross-sectional view of a conventional FD-SOI MOSFET is shown in Figure 1(a) [3]. In this structure, we introduce a pocket of germanium material in the drain and source side with length P_L and width P_w, it creates a double side-induced germanium pocket FD-SOI MOSFET (IGPFDSOI), as shown in Figure 1(b). These pockets help to reduce the high field at the source and drain sides. This enables the uniform distribution of electric fields across the channel. If we introduce dual material gate, i.e., gate material 1(M1) and gate material 2 (M2) in IGPFDSOI, as shown in Figure 1(c), we get our desired structure, i.e., dual material gate IGPFDSOI (DIGPFDSOI). The work functions of the two metal gates, M1 and M2, are denoted as φ_{M1} and φ_{M2}, respectively. The lateral amalgamation of these two metals results in concurrent enhancements in transconductance and suppression of SCEs, attributed to a surface-potential profile step when compared to a single-gate IGPFDSOI. M1, the material chosen near the source, has a greater work function, while M2, the material chosen near the drain, has a lower work function. As a result, the threshold voltage will follow a similar pattern, [21]. This design lowers the highest electric field near the drain end, raises the voltage at the drain end, and makes the transconductance better, [22].

Table 1 displays the physical characteristics of the normal FD-SOI MOSFET, IGPFDSOI MOSFET, and DIGPFDSOI MOSFET, together with their respective doping concentrations. The design specifications align with both the standard road map and the industry standards 22 nm technology node. The gate oxide has a thickness of 0.9 nm. Proper design of the device is necessary as the electrical performance is determined by the thickness and length of the channel. To enhance performance, we have utilized a channel length of 22 nm and a thickness of 7 nm, which is almost one-fourth of the channel length. The thickness of the buried oxide layer is 10 nm. Studies indicate that the elongated channel region in the drain enhances the efficiency of the device [23]. Considering this, we have an extended Ge channel on both sides. The dimensions of these Ge pockets have been tuned to enhance performance, with a length of 6 nm and a

height of 5 nm. The sizes of M1 and M2 of the DIGPFDSOI MOSFET are taken as equal, i.e., 11 nm. The work function of M2 (φ_{M2}) is fixed at 4.3, and we are varying the work function of M1 (φ_{M1}) from 4.3 to 5.1.

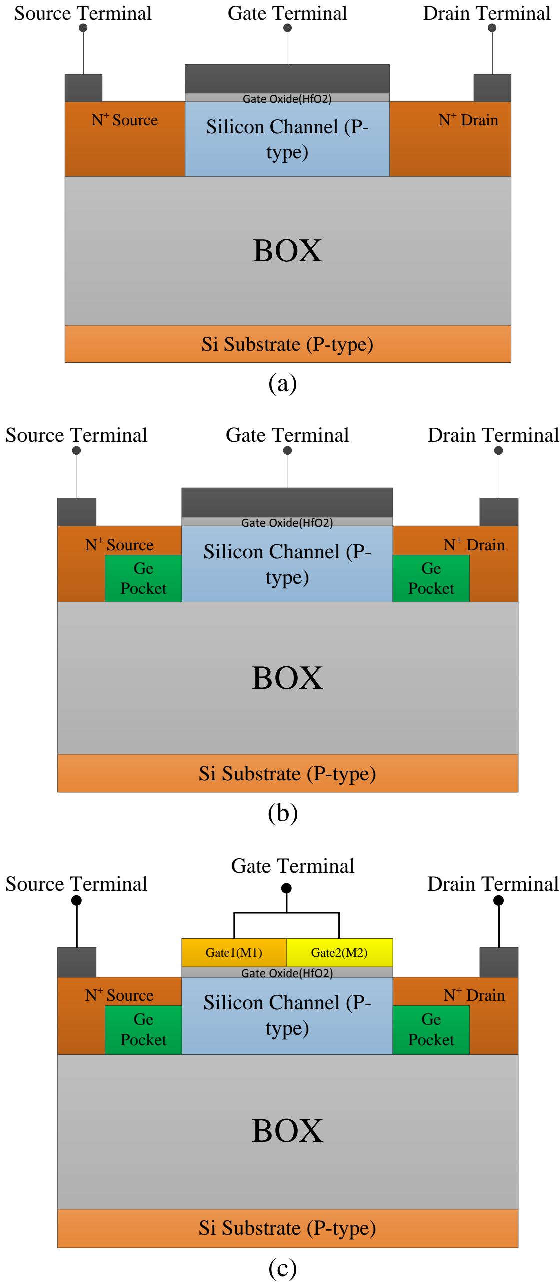

Fig. 1: (a) conventional FD-SOI MOSFET (b) double side-induced germanium pocket FD-SOI MOSFET (IGPFDSOI) (c) dual metal gate IGPFDSOI MOSFET (DIGPFDSOI)

Table 1. Parameters and its value of conventional MOSFET, IGPFDSOI MOSFET, and DIGPFDSOI MOSFET

Device parameters	**Value**		
	Conventional FD-SOI MOSFET [3]	IGPFDSOI MOSFET	DIGPFDSOI MOSFET
Source/ Drain Length	11nm	11nm	11nm
Channel thickness	7nm	7nm	7nm
Doping concentration of Source/ Drain	5×10^{20}	5×10^{20}	5×10^{20}
Pocket Length	-	6nm	6nm
Pocket width	-	5nm	5nm
Doping concentration of Source/ Drain side Pockets	-	5×10^{20} (optimized)	5×10^{20} (optimized)
Channel length	22nm	22nm	22nm
Gate length	22nm	22nm	M1= 11nm M2= 11nm
Doping concentration of Channel Region	1×10^{16}	1×10^{16}	1×10^{16}
Thickness of gate oxide	0.9nm	0.9nm	0.9nm
Thickness of BOX	10nm	0.9nm	0.9nm
Gate work function	4.7 eV	4.7eV (optimized)	φ_{M1}= 4.3 to 5.1 φ_{M2}=4.3
Doping concentration of Substrate Region	1×10^{17}	1×10^{17}	1×10^{17}

The suggested structure's simulation results were generated using Sentaurus TCAD. The fabrication approach of the suggested structure follows the typical SOI structure, with the addition of stages to integrate pockets near the source and drain sides. The proposed structure is simulated using models named BTBT, Shockley Reed-Hall, and drift-diffusion. For the proposed configuration, the thickness of the silicon layer was set to 7 nm, thus accounting for the quantum tunneling phenomenon in the simulation. The structures in question were constructed using a gate oxide thickness of 0.9 nm. Both field-dependent models and concentration-dependent models have been incorporated into the equation to accurately

characterize mobility. The Auger recombination model is being studied due to the need to assess high current densities, [24], [25]. The dynamic non-tunneling model is employed to compute the adverse slope of the valance band from the source to the drain and within the channel, as well as the gradients of the conduction band. We have employed iterative numerical techniques to solve the devices under various biasing situations.

3 Results and Discussion

In this section, we contrast and compare the features of traditional FDSOI with the characteristics of IGPFDSOI and the characteristics of IGPFDSOI with DIGPFDSOI.

Figure 2 depicts the input transfer characteristic curves of standard FDSOI and IGPFDSOI. From this, we can see that the off-state current for IGPFDSOI MOSFET is lower than for conventional FDSOI MOSFET for constant V_{ds} = 1 V and variable V_{gs} from 0 V to 1 V. The on-current of both structures is virtually equal and in the 10^{-2} A/µm region. The off-state current for traditional FDSOI is in the 10^{-9} A/µm range, while it is in the 10^{-11} A/µm region for IGPFDSOI. Based on the data presented above, we can conclude that the I_{on} to I_{off} ratio is greater in IGPFDSOI. In switching applications, the I_{on} to I_{off} ratio (I_{on}/I_{off}) is an essential metric. These enhancements are due to the induced pockets, which aid in reducing the powerful electric field near the source and drain sides. This contributes to a uniform distribution of electric fields across the channel.

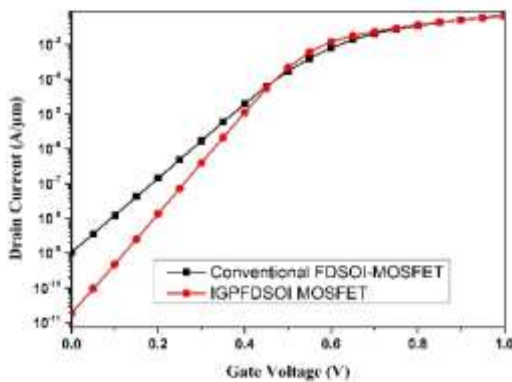

Fig. 2: I_D-V_{GS} characteristics of Conventional FD-SOI MOSFET, [3] and IGPFDSOI MOSFET

Figure 3 examines the input characteristics of the DIGPFDSOI MOSFET about work functions. The value of φ_{M2} is 4.3 and remains constant. The value of φ_{M1} ranges from 4.3 to 5.1, increasing by increments of 0.2. The drain voltage is maintained at 1 V, while the gate voltages vary between 0 V and 1 V. The biasing is uniform across all structures. By increasing the work function of the M1 gate (φ_{M1}) from 4.3 eV to 5.1 eV, the off-state current reduces from a range of 10^{-6} A/µm to 10^{-12} A/µm, while the on-current remains unaffected. Studying the work function behavior also requires consideration of the on-state current. As the work function increases, there is a significant reduction in the electron concentration in the gate channel region. Consequently, the on-current decreases when the work function is increased.

Relative switching power (RSP), which is used to compare the switching power of the proposed structure under examination, is defined as [26].

$$RSP=\frac{\left(I_{on}/I_{off}\right)_{DIGPFDSOI}}{\left(I_{on}/I_{off}\right)_{IGPFDSOI}} \quad (1)$$

Because the value of RSP that was calculated using equation (1) is much higher than one, it can be deduced that the structure that was presented possesses outstanding electrical performance and is thus ideal for low-power digital applications.

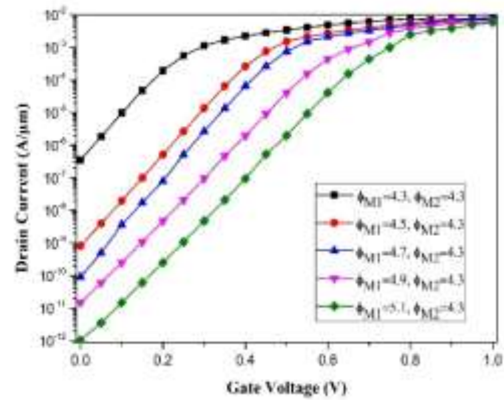

Fig. 3: I_D-V_{GS} characteristics of DIGPFDSOI MOSFET for different gate work functions (φ_{M2}=4.3, φ_{M1}= 4.3 to 5.1)

The electric-field distribution of both devices as a function of their lateral positions is depicted in Figure 4. As can be observed, the peak electric field in the DIGPFDSOI MOSFET is substantially smaller than in the IGPFDSOI MOSFET. As indicated in the picture, the simulated longitudinal electric field distribution of DIGPFDSOI MOSFET exhibits two peaks compared to a single peak in IGPFDSOI MOSFET. The benefit of material work function differences is that the threshold voltage near the source can be more positive than the threshold voltage at the drain. This holds true for n-channel FETs and the inverse for p-channel FETs. The electric field diminishes at the depletion areas (P-N junctions) on both the source and drain sides

due to impact ionization. This is where the majority of the recombination occurs. The suggested model has a longer depletion length than previous models. The proposed model's peak electric field drops due to the high number of recombinations.

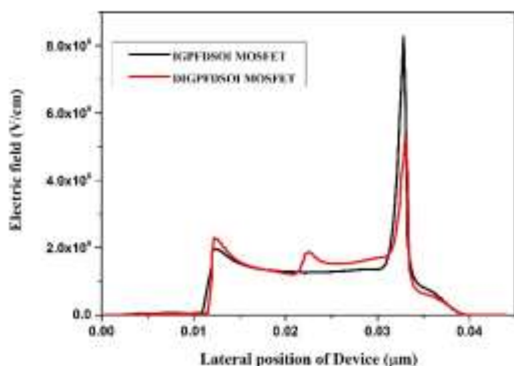

Fig. 4: Lateral Electric Field along with channel of IGPFDSOI MOSFET and DIGPFDSOI MOSFET

In Figure 5, we can see the electron velocity on lateral sides of both devices discussed above. As we see the electron velocity in the source side of DIGPFDSOI MOSFET is higher than the electron velocity in the source side of IGPFDSOI MOSFET. The reason for this is that the material with a higher work function is located closer to the source, while the material with a lower work function is located closer to the drain. As a result, the threshold voltage near the source of the transistor is higher than at the drain (in the case of an n-channel FET, the converse is true for a p-channel FET). This voltage difference creates a stronger electric field, which accelerates the movement of charge carriers in the channel more quickly.

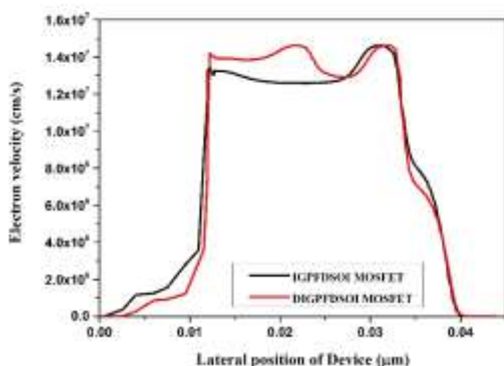

Fig. 5: Electron velocity along with channel of IGPFDSOI MOSFET and DIGPFDSOI MOSFET

Figure 6 depicts the surface potential graph for both configurations. The graph demonstrates that the surface potential of the DIGPFDSOI MOSFET exceeds that of the IGPFDSOI MOSFET. The work function at the source side is higher as compared to the work function at the drain side. This means that the threshold voltage close to the source is higher compared to that at the drain, resulting in higher potential.

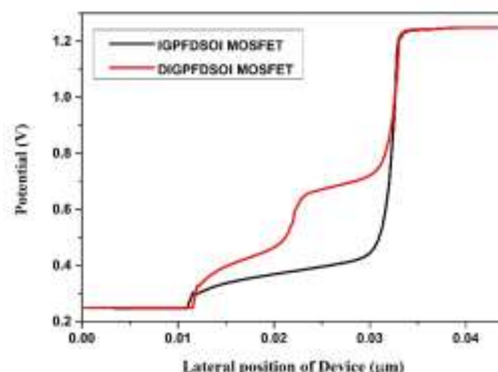

Fig. 6: Potential along with channel of IGPFDSOI MOSFET and DIGPFDSOI MOSFET

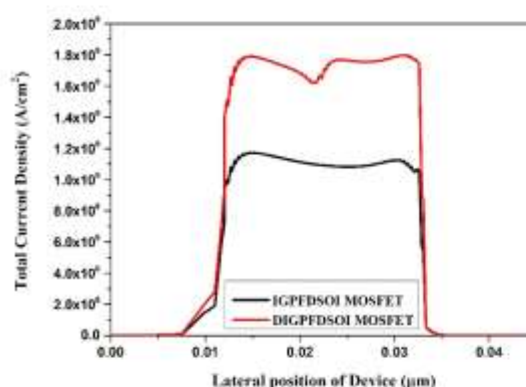

Fig. 7: Total Current Density along with channel of IGPFDSOI MOSFET and DIGPFDSOI MOSFET

For the switching process to work more efficiently, the current density needs to be higher. Figure 7 depicts the current density along with the channel of both devices. The plot shows that the average current density in the DIGPFDSOI MOSFET is higher. This happens because current density is proportional to an electric field, and induced pockets and dual material help to lower the intense electric field near the source and drain sides while increasing the field in the channel region.

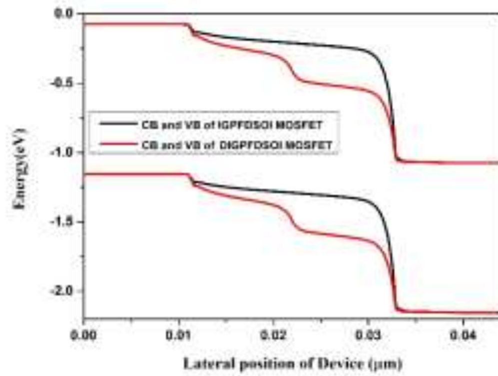

Fig. 8: Energy band diagram (EBD) along with channel of IGPFDSOI MOSFET and DIGPFDSOI MOSFET

Both the IGPFDSOI MOSFET and the DIGPFDSOI MOSFET have their energy band diagrams displayed in Figure 8. It is possible to deduce from the figure that the DIGPFDSOI MOSFET has a smaller band energy in comparison to the IGPFDSOI MOSFET.

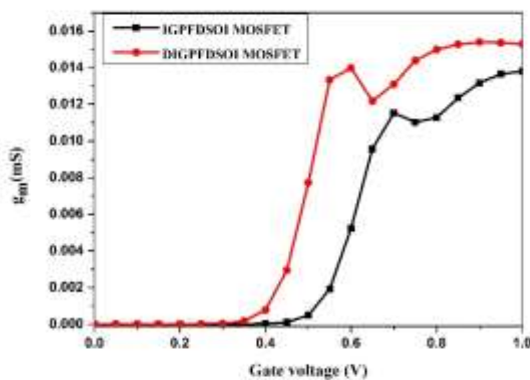

Fig. 9: Transconductance at different gate voltage for IGPFDSOI MOSFET and DIGPFDSOI MOSFET

Figure 9 shows the investigation of transconductance for different gate voltages for both the IGPFDSOI MOSFET and the DIGPFDSOI MOSFET. The transconductance of DIGPFDSOI MOSFET is 1.5×10^{-2} S/m, which is higher than that of IGPFDSOI MOSFET. Transconductance is a key factor in determining circuit switching speed, as we all know. The higher the transconductance, the better the switching speed. Here we can see that the value of g_m is higher in DIGPFDSOI MOSFET. The value of g_m in DIGPFDSOI MOSFET is nearly 1.2 times higher than in IGPFDSOI MOSFET, so we get better switching speed.

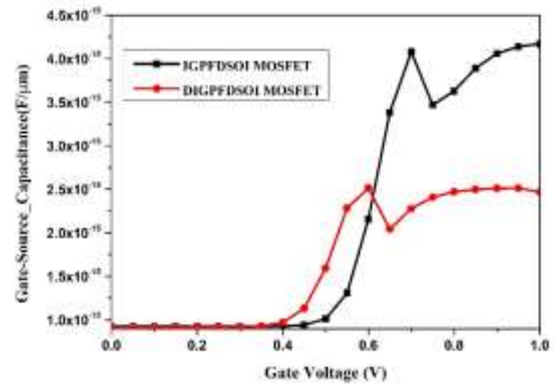

Fig. 10: Gate-Source Capacitance at different gate voltage for IGPFDSOI MOSFET and DIGPFDSOI MOSFET

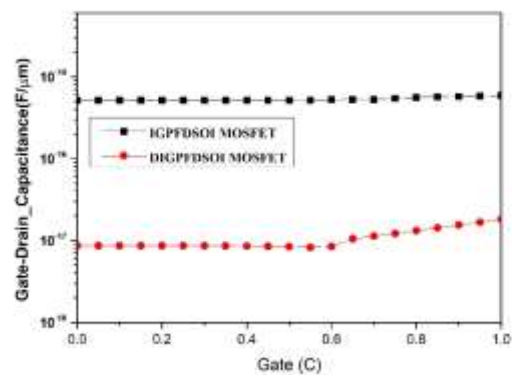

Fig. 11: Gate-Drain Capacitance at different gate voltage for IGPFDSOI MOSFET and DIGPFDSOI MOSFET

The gate-to-source and gate to drain capacitance for both architectures are depicted in Figure 10 and Figure 11, respectively, for a variety of gate voltages ranging from 0 to 1V. Upon closer inspection, we can observe that the capacitances of the DIGPFDSOI MOSFET in both instances are smaller than the capacitances of the IGPFDSOI MOSFET. Because of this, the performance of the device is improved.

To gain a greater understanding of the device speed, it is required to first understand the transit/cut-off frequency (f_T). We performed an ac analysis of the proposed structure and applied a 100 MHz tiny signal at the gate to the source terminals. Cut-off frequency (f_T) is a function of g_m, gate to source capacitance which is denoted by C_{gs}, and gate to drain capacitance which is denoted by C_{gd}, as shown in equation 2.

$$f_T = \frac{g_m}{2\pi(C_{gd}+C_{gs})} \quad (2)$$

From Figure 9, we can get the value of transconductance of IGPFDSOI MOSFET and DIGPFDSOI MOSFET and the value of effective capacitances (sum off C_{gs} and C_{gd}) of IGPFDSOI MOSFET and DIGPFDSOI MOSFET can be extracted from Figure 10 and Figure 11. After getting these two values and using equation 2, we can easily get the value of the cut-off frequency.

Figure 12 demonstrates the cut-off frequencies of IGPFDSOI MOSFET and DIGPFDSOI MOSFET. From the figure, we can infer that the cut-off frequency of the DIGPFDSOI MOSFET is better as compared to the IGPFDSOI MOSFET because capacitances in DIGPFDSOI MOSFET are less than the IGPFDSOI MOSFET.

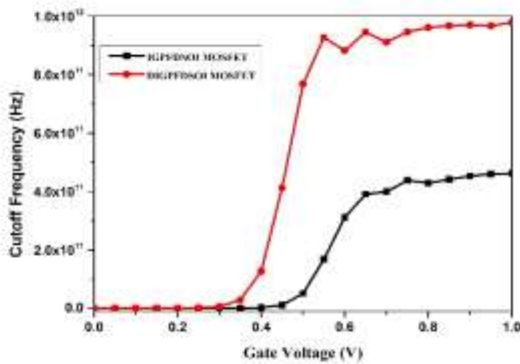

Fig. 12: Cut-off frequency at different gate voltage for IGPFDSOI MOSFET and DIGPFDSOI MOSFET

Figure 12 shows the cut-off frequencies of IGPFDSOI MOSFET and DIGPFDSOI MOSFET. From the figure, we can infer that the cut-off frequency of the DIGPFDSOI MOSFET is better as compared to the IGPFDSOI MOSFET because capacitances are less than the IGPFDSOI MOSFET.

4 CMOS Inverter Circuit

Further, we have designed a CMOS inverter circuit from the proposed DIGPFDSOI MOSFET. For it, we are using n-type and p-type DIGPFDSOI MOSFETs. The data in Table 1 served as inspiration for the device structure sizes. The p-type DIGPFDSOI MOSFET has a dimension that is 2.5 times larger than the n-type DIGPFDSOI MOSFET to offset the reduced mobility of holes. In p-type DIGPFDSOI, we take a dual material gate in a manner where the threshold voltage close to the source is less positive compared to that close to the drain (opposite to n-type). This structure has a work function of 4.3 and 4.7. This CMOS inverter is simulated using Sentaurus TCAD in mixed-mode simulation.

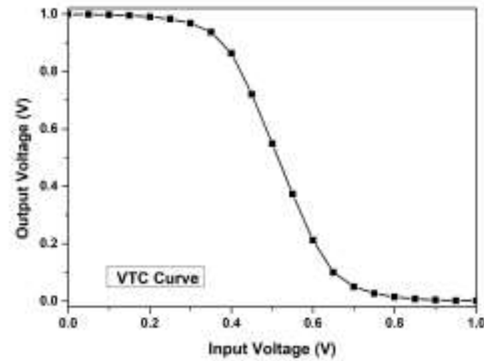

Fig. 13: VTC curve of CMOS inverter using DIGPFDSOI MOSFETs

The dc analysis of the suggested CMOS inverter circuit made with DIGPFDSOI MOSFETs is displayed in Figure 13. From the figure, we can infer that the threshold voltage of the proposed CMOS inverter circuit is nearly 0.47 volts, this is nearly fifty percent of the supply voltage, i.e., 1 volt. This CMOS inverter circuit can be further investigated through ML-based models, which will be necessary to keep pace with the development process and follow Moore's law.

5 Conclusion

The benefits of incorporating germanium pockets and a dual-material gate into standard FD-SOI FETs were highlighted in this work. The paper's results reveal that the DIGPFDSOI MOSFET has significantly higher switching and cutoff frequencies than standard FDSOI and IGPFDSOI MOSFETs. The DIGPFDSOI MOSFET's input characteristic displays an off-state current in the range of 10^{-12}A and an on-state current in the range of 10^{-2}A at work functions φ_{M2}=4.3 and φ_{M1}=5.1, and the RSP of the device is more than 1, indicating that the proposed device is well suited for digital applications. Frequency analysis is also performed on IGPFDSOI and DIGPFDSOI MOSFETs with work functions φ_{M2}=4.3 and φ_{M1}=4.7. The analysis shows that the capacitance of the DIGPFDSOI is smaller than that of the IGPFDSOI MOSFET, and so the cut-off frequency of the DIGPFDSOI is also less. As a result, pockets with dual material gates in FDSOI MOSFETs are well suited to replace traditional FDSOI MOSFETs in integrated circuits. The introduction of pockets and dual material gates in FDSOI MOSFETs has further enhanced the I_{on} to I_{off} ratio (0.556×10^{10}), total capacitances (C_{gs}= 2.47×10^{-15}F, C_{gd}=8.63×10^{-18}F), and

transconductance gm (1.58×10^{-2} S/m). Furthermore, the results demonstrate that in terms of switching and other metrics, DIGPFDSOI MOSFET surpasses IGPFDSOI MOSFET. Because of this, the structure that has been presented is suitable for use in gadgets that involve high-frequency switching. A CMOS inverter circuit made with DIGPFDSOI MOSFETs provides a threshold voltage of 0.47 volts, this is nearly fifty percent of the voltage of the 1-volt supply voltage.

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