Analysis and Design of MBCFET and Their Circuit Application in Current Mirror and DRAM

TEJAS KUMAR, ABHAY PRATAP SINGH, VIMAL KUMAR MISHRA
Electronics and Communication Engineering,
Jaypee Institute of Information Technology, Noida,
INDIA

Abstract: - This research paper addresses the challenges associated with transistor downscaling, particularly short channel effects (SCEs) in conventional silicon metal-oxide-semiconductor field-effect transistors (Si MOSFETs), and introduces Multi-Bridge-Channel MOSFETs (MBCFETs) as a potential solution. This study explores their attributes, emphasizing flexibility and faster switching, and comprehensively examines device parameters, fabrication processes, and simulation frameworks, offering a detailed analysis of critical factors influencing MBCFET performance. Investigating the intricate relationship between nanosheet dimensions and device characteristics, the research provides insights for optimized design and integration into future semiconductor technologies. The research looks at how the gate electrode's work function, the nanosheets' thickness and count, and the different types of doping affect important device properties such as transconductance, drive current, OFF-state current, and threshold voltage. Furthermore, the study is being carried out to form a current mirror and DRAM circuit by using the proposed MBCFET. This study demonstrates the transformative potential of MBCFETs in high-performance electronic applications.

Key-Words: - Multi-Bridge-Channel MOSFETs, Gate All Around, Nano Sheet, DIBL, Current Mirror, DRAM.

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1 Introduction

In the era of electronic industry, there is a demand to increase the computational power and effectiveness of integrated circuits. In this regard the size of the transistors is being downscaled aggressively. This reduction in the size of transistors serves to increase the number of transistors on a single chip, which in turn allows for more dense and complex designs on the same substrate area, advancing the integrated circuit. But as the device size reaches the nano level, the add-on short channel effects (SCEs) have been causing complications in the way of achieving better performance of the device, [1]. The conventional silicon MOSFETs with nanoscale channel lengths face many challenges, such as increasing OFF-state current (I_{off}) and rising subthreshold leakage current due to strongly influenced channel potential by the drain potential, [2], [3]. To overcome these issues the novel MOS device structures have been investigated by the researchers, [4], [5]. As technology got better, FinFET became a possible way to get around the issues associated with planar technology devices. But FinFETs have a lot of problems, like fabrication complexity, high costs to scale up, process limits, hard to make steep fins for current control, and problems with handling process variation, [6]. To mitigate this the Multi-bridge-channel MOSFETs (MBCFETs) have become an outstanding example of technological advancement when compared with other non-planer devices, [7]. They can break through the current scaling hurdles and lead the industry into a new era. The MBCFETs could be useful in a wide range of new applications, from low-power (LP) switching without comprises with performance. Due to this, the MBCFET is widely used in artificial intelligence (AI) and 5G technology, [8]. Moreover, it can easily demonstrate the largest drive current, superior area efficiency, and an extraordinary level of immunity to short-channel effects. Furthermore, the MBCFET is easily fabricated because of its compatibility with the existing FinFET technology process flow, [9]. However, the structure of the MBCFET is designed by using a vertically stacked nanosheet (NS) and a gate-all-around (GAA) structure, which provides them with superior performance and better short-channel control which shows better electrical performance as compared to the FinFETs and makes them a possible successor for future nodes, [10]. In this research paper, we study the characteristics of MBCFETs and explore the factors that influence their performance, such as the work function, the thickness of the nanosheet, the number of nanosheets, and the effect of different doping levels.

Furthermore, we study how the variance in the above factors impacts the important parameters of the device, such as threshold voltage (V_t), subthreshold swing (SS), transconductance (g_m), drive current (I_{on}), and OFF-state current (I_{off}). Moreover, the study talks about every positive aspect of MBCFETs, focusing on their versatility, fast switching, and how they might be able to solve issues that current semiconductor technologies are facing and their seamless integration into future semiconductor technologies.

2 Device Structure and Simulation Framework

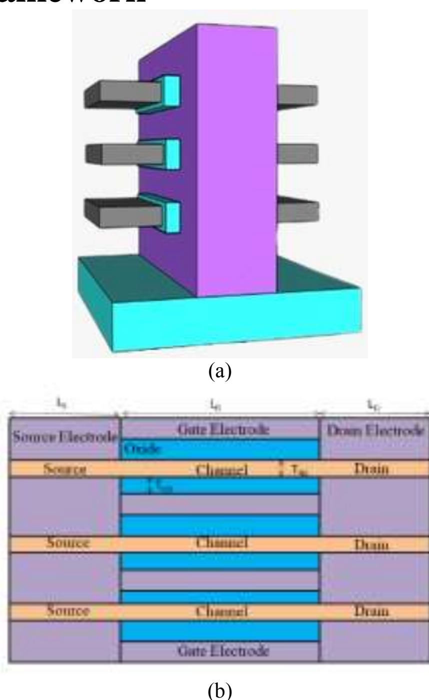


Fig. 1. (a) 3D structure of the proposed MBCFET (b) Cross-section view of the proposed MBCFET

Table 1. Overview of Device Specifications

S.no	Parameter	Value
1.	Nanosheet Thickness (T_{NS})	2 nm
2.	Gate Length (L_G)	30 nm
3.	Oxide Thickness (T_{ox})	3 nm
4.	Doping Concentration	1×10^{16} cm^{-3}
5.	Nanosheet Height (H_{NS})	2 nm
6.	Channel Width	6 nm
7.	Source/Drain Length	10 nm
8.	Channel Length (L)	30 nm

Figure 1 shows the structure of the MBCFET which consists of 3 fins in between the source and drain. The fin basically helps to flow the current from the source region to the drain region. In continuation, the different process steps are involved to form the proposed device. Firstly, on top of the bulk Si substrate, or SOI substrate, the Si layers are grown, making the transistor’s base. After forming the base region silicon die oxide layers are formed. In the further process, the source-drain extension (SDE) is formed with the help of an etching process like a chemical dry etch (CDE. After the process, a selective epitaxy growth of SDE layers is done with Si, and a thick mask layer is deposited. Moving further, the gate oxide is removed, and the Si layers are exposed with the help of a partial etching process. Around the channel layer, a subsequent gate oxide and gate electrode formation process takes place, [11], [12]. The Silvaco TCAD tool is being used for the simulation of the proposed device. The device was simulated by using a finer Schrodinger-Poisson mesh equation for quantum analysis, which helps in more accurate simulation without errors made in the mode-space of drift-diffusion equations. This method also utilizes the transport Hamiltonian in Non-Equilibrium Green's Function (NEGF) equations. Moreover, the quantum solution is refined by the specification of fine mesh because the channel length of the proposed device is 30nm, hence it requires a rectangular mesh for the Schrodinger solver. Furthermore, the source and drain regions of this device have a concentration of 10^{16} cm^{-3}. Hence, heavily doped source and drain regions enable efficient charge carrier injection and extraction methods, which improves the electrical performance of the proposed device. The dimensions of the MBCFET as shown in Table 1 includes a nanosheet thickness (T_{NS}) of 2 nm, a channel length of 30 nm, a source and drain length of 10 nm each, a channel width of 6 nm, a channel height of 2 nm, an oxide thickness of 3 nm, a gate length of 30 nm, and an oxide thickness (T_{ox}) of 3 nm. The effective oxide thickness of the device improves performance by reducing leakage current from the gate terminal, which further improves the device's electrical performance in terms of switching. Figure 1(a) shows the 3D view of the MBCFET structure and Figure 1 (b) correspondingly presents a cross-sectional view of the structure. Additionally, the gate length (L_G) is firmly set at 30 nm, and the gate oxide thickness (T_{ox}) at 3 nm. The nanosheet thickness (T_{NS}) and height (H_{NS}) are both stipulated at 2 nm, while the source/drain extension length (L_{ext}) is 20 nm, evenly distributed among the source and drain regions. MBCFET emerges as a cutting-edge nanoscale device with a meticulously engineered structure, poised to revolutionize high-performance electronic applications.

3 Result and Discussion

In Figure 2, the relationship between gate bias (V_g) and drain current (I_d) is illustrated, serving as an indicator of electrostatic properties. A steeper I_d-V_g curve signifies superior electrostatic characteristics. The measured transfer characteristics, displayed in both log (left axis) and linear (right axis) scales for a drain bias (V_d) of 0.05, exhibit the behavior of three-channel configurations.

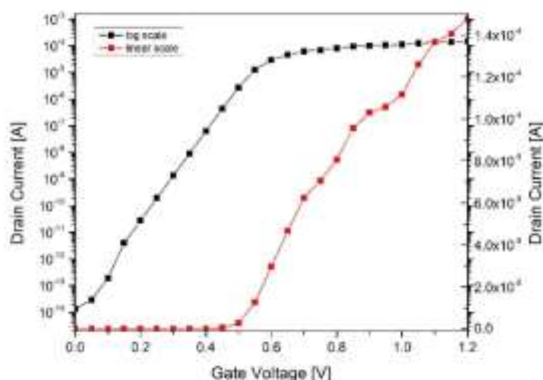
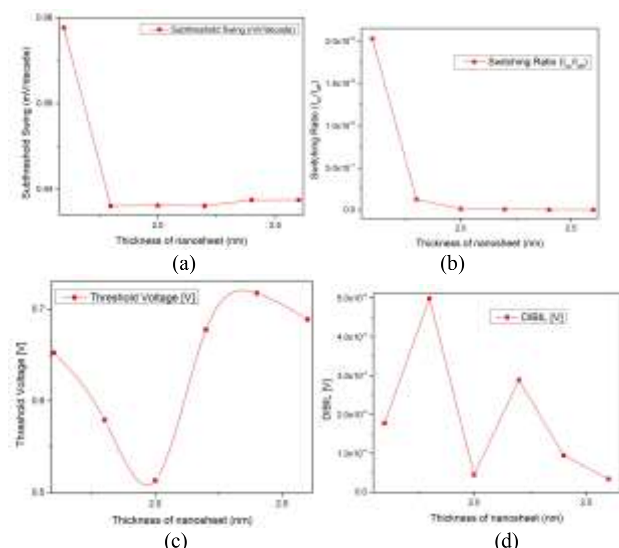


Fig. 2. I_d-V_{gs} characteristics of GAA MBCFET at V_{ds} = 50 mV

The off current (I_{off}) for the Multi-Bridged Channel Field-Effect Transistor (MBCFET) registers at approximately 10 fA at V_d = 50 mV, indicating a substantial on-off ratio (I_{on}/I_{off}) and highlighting the device's effectiveness in suppressing leakage current. The obtained subthreshold slope (SS) from Figure 2 is approximately 38 mV/dec over multiple decades of drain current (I_d), remaining consistent across varying drain voltages (V_d) showcasing the stability of the device.



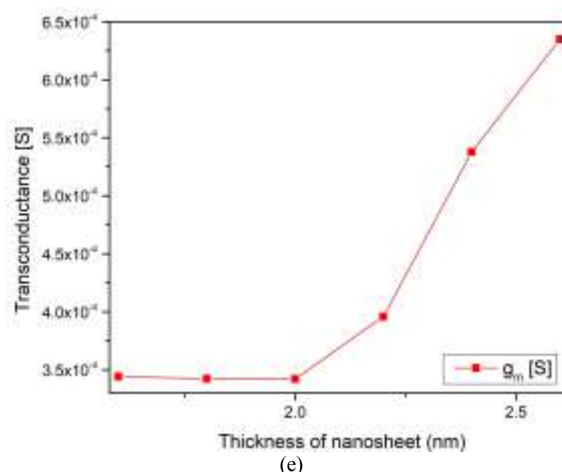


Fig. 3. Variance of (a) Subthreshold Swing(SS) (b) Switching Ratio (c) Threshold Voltage (d) DIBL & (e) Transconductance against varied thickness of nanosheet

The subthreshold swing characterizes the alteration in gate-to-source voltage needed for a tenfold shift in drain/source current. Calculated from the inverse slope of the logarithm of drain current versus gate voltage in the subthreshold range, a smaller subthreshold swing is generally preferred for a rapid transition between off current (I_{off}) and on current (I_{on}). Research indicates that a reduced subthreshold swing is associated with lower leakage current and elevated threshold voltage, substantially enhancing device performance. The primary contributors to transistor leakage comprise subthreshold leakage due to minority carrier diffusion, gate leakage arising from dielectric tunneling, and junction leakage due to reverse bias.

Figure 3(a) illustrates the relationship between subthreshold swing and nanosheet thickness, ranging from 1.6 to 2 nm. This demonstrates the intricate correlation between the size of nanosheets and the behavior of subthreshold swing. The I_{on}/I_{off} ratio is a useful measure for evaluating the overall efficiency of a device. It represents the ratio of the current at $V_{gs} = V_{dd}$ to the current at $V_{gs} = 0$. This ratio tells us that when no voltage is applied to the gate at that time, the amount of current flows through a field-effect transistor. When a voltage difference is applied between the gate and source, the current flowing from the drain to the source is referred to as I_{on}. A larger on-current (I_{on}) helps in reducing gate switching time, making the switching activity fast, but it is also important to minimize the leakage current to keep the static power loss low. It also increases the fan-out capability of the device. So, when the I_{on}/I_{off} ratio increases, it shows an improvement in the overall functioning of the device. The relation between the switching ratio and

the nanosheet thickness is shown in Figure 3(b). In a field-effect transistor (FET), the threshold voltage is a crucial parameter that shapes the performance of the device. It is the minimum gate-to-source voltage (V_{gs}) that the device requires to work as a field effect transistor. Threshold voltage can be impacted if any minor change occurs in device structure, like variance in device thickness, channel length, etc. of the device, which can change the amount of power consumption due to the leakage current. The graph is shown in Figure 3(c), i.e. the relationship between nanosheet thickness and threshold voltage. At 2nm nanosheet thickness, the device's overall performance is improved, and the lowest threshold voltage is recorded as compared to 1 and 3 nm thickness. The reason behind that is the reduction in the energy barrier is referred to as drain-induced barrier lowering (DIBL). It occurs when the drain voltage increases. This factor results in changes in many other parameters, such as a decrease in the threshold voltage which trade-off the subthreshold slope, and it also affects the device's ability to switch efficiently between the on and off states. DIBL is a very important factor for devices with short channel lengths. Figure 3(d) shows the change in DIBL (drain-induced barrier lowering) as a function of nanosheet thickness. From figure, we can inferred that the DIBL is less at 2nm and 3nm of thickness. It can be realized that there is an initial increase in DIBL with increasing thickness, followed by a drop at a thickness of 2nm. This observation shows a complex connection between the dimensions of nanosheets and DIBL. The reason behind this is that the variation in doping concentration with the thickness of the nanosheet. Furthermore, the transconductance parameters (gm) are being analysed for understanding the amplification capability of a proposed field-effect transistor (FET) which measures the transistor's responsiveness to changes in the gate voltage, which affects its capacity to amplify signals. In available FET devices, the sensitivity and amplification of the signal is determined with the help of transconductance value. Hence, we can observe from Figure 3(e) a clear pattern of how the transconductance rises with the increase in nanosheet thickness. From this observation, we can understand a potential method to enhance transconductance by adjusting the dimensions of nanosheets. This has the potential to improve FET design and overall performance.

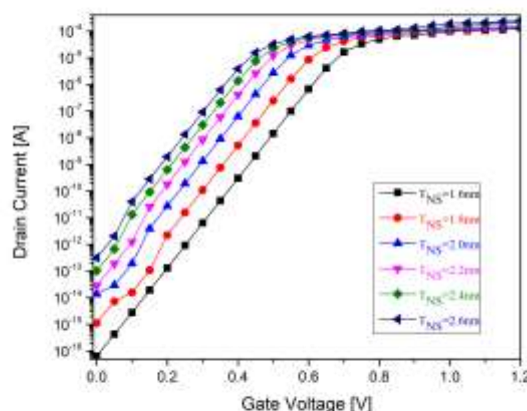


Fig. 4. I_d -V_g curve with a variance of the thickness of nanosheets

The change in the thickness of the nanosheets changes the transfer characteristics of the MBCFET, which can be observed in Figure 4. We can also note improvements in subthreshold behavior with the reduction in off-current and the decrease in the thickness of the nanosheet. Similarly, a considerable decrease in the current is observed, which shows the interplay between quantum confinement effects and charge transport dynamics caused by the nanosheet's size, [13], [14]. The impact of nanosheet thickness on both on and off currents in the MBCFET can be observed from the above relationship, from which we can understand its performance over different dimensions.

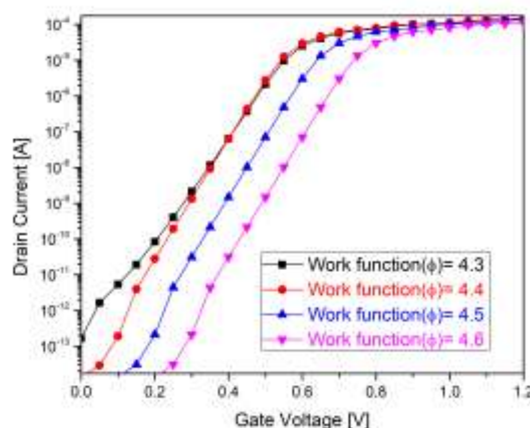


Fig. 5. Impact of work function on transfer characteristics of MBCFET

In Figure 5, we can see how the work function changes the MBCFET's transfer properties in log form. From figure, we can observe that the off current decreases as the work function increases. This is because a higher work function needs a higher gate voltage to turn on the device. Due to the

trade-off between the off-state current and threshold voltage the conductance and on-state current drops slightly. The reason behind this is that the larger work function corresponds to a greater threshold voltage. In this situation, the threshold voltage of the proposed device is 0.71V with a work function equivalent to 4.6, compared to 0.51V at a work function equivalent to 4.4. Furthermore, as the work function increases, the subthreshold swing decreases, indicating better efficiency in transitioning between on and off states. The analysis of the Multi-Bridged Channel Field-Effect Transistor (MBCFET) encompassed two distinct gate structures: the Gate-All-Around (GAA) structure and the Double Gate (DG) structure. In the GAA structure, all three nanosheets are governed by two gates—one positioned above the nanosheets and oxide layer, and the other beneath. Conversely, the DG structure employs a single gate to control two nanosheets. Transfer characteristics for both structures are illustrated in Figure 6. Notably, the DG structure exhibits a lower off-state current compared to the GAA structure, indicating enhanced leakage control. In the DG structure, on the other hand, the ON current is only slightly higher than in the GAA structure. The trade-off between on and off currents helps us understand how gate structure affects the performance of the MBCFET. It also makes it easy to design and improve the device based on the needs of the design. Current mirrors are analog circuits that copy the current present in the other circuit into its circuit. They are widely used for replicating the current flow from one transistor to another.

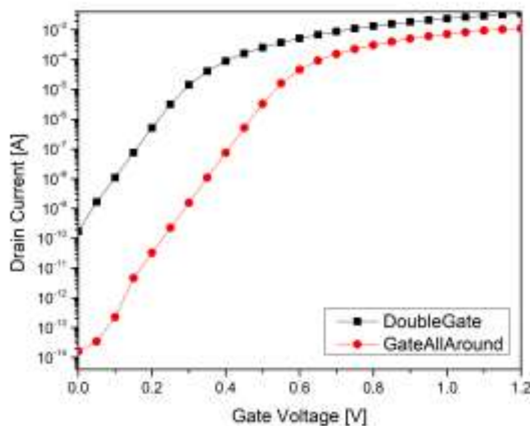


Fig. 6. Id-Vg of Double Gate(DG) and Gate all around(GAA) structures of MBCFET

The basic functionality of a current mirror is that the output of the current mirror replicates the input current. The circuit contains two transistors, one of which acts as a reference transistor, which senses the reference current, and the other, which mirrors the current. For designing the circuit a Verilog-A modules are used. It makes the circuit easier to build and do analyses by using device models. For this study, we simulated the Verilog-A code in Cadence Virtuoso. To write the Verilog-A code, we start with the header files, define the input and output ports, and then specify the values of constant and real parameters that we got through TCAD simulations. After the simulations, with the use of Verilog-A code of the proposed device MBCFET based current mirror is designed. In Figure 7, the DC analysis performed on the current mirror is shown. The current source provides a stable 20µA current as input to the current mirror. It is observed that when a DC voltage input of 576 mV is applied, the other transistor within the mirror precisely mirrors this input by maintaining an equivalent 20µA current.

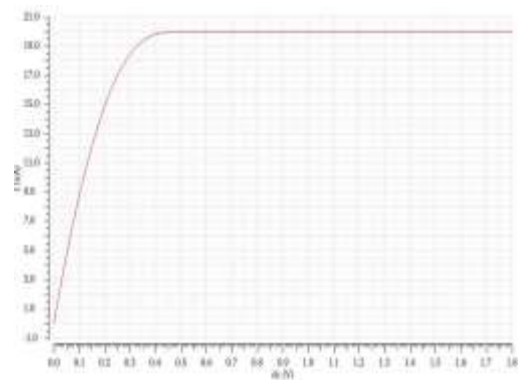


Fig. 7. DC analysis curve of current mirror simulated through Verilog A code

This finding underscores the accuracy and efficiency of the current mirror in replicating the specified current under controlled DC conditions.

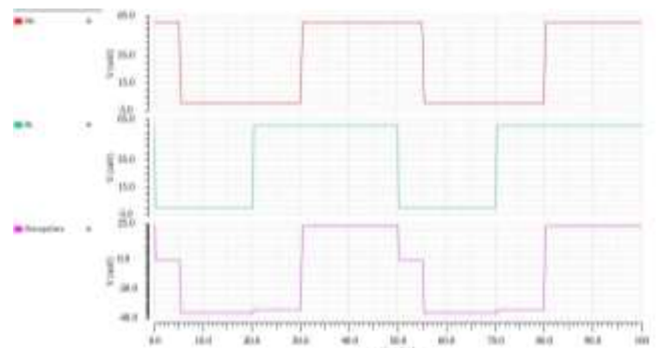


Fig. 8. Transient analysis of 1T-DRAM simulated through Verilog A code

Dynamic Random-Access Memory (DRAM) is a type of volatile memory widely used in computing systems for its high-density storage and fast access times. The bit line (BL) and word line (WL) are

crucial components leading to data storage and retrieval. BL facilitates reading and writing binary data by transferring charge to and from the memory cell's capacitor, whereas WL activates the transistor in a DRAM cell, enabling the flow of charge and controlling access to stored data during read or write operations, as illustrated in Figure 8. The 1T DRAM, relying on the unique attributes of MBCFET, exhibits unique transient characteristics during read and write cycles.

4 Conclusion

The in-depth study of MBCFET performance across a wide range of parameters, such as nanosheet thickness, gate electrode work function, and different doping effects, shows how these factors interact in complex ways. The study finds that a thickness of 2 nm might be the best way to make nanosheets work best by balancing threshold voltage, subthreshold swing, and drain-induced barrier lowering (DIBL). The fact that DIBL goes up and then down with nanosheet thickness makes the relationship more complicated and calls for more research to help improve device optimization. Furthermore, the comparison of Gate-All-Around (GAA) and Double Gate (DG) structures elucidates the nuanced trade-off between ON and OFF currents, offering valuable guidance for tailored MBCFET design. Moreover, the proposed MBCFET is used to design a current mirror and a DRAM circuit. The DC analysis of the current mirror circuit provides a stable current at different voltages. Also, the analysis of the DRAM circuit shows a stable read, write, and hold margin.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

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Conflict of Interest

The authors have no conflicts of interest to declare.

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