Impact of Discrete-Time Modeling on Dual Input Buck-SEPIC Converter

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Abstract: - This paper addresses aspects of a two-input Buck-SEPIC dc-dc converter. This integrated DC-DC converter processes power from two sources, two switches, and four different energy storage elements. The designed converter is processing 48 volts from two sources V_{g1} = 36 V and V_{g2} = 60 V. The transfer function modeling of this converter plays an important role in addressing several crucial aspects like optimal parameter design, controller design, stability, and robustness issues. Here, two types of transfer function modeling aspects are considered: continuous-time and discrete-time. The discrete-time transfer function is derived by considering trailing-edge as well as leading-edge digital pulse-width modulation scheme (DPWM) and for each of these cases time-delays in the control loop are also included. The designed converter parameters L_1, L_2, C_1, and C_2 are based on the design equations. The transfer functions are obtained in continuous-time and discrete-time for the TI-BS converter in the MATLAB environment. The experimental validation of the TI-BS dc-dc converter is performed through Hardware in Loop (HIL) using the real-time environment of the OPAL RT. For TIBS converter polezero configurations and frequency response characteristics are plotted. Using these plots important characteristics related to the deviation in phase angle of frequency response at higher frequencies due to RHP zeros are observed. The simulation studies are performed considering a 36 V / 60 V to 48 V, 500 W, prototype, DC power distribution system. The detailed modeling aspects in continuous-time as well as in discrete time are discussed considering a two-input Buck-SEPIC converter. The mathematical derivations of four different transfer function matrices using discrete-time modeling (trailing-edge and leading-edge modulation) are discussed in detail along with timing diagrams considering interval-1 and interval-2 sampling. The frequency response of the TI-BS dc-dc converter is affected when it is modeled using the discrete-time models and such frequency response deviation in phase response is observed for the TI-BS converter. The non-minimum phase response of this converter is shown using the Bode frequency response in the MATLAB environment and verified using the pole-zero map.

Key-Words: - DC-DC Converter, Two Input Buck SEPIC, Digital Pulse Width Modulation, Leading Edge DPWM, Trailing Edge DPWM, Bode Plots, Pole-Zero Maps.

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1 Introduction

The 48-volt application dc-dc converters are gradually increasing due to its feature i.e., the highest safe voltage and its applications include data centers, automobiles, and LED lighting. Modeling is essential for dc-dc converters (i) to know the principle of operation and its steady-state behavior of converter, (ii) to obtain critical characteristics through the generation of pole-zero maps, (iii) proper parameter selection to avoid instability, (iv) to extract the frequency response behavior thereby deriving the conditions for stability, (iv) to identify permissible load conditions to protect the circuit from overheating, (v) to identify suitable sources for proper power management (vi) to design robust controllers to ensure closed-loop system stability under uncertain conditions. If the true model is not known, the designed controller may be ineffective in regulating the converter output variables and the resultant dynamic performance characteristics of the closed-loop system are poor. Hence, modeling of the converter system plays an extremely important role in controller design and that can be implemented. In the following paragraph, the literature relevant to converter system modeling is discussed.

Converter mathematical modeling can be obtained in numerous ways these are (i) state-space averaging (SSA), [1] (ii) sampled-data modeling, [2] (iii) switch PWM model, and (iv) dynamic phasor

model, [3]. Though several methods to model the integrated dc-dc converters were reported in the literature to define the dynamics, the SSA model, [4], [5], [6], [7], [8], [9], [10], is popularly used. State-variable modeling aspects of multi-input converters have been discussed in, [11], [12]. An overview of mathematical modeling aspects of dc-dc converter systems is reported in, [12]. An exact discrete-time small-signal model useful for direct digital controller design for multiphase converters is proposed in, [13], [14], [15]. The comparative study of different two input converter topologies are presented in Table 1. Discrete-time small-signal analysis has been used to formulate the model for digitally controlled dc-dc converters. The dc-dc converters can be modelled in continuous as well as discrete-time. Modeling of Boost converter using discrete-time models with leading edge modulation, leads to undesirable non-minimum phase response as compared to continuous-time case. Some of the recently reported two-input integrated dc-dc converters are studied in detail and the comparison table is shown below. The TI-BS converter exhibits higher efficiency (among the listed) and is taken as reference to study in detail to study the converter frequency response behavior. The detailed modeling aspects of this converter are discussed (i) to extract frequency response behavior of the integrated converter at high frequencies and (ii) to identify critical pole-zero pairs that lead to up-down or down-up glitches that are responsible for regulation difficulties. In this paper a systematic study has been performed to address the modeling aspects as well as to extract frequency response characteristics that helps to design and identify converter parameters for 48 V dc-dc converter applications.

Detailed modeling aspects are discussed in this paper for TI-BS dc-dc converter in detail. A brief description of the design steps is enumerated as follows: (i) TI-BS converter is discussed, and presented equivalent circuit models in section 2 (ii) State-variable modeling of TI-BS dc-dc converter is discussed and also small-signal continuous-time Modeling aspects are discussed in section 3 (iv) Derivation of TFM using Small-Signal Discrete-Time Model are discussed in section 4 (v) Simulation results and experimental results are discussed in section 5.

Table 1. Comparison of different Two Input Converters

No. of Sources	*2*	*2*	*2*	*2*	*2*	*2*
No. of Switches	*4*	*4*	*3*	*2*	*4*	*2*
No. of Diodes	*0*	*4*	*1*	*1*	*3*	*2*
No. of Passive Elements	*6*	*5*	*4*	*6*	*5*	*4*
Voltage Gain	$\frac{d_1}{1-d_1}V_{g1}$	$\left(\frac{d_1}{1-d_1}\right)^2 V_{g1}$	$\frac{d_1}{1-d_1}V_{g1}$	*M*	$\frac{1+d_1}{d_2}V_{g1}$	*N*
Switching Frequency (KHz)	*100*	*20*	*50*	*50*	*100*	*50*
Efficiency	*93.2%*	*93.6%*	*93.75%*	*94%*	*96%*	*97%*
Reference Number	[15]	[16]	[17]	[18]	[19]	*Buck-SEPIC*

$$M = \frac{d_1}{(1-d_1)}V_{g1} + \frac{d_2}{(1-d_2)}V_{g2}N = d_1V_{g1} + \frac{d_2}{(1-d_2)}V_{g2}$$

Table 2. Design Equations of TI-BS Converter

	L_1	L_2	C_1	C_2
TI-BS Converter	$\frac{V_0(1-d_1)}{f_S\Delta I_{g1}}$	$\frac{(V_{g_2}-V_{C_1}-V_0)(1-d_1)}{f_S\Delta I_{g2}}$	$\frac{I_{L_2}(1-d_1)}{f_S\Delta v_{C1}}$	$\frac{I_0 d_2}{f_S\Delta v_{C0}}$

2 TI-BS DC-DC Converter

Two-Input Buck-SEPIC converter is considered for processing power from sources V_{g1} and V_{g2} where V_{g1}, is a voltage source with high magnitude (HMVS) and V_{g2}, is a voltage source with low magnitude (LMVS). During the process of power conversion, the converter functions as buck and buck-boost operations with respect to HMVS (V_{g1}), and LMVS (V_{g2}) respectively. The converter operating modes either continuous conduction mode or discontinuous conduction mode, depend on the nature of current through the inductor. Two independent duty-ratio PWM signals are needed to regulate the two switching devices of the converter. The operating principle along with important features of TI-BS converter is discussed in detail. The frequency response and time-response characteristics of this converter are discussed in the following section considering (i) continuous-time modeling (ii) discrete-time modeling. The reason for modeling of the converters in two different domains is to extract the frequency response behavior of TI-BS converter at high frequencies that may indicate non-minimum phase response behavior as observed with boost converters using discrete-time modeling.

The TI-BS Converter topology is given in Figure 1, it is observed that the converter is having two switching devices. The two switching devices of TI-BS converter are driven in either by leading edge or by trailing edge digital PWM signals with constant switching frequency of (fs=1/Ts). The discrete-time modeling aspects of these converters are discussed using trailing-edge and leading-edge modulations with on-time as well as off-time sampling. Using these two-different modeling methodologies the effects of modeling on frequency response characteristics can be extracted.

The equivalent circuit diagrams and principle of operation of TI-BS converter. The converter can be operated for $d_1 < d_2$ and $d_1 > d_2$ and for both of these cases TI-BS converter undergoes three different structural changes namely mode-1,2,3 shown in Figure 2. Using these equivalent circuits in respective modes the converter modeling is obtained in the state-space domain. The load voltage dependency on the source voltages and PWM duty-ratio signals is called as voltage gain expression. It will be established by applying volt-sec balance to the inductive elements as shown in Figure 1 and for this converter final expression for voltage gain is obtained as $V_o = V_{g1} d_1 + \left(\frac{V_{g2} d_2}{(1-d_2)}\right)$. Output voltage is a function of V_{g1}, V_{g2}, d_1, d_2, i.e. $V_o = f(V_{g1}, V_{g2}, d_1, d_2)$ and hence these factors decide the system performance. The design equations obtained from time-domain analysis for the TI-BS dc-dc converter is given in Table 2.

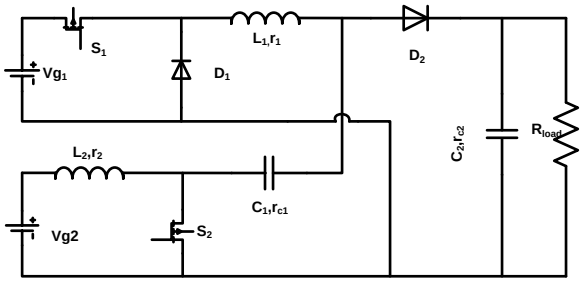


Fig. 1: TI-BS Converter Topology

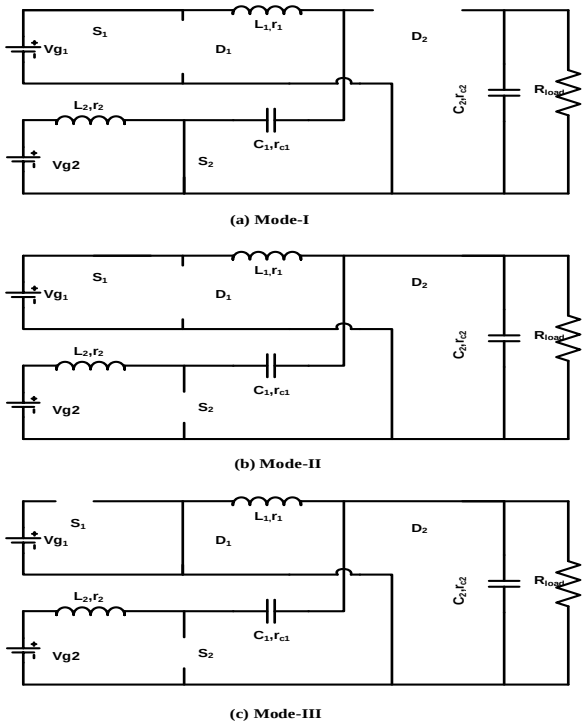


Fig. 2: Mode-I, II and III Equivalent Circuits of TI-BS converters

3 State-Space Modeling Aspects of TI-BS DC-DC Converter

In the power management of TI-BS dc-dc converter, the voltage magnitudes of V_{g1} and V_{g2} are high and low respectively. The power share between the two sources (V_{g1} and V_{g2}) with load can be assigned as (i) Designed voltage source V_{g1} is to supply higher power share and voltage source V_{g2} is supply lower power share and (ii) V_{g1} is designed to supply lower power share and supply voltage V_{g2} is designed to supply higher power share (iii) V_{g1} and V_{g2} are designed to supply higher power share and (iv) V_{g1}

and V_{g2} are designed to supply lower power share. In all these possible power supplying conditions case (i) can be called as power sharing proportional to their capacities, case(ii) is nonlinear (inverse proportion to their capacities) where the capacity of V_{g1} is under-utilized and capacity of V_{g2} is burdened, for case (iii) Vg_2 may be burdened and for case (iv) V_{g1} is under-utilized. For effective utilization of two sources and to avoid the overloading of V_{g2}, constraint on the current drawn from V_{g2} is generally imposed to avoid overload and therefore its power share should be proportional to its capacity. Here, the source current (i_{g2}) of V_{g2} needs to be monitored along with output voltage regulation (V_0). Therefore, TI-BS converter is a two-input (control inputs d_1 and d_2) two-output (V_0 and i_{g2}) converter (TITOC) system and from control point-of-view, each of the output variables depends on the controlling inputs (d_1 and d_2). Hence, the output variable's functional dependency with respect to its input variables is named as transfer function matrix (TFM) and is represented mathematically by a set of transfer functions assembled in matrix form. To derive the TFM, the state-variable model along with small-signal model is essential wherein the state-variable model describes dynamic and steady-state behavior of the converter system.

3.1 State-Variable Modeling

This TI-BS converter circuit is operated in three different modes for switch synchronization of $d_1>d_2$. In each mode of operation, the state-space equations are derived, and the resulting matrices of equation (1) are given in Table 3 and describe the dynamic behavior of the power conversion process. These state-space matrices are used in small-signal continuous-time or discrete-time modeling methodologies which are generally used to derive the transfer function matrix of this converter.

$$\dot{x} = A_k x + B_k u \tag{1}$$

$$\begin{bmatrix} v_0 \\ i_{g2} \end{bmatrix} = \begin{bmatrix} E_k \\ P_k \end{bmatrix} x \tag{2}$$

where $A_k \in R^{4\times4}, B_k \in R^{4\times2}, E_k \in R^{1\times4}, P_k \in R^{1\times4}$

$$[x] = [i_1 \quad i_2 \quad v_{C_1} \quad v_{C_2}]^T$$

$$[u] = [V_{g1} \quad V_{g2}]^T \tag{3}$$

k=1, 2, 3 for mode-1, mode-2 and mode- 3, respectively.

The transfer function matrix (TFM) is useful to analyze the dynamic behavior, used for design of direct digital controllers for TI-BS converters. The TFM of this converter is formulated using two different ways: (i) small-signal continuous-time modeling (ii) small-signal discrete-time model. In the following sections, the procedure to derive the TFM using these modeling methodologies is discussed in detail.

3.2 Small-signal Continuous-Time Modeling

The TI-BS converter is controlled and operated in a cyclic manner. It has two control input variables (d_1 and d_2), and two output variables (V_0 and i_{g2}). Here, this circuit undergoes three different structural changes which depend on operating modes and leading to three different state-variable models. The converter which undergoes cyclic operation can be conveniently modelled using state-space averaging method and it depends on conduction periods of switches. The state-space averaging model of the integrated converter is used to derive the small-signal continuous-time TFM model. The averaged value matrices are given in equation (4), when switch duty ratio control signals are operated with $d_1>d_2$. The equation (4) is substituted in equation (1) and the resultant equation is described using the equation (5) and equation (6).

$$\begin{aligned} A &= d_2A_1 + (d_1 - d_2)A_2 + (1 - d_1)A_3 \\ B &= B_1d_2 + B_2(d_1 - d_2) + B_3(1 - d_1) \\ E_0 &= E_{01}d_2 + E_{02}(d_1 - d_2) + E_{03}(1 - d_1) \\ F &= F_1d_2 + F_2(d_1 - d_2) + F_3(1 - d_1) \end{aligned} \tag{4}$$

Table 3. State-Variable Matrices of TI-BS Converter

A_1

$$\begin{bmatrix} -\frac{(r_{C_1}+r_1)}{L_1} & 0 & -\frac{1}{L_1} & 0 \\ 0 & -\frac{r_2}{L_2} & 0 & 0 \\ -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_2(R+r_{C_2})} \end{bmatrix}$$

A_2

$$\begin{bmatrix} -\frac{r_1+a_1}{L_1} & -\frac{a_1}{L_1} & 0 & -\frac{Re}{L_1} \\ -\frac{a_1}{L_2} & -\frac{r_2+r_{C_1}+a_1}{L_2} & -\frac{1}{L_2} & -\frac{Re}{L_2} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{Re}{C_2} & \frac{Re}{C_2} & 0 & -\frac{Re}{C_2R} \end{bmatrix}$$

A_3

$$\begin{bmatrix} -\frac{r_1+a_1}{L_1} & -\frac{a_1}{L_1} & 0 & -\frac{Re}{L_1} \\ -\frac{a_1}{L_2} & -\frac{a_1+r_2+r_{C_1}}{L_2} & -\frac{1}{L_2} & \frac{-R+a_1}{L_2R} \\ 0 & \frac{1}{C_1} & 0 & 0 \\ \frac{Re}{C_2} & \frac{Re}{C_2} & 0 & -\frac{Re}{RC_2} \end{bmatrix}$$

$$Re = \frac{R}{R + r_{C_2}};\ a_1 = (Re)\, r_{C_2}$$

B

$$B_1 = B_2 = \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix};\ B_3 = \begin{bmatrix} 0 & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}$$

E

$$E_1 = [0 \quad 0 \quad 0 \quad Re];\ E_2 = E_3 = [a_1 \quad a_1 \quad 0 \quad Re]$$

$$P_1 = P_2 = P_3 = [0\ 1\ 0\ 0]$$

$$\frac{dx}{dt} = (d_2A_1 + (d_1 - d_2)A_2 + (1 - d_1)A_3)x(t) + \big(B_1d_2 + B_2(d_1 - d_2) + B_3(1 - d_1)\big)u(t) \tag{5}$$

$$Y = (d_2E_{01} + (d_1 - d_2)E_{02} + (1 - d_1)E_{03})x(t) + \big(F_1d_2 + F_2(d_1 - d_2) + F_3(1 - d_1)\big)u(t) \tag{6}$$

$$x(t) = X + \hat{x}, u(t) = U + \hat{u}, y(t) = Y + \hat{y}; d_1 = D_1 + \hat{d}_1, d_2 = D_2 + \hat{d}_2, 1 - d_1 = d_1^{'} = D^{'}_1 - \hat{d}_1 \tag{7}$$

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u} + \big((A_2 - A_3)X + (B_2 - B_3)U\big)\hat{d}_1 + \big((A_1 - A_2)X + (B_1 - B_2)U\big)\hat{d}_2 \tag{8}$$

$$\hat{y} = E_0\hat{x} + F\hat{u} + \big((E_{02} - E_{03})X + (F_2 - F_3)U\big)\hat{d}_1 + \big((E_{01} - E_{02})X + (F_1 - F_2)U\big)\hat{d}_2 \tag{9}$$

$$\begin{bmatrix} \hat{v}_0(s) \\ \hat{i}_g(s) \end{bmatrix} = \begin{bmatrix} E[sI - A]^{-1}\gamma_1 + \psi_1 & E[sI - A]^{-1}\gamma_2 + \psi_2 \\ P[sI - A]^{-1}\gamma_1 + \psi_3 & P[sI - A]^{-1}\gamma_2 + \psi_4 \end{bmatrix} \begin{bmatrix} \hat{d}_1(s) \\ \hat{d}_2(s) \end{bmatrix} = \begin{bmatrix} G_{11}(s) & G_{12}(s) \\ G_{21}(s) & G_{22}(s) \end{bmatrix} \begin{bmatrix} \hat{d}_1(s) \\ \hat{d}_2(s) \end{bmatrix} \tag{10}$$

where $A = d_1A_1 + (d_2 - d_1)A_2 + (1 - d_2)A_3;\ \ B = d_1B_1 + (d_2 - d_1)B_2 + (1 - d_2)B_3$

$P = d_1P_1 + (d_2 - d_1)P_2 + (1 - d_2)P_3;\ \ E = d_1E_1 + (d_2 - d_1)E_2 + (1 - d_2)E_3$

$\gamma_1 = [(A_1 - A_2)X + (B_1 - B_2)U];\ \ \gamma_2 = [(A_2 - A_3)X + (B_2 - B_3)U]$

$\psi_1 = [(E_1 - E_2)X];\ \psi_2 = [(E_2 - E_3)X];\ \psi_3 = [(P_1 - P_2)X];\ \psi_4 = [(P_2 - P_3)X]$

$$\begin{bmatrix} \hat{v}_0(z) \\ \hat{i}_g(z) \end{bmatrix} = \begin{bmatrix} E_i[zI - \phi]^{-1}\gamma_1 & E_i[zI - \phi]^{-1}\gamma_2 \\ P_i[zI - \phi]^{-1}\gamma_1 & P_i[zI - \phi]^{-1}\gamma_2 \end{bmatrix} \begin{bmatrix} \hat{d}_1(z) \\ \hat{d}_2(z) \end{bmatrix} = \begin{bmatrix} G_{11}(z) & G_{12}(z) \\ G_{21}(z) & G_{22}(z) \end{bmatrix} \begin{bmatrix} \hat{d}_1(z) \\ \hat{d}_2(z) \end{bmatrix} \tag{11}$$

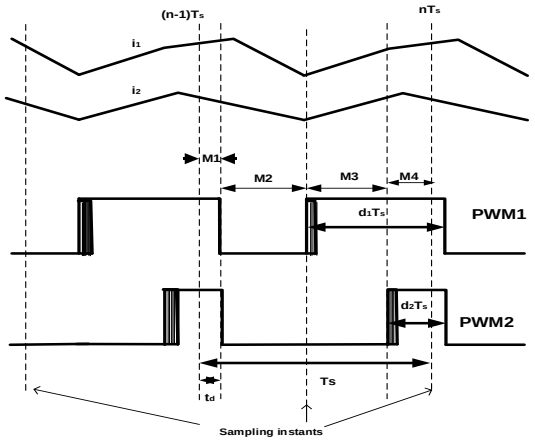


Fig. 3: Leading-edge interval-1 sampling

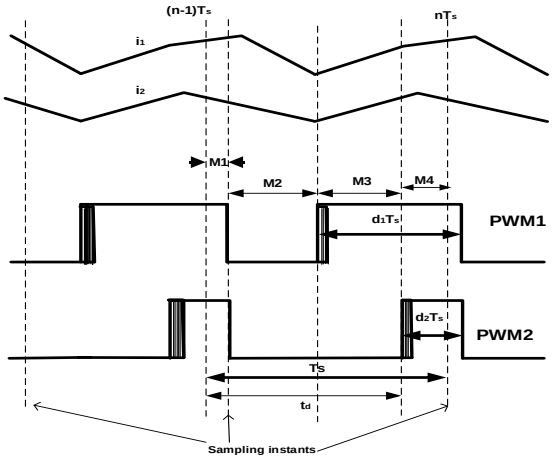


Fig. 4: Leading-edge interval-2 sampling

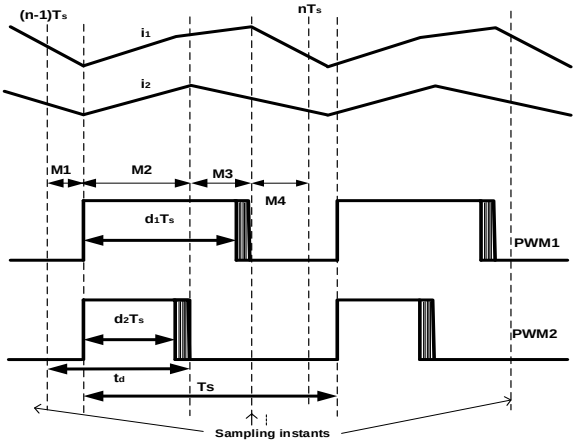


Fig. 5: Trailing-edge interval-1 sampling

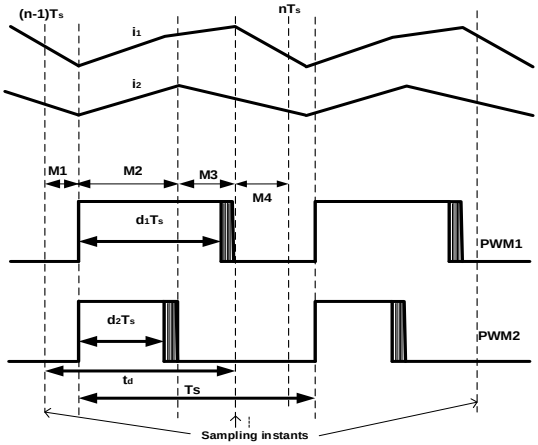


Fig. 6: Trailing-edge interval-2 sampling

To derive TFM, the output variables, state variables and input variables (duty cycles) are perturbed at a steady-state operating point as given in equation (7) and each variable becomes steady-state values plus superimposed small ac variations. Here, the steady-state variables state, input, output, and duty cycles are denoted using X, U, Y, D_1, D_2 and the small ac variations in state, input, output, and duty cycles are denoted by $\hat{x}, \hat{u}, \hat{y}, \hat{d}_1, \hat{d}_2$

Substitute the perturbed variables as given in equation (7) in the state and output equations (5) & (6), the resulting equation contains steady-state values, linear terms of small ac variations, and higher order non-linear (H.O.NL) terms in both state and output equations. The small signal TFM model is obtained by considering only linear terms of small variations by dropping the nonlinear product terms. These are given in equation (8) and equation (9). Taking the Laplace transform of these equations and substitution of $\hat{x}(s)$ in each individual output equation and resulting equation is given in equation (10).

$$\begin{bmatrix}\hat{v}_0(s)\\ \hat{i}_g(s)\end{bmatrix} = \begin{bmatrix}G_{11}(s) & G_{12}(s)\\ G_{21}(s) & G_{22}(s)\end{bmatrix}\begin{bmatrix}\hat{d}_1(s)\\ \hat{d}_2(s)\end{bmatrix}$$

$$\begin{bmatrix}\hat{v}_0(z)\\ \hat{i}_g(z)\end{bmatrix} = \begin{bmatrix}G_{11}(z) & G_{12}(z)\\ G_{21}(z) & G_{22}(z)\end{bmatrix}\begin{bmatrix}\hat{d}_1(z)\\ \hat{d}_2(z)\end{bmatrix} \quad (12)$$

4 Derivation of TFM using Small-Signal Discrete-Time Model

Small-signal continuous time model is one popular method to obtain the TFM and discussed in the previous section. TFM can also be obtained in discrete-time using a small-signal discrete-time model. The transfer function obtained using this method for boost converter exhibits deviation in

phase characteristics at high frequencies as compared to the small-signal continuous-time model. To identify the presence of any deviation in phase response characteristics, the procedure to derive TFM using discrete-time model is discussed in the following paragraphs. Discrete-time models are naturally matched with integrated dc-dc converters because power converters are controlled and operated in a cyclic manner. The discrete-time models can be obtained in two different ways trailing-edge and leading-edge digital pulse width modulation and each one can be modelled in interval-1 and interval-2 samplings. Procedural steps for formulation of discrete-time model for trailing edge and leading edge are similar and require digital pulse-width modulation (DPWM) gating diagrams. Gating diagrams for leading-edge DPWM with interval-1 and interval-2 sampling are shown in Figure 3 and Figure 4 respectively. Gating diagrams for trailing-edge DPWM with interval-1 and interval-2 sampling are shown in Figure 5 and Figure 6 respectively. Using these gating diagrams, the procedural steps to derive discrete-time small-signal models are enumerated as follows.

(i) Consider $([(n-1)T_s] < t < [nT_s])$ as one switching time period and divide this period into sub-intervals of specific numbers based on the operating modes as shown in following figures (Figure 3, Figure 4, Figure 5 and Figure 6). Here, four sub-intervals are considered namely M1, M2, M3, and M4.

(ii) Consider the first sub-interval 'M1' as shown in Figure 5, and identify the operating mode corresponding to this M1. The specific mode depends on the conduction periods of switches and diodes. Here, the two switches are in OFF condition. Therefore, it indicates mode-3.

(iii) Corresponding to this operating mode, obtain the solution of the state equation. The solution of state-equation is obtained in terms of different equations. Here, the value of the state-variable at the end of a specific interval is obtained in terms of its starting point of the corresponding interval i.e., the transition in state variables in discrete-time are obtained.

(iv) Repeat the steps (ii) and (iii) for M2, M3, M4. The final solution is obtained by stacking these solutions.

(v) The small-signal discrete-time TFM is obtained and given in equation (11). The values of Γ_1, Γ_2, ϕ, and (K_1& K_2), for trailing edge and leading edge are given in Table 4 and Table 5 respectively.

Table 4. Small Signal Discreate Model Parameters of TI-BS Converter with Trailing Edge DPWM

S.No.	Trailing Edge Interval-1 Sampling	Trailing Edge Interval-2 Sampling
k_1	$(A_2 - A_3)X + (B_2 - B_3)U$	$(A_2 - A_3)X + (B_2 - B_3)U$
k_2	$(A_1 - A_2)X + (B_1 - B_2)U$	$(A_1 - A_2)X + (B_1 - B_2)U$
Γ_1	$k_1 T_S e^{A_3[T_S - d_1 T_S - t_d + d_2 T_S]}$	$k_1 T_S e^{A_3[T_S - t_d]}$
Γ_2	$k_2 T_S e^{A_3[T_S - d_1 T_S - t_d + d_2 T_S]} e^{A_2[d_1 - d_2]T_S}$	$k_2 T_S e^{A_3[T_S - t_d]} e^{A_2[d_1 - d_2]T_S}$
ϕ	$(e^{A_3[T_S - d_1 T_S - t_d + d_2 T_S]} * e^{A_3[t_d - d_2 T_S]} * e^{A_2[d_1 - d_2]T_S} * e^{A_1 d_2 T_S})$	$(e^{A_3\lfloor T_S - d_1 T_S - t_d + d_2 T_S \rfloor} * e^{A_3\lfloor t_d - d_2 T_S \rfloor} * e^{A_2\lfloor d_1 - d_2 \rfloor T_S} * e^{A_1 d_2 T_S})$

Table 5. Small Signal Discrete Model Parameters of TI-BS Converter with Trailing Edge DPWM

S.No	Leading Edge Interval-1 Sampling	Leading Edge Interval-2 Sampling
k_1	$(A_2 - A_3)X + (B_2 - B_3)U$	$(A_2 - A_3)X + (B_2 - B_3)U$
k_2	$(A_1 - A_2)X + (B_1 - B_2)U$	$(A_1 - A_2)X + (B_1 - B_2)U$
Γ_1	$k_1 T_S e^{A_2[d_1 - d_2]T_S}$	$k_1 T_S e^{A_2[d_1 - d_2]T_S} e^{A_1[T_S - t_d]}$
Γ_2	$k_2 T_S e^{A_1[-t_d + d_2 T_S]} e^{A_2[d_1 - d_2]T_S}$	$k_2 T_S e^{A_1[-t_d + T_S]}$
ϕ	$(e^{A_1\lfloor -t_d + d_2 T_S \rfloor} * e^{A_2\lfloor d_1 - d_2 \rfloor T_S} * e^{A_3\lfloor 1 - d_1 \rfloor T_S} * e^{A_1 t_d})$	$(e^{A_1\lfloor -t_d + T_S \rfloor} * e^{A_2\lfloor d_1 - d_2 \rfloor T_S} * e^{A_3\lfloor 1 + d_2 - 2d_1 \rfloor T_S} * e^{A_1[t_d - (1 - d_1)T_S]})$

5 Results & Discussions

5.1 Simulation Results

To extract the features of TI-BS dc-dc converter, a 48 V, 500 W, system is considered for analysis and simulation. Time-domain analysis is carried out for obtaining the design equations of various parameters. The design equations for converter parameters are given in Table 2 and these are used to obtain parameter values. The specifications and parameters considered are as follows: Vg1=60 V, Vg2=36 V, R=6Ω +/- 50%, fs=50 kHz, P0=500 W, L1=300 µH, L2=300 µH, C1=60 µF, and C2=60 µF.

Using the parameters given in the above paragraph, the frequency response of the TI-BS dc-dc converter is obtained in the MATLAB environment considering continuous-time as well as discrete-time models. The four different discrete-time models along with continuous-time models are used to obtain the frequency response characteristics. Here, the four discrete-time models considered are trailing-edge DPWM scheme with interval-1 & interval-2 sampling and leading edge DPWM scheme with interval-1 & interval-2 sampling. The TFMs are obtained in the MATLAB environment. The TFM representations of TI-BS dc-dc converter in continuous and discrete-time are given in equation (12). The elements of each TFM are computed in MATLAB environment for TI-BS converter considering (i) continuous-time (ii) trailing-edge DPWM (iii) leading-edge DPWM and these are given using equation (13) to equation (17).

TI-BS Converter

$$\begin{bmatrix} G_{11}(s) \\ G_{12}(s) \\ G_{21}(s) \\ G_{22}(s) \end{bmatrix} = \begin{bmatrix} \dfrac{1396s^3 + 2.326\times10^9 s^2 + 1.163\times10^{11}s + 9.046\times10^{16}}{s^4 + 5279s^3 + 7.678\times10^7 s^2 + 1.172\times10^{11}s + 6.051\times10^{14}} \\ \dfrac{-0.2148s^4 - 3.558\times10^5 s^3 + 3.717\times10^9 s^2 + 60.61\times10^{11}s + 3.484\times10^{16}}{s^4 + 5279s^3 + 7.678\times10^7 s^2 + 1.172\times10^{11}s + 6.051\times10^{14}} \\ \dfrac{-4.652\times10^6 s^2 - 3.101\times10^{12}s + 1.211\times10^{16}}{s^4 + 5279s^3 + 7.678\times10^7 s^2 + 1.172\times10^{11}s + 6.051\times10^{14}} \\ \dfrac{1.714\times10^5 s^3 + 2.563\times10^9 s^2 + 5.862\times10^{12}s + 2.329\times10^{16}}{s^4 + 5279s^3 + 7.678\times10^7 s^2 + 1.172\times10^{11}s + 6.051\times10^{14}} \end{bmatrix} \quad (13)$$

TI − BS Trailing Edge (Interval − 1)

$$\begin{bmatrix} G_{11}(z) \\ G_{12}(z) \\ G_{21}(z) \\ G_{22}(z) \end{bmatrix} = \begin{bmatrix} \dfrac{0.4445z^3 - 0.4456z^2 - 0.4239z + 0.4387}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{-5.339z^3 + 17.54z^2 - 19.01z + 6.817}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{-0.005319z^3 - 0.0164z^2 + 0.02706z - 0.003553}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{3.947z^3 - 10.85z^2 + 9.906z - 3.001}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \end{bmatrix} \quad (14)$$

TI − BS Trailing Edge (Interval − 2)

$$\begin{bmatrix} G_{11}(z) \\ G_{12}(z) \\ G_{21}(z) \\ G_{22}(z) \end{bmatrix} = \begin{bmatrix} \dfrac{0.5462z^3 - 0.7499z^2 - 0.1196z + 0.337}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{-5.102z^3 + 16.86z^2 - 18.35z + 6.603}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{-0.008023z^3 - 0.01308z^2 + 0.0285z - 0.00563}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{4.009z^3 - 11.04z^2 + 10.11z - 3.07}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \end{bmatrix} \quad (15)$$

TI − BS Leading Edge (Interval − 1)

$$\begin{bmatrix} G_{11}(z) \\ G_{12}(z) \\ G_{21}(z) \\ G_{22}(z) \end{bmatrix} = \begin{bmatrix} \dfrac{0.3932z^3 - 0.2924z^2 - 0.577z + 0.4899}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{-6.351z^3 + 20.47z^2 - 21.83z + 7.72}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{-0.004171z^3 - 0.01746z^2 + 0.02574z - 0.002317}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{3.682z^3 - 10.03z^2 + 9.056z - 2.708}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \end{bmatrix} \quad (16)$$

$$\text{TI} - \text{BS Leading Edge (Interval} - 2)$$

$$\begin{bmatrix} G_{11}(z) \\ G_{12}(z) \\ G_{21}(z) \\ G_{22}(z) \end{bmatrix} = \begin{bmatrix} \dfrac{0.3862z^3 - 0.2648z^2 - 0.6033z + 0.4956}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{-6.801z^3 + 21.78z^2 - 23.11z + 8.129}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{0.0008506z^3 - 0.006868z^2 - 0.007893z + 0.01585}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \\ \dfrac{3.428z^3 - 9.235z^2 + 8.236z - 2.426}{z^4 - 3.87z^3 + 5.641z^2 - 3.6171z + 0.8998} \end{bmatrix} \quad (17)$$

The Bode plot of "G11" of TI-BS converter considering continuous-time and Trailing-edge discrete-time models is plotted and it is shown in Figure 7. From this plot two important characteristics can be extracted. (i) The magnitude plot of this system in continuous and discrete-time domains is the same. (ii) There is a sudden change in magnitude (called as down-up glitch) and also in phase angle plots around the frequency 1000 Hz and this is due to the presence of one pair of the poles (at a frequency of 3130 rad/sec) and also pair of the zeros (at a frequency of 6230 rad/sec). The phase angle is also decreased by 180 degrees due to the pair of poles and an increase in phase angle due to the presence of a pair of zeros. The pole-zero plot of this system is shown in Figure 8 and Figure 9. From this map, it is observed that all the zeros of this system are within the unit circle.

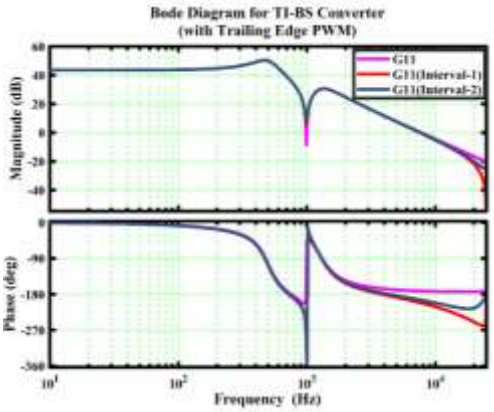


Fig. 7: Bode diagram of G_{11} for TI-BS Converter with Trailing Edge DPWM

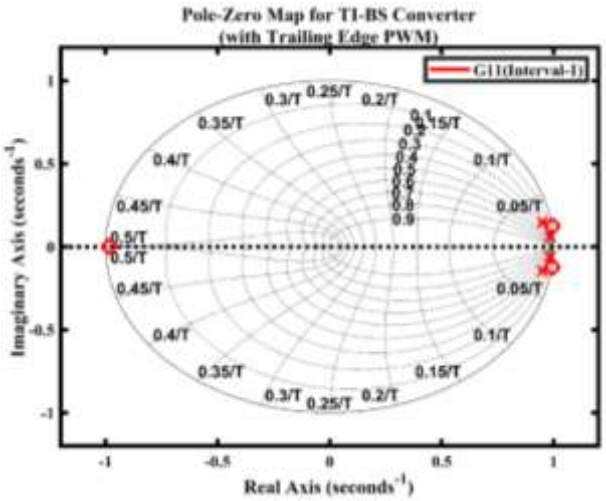


Fig. 8: Pole Zero Map of G_{11} for Trailing Edge TI-BS Converter Interval-1 Sampling

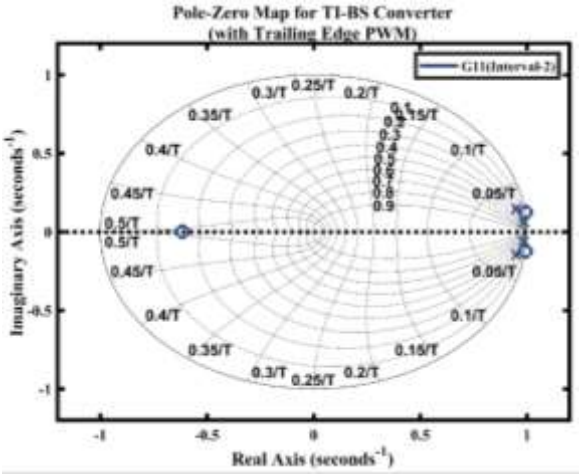


Fig. 9: Pole Zero Map of G_{11} for Trailing Edge TI-BS Converter Interval-2 Sampling

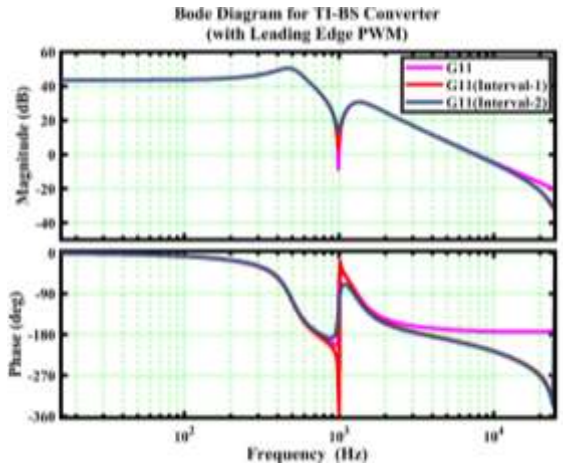


Fig. 10: Bode diagram of G_{11} for TI-BS Converter with Leading Edge DPWM

The Bode plot of "G11" of TI-BS converter considering continuous-time and leading-edge discrete-time models is plotted and it is shown in Figure 10. From this plot, it is observed that phase response of interval-1 and interval-2 discrete-time models is deviated by 90° at high frequencies. The PZ maps of these discrete-time systems are shown in Figure 11 and Figure 12. It is observed from these plots that one zero of interval-1 as well as interval-2 discrete-time models are outside the unit circle. If Right Hand Plane (RHP) zero bode-plot is drawn alone. The 'n' number of RHP zeros introduces an extra phase lag of n*90° at high frequencies which is elaborated in section 5.2, due to this fact non-minimum phase behavior is observed. This characteristic is observed from the phase plot of Figure 10. The RHP zeros can also affect the bandwidth of the system and also the initial direction of the time response. Therefore, a leading-edge digitally controlled TI-BS system is exhibiting non-minimum phase behavior due to the presence of zero outside the unit circle.

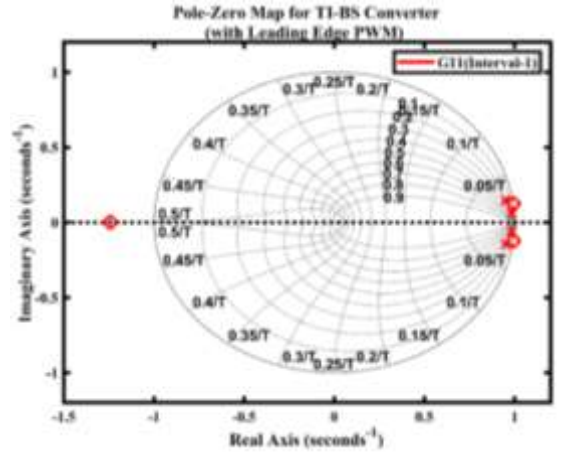


Fig. 11: Pole Zero Map of G_{11} for Leading Edge TI-BS Converter Interval-1 Sampling

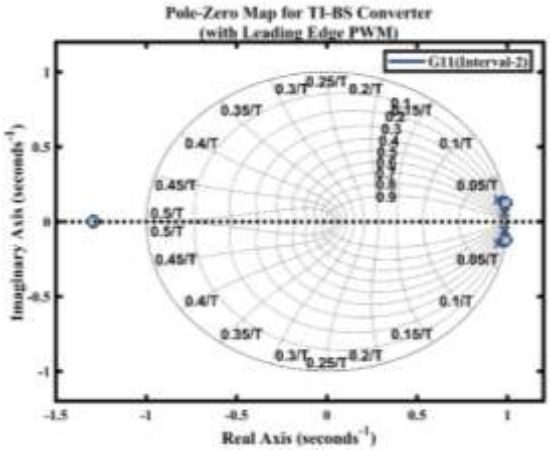


Fig. 12: Pole Zero Map of G_{11} for Leading Edge TI-BS Converter Interval-2 Sampling

5.2 The Effect of RHP Zero

To extract the salient features of the frequency response for the systems with RHP zeros bode plots are drawn. Figure 13 shows the frequency response of a simple plant without any RHP zero (whose transfer function is (***s+1.3***)). Figure 14 shows the frequency response of a plant with RHP zero (whose transfer function is (***s-1.3***)). It is observed that the magnitude plot in these two cases is the same whereas the phase characteristics are opposite. Because of this phase deviation extra phase lag is seen for the systems with RHP zeros. The 'n' number of RHP zeros introduces an extra phase-lag of n*90°.

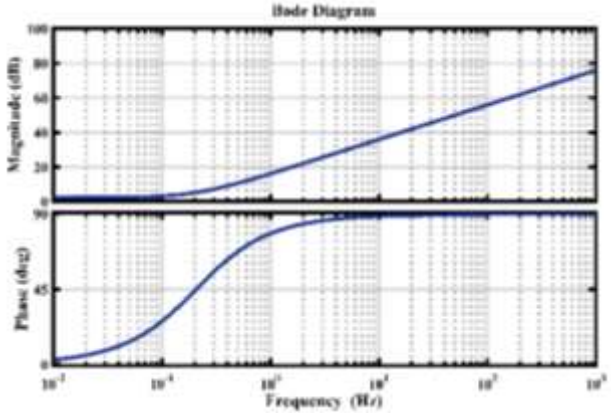


Fig. 13: Bode plot response for Left Hand Plane Zero Zero

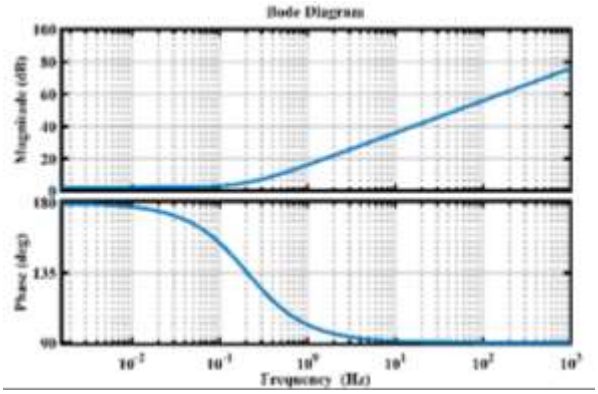


Fig. 14: Bode plot response for Right Hand Plane Zero

5.3 PSIM Results

Open-loop simulation results of the TI-BS converter for the chosen source voltages (V_{g1}, V_{g2}) and the designed parameters (L_1, L_2, C_1, C_2) are plotted in the PSIM environment. Here, converter source voltages (V_{g1}=60V, V_{g2}=36V), output voltage and current (V_0=48V(fixed), i_0), inductor currents (i_{L1} and i_{L2}), duty cycles (d_1=0.58, d_2=0.3(fixed)) are shown in Figure15, Figure 16, Figure 17 and Figure 18 with load resistance of 6Ω (designed value).

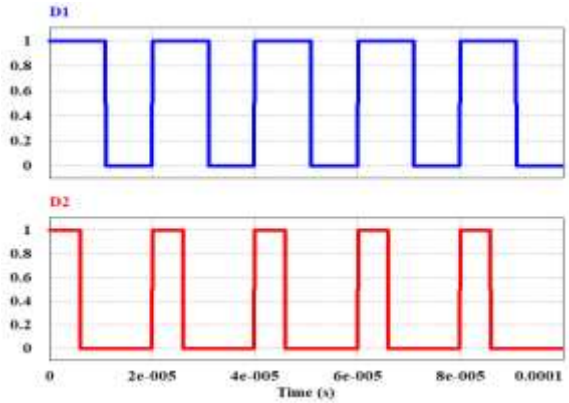


Fig. 15: Duty cycles: Switch-1and Switch-2 of TI-BS Converter

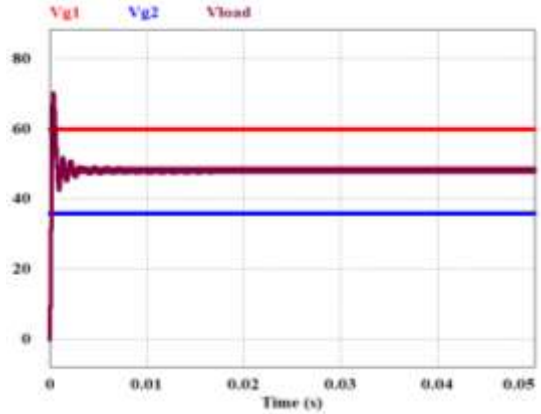


Fig. 16: Input voltages and Load voltage of TI-BS Converter

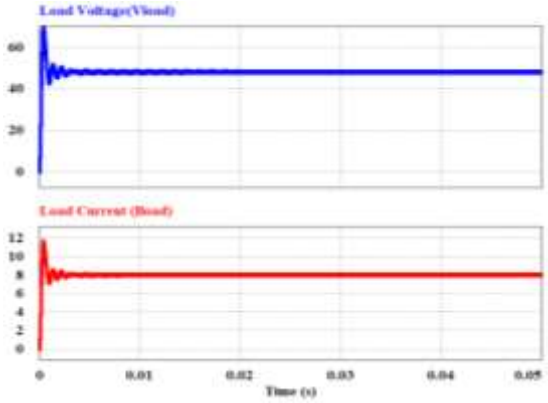


Fig. 17: Load voltage and Load Current of TI-BS Converter

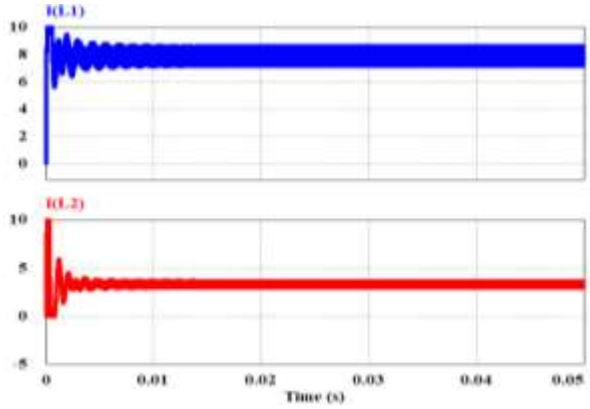


Fig. 18: Inductor Currents of TI-BS Converter

The open-loop simulations of the TI-BS dc-dc converter are performed in the PSIM environment with designed parameters and with load resistance of 9Ω, these are presented in Figure 19 and Figure 20.

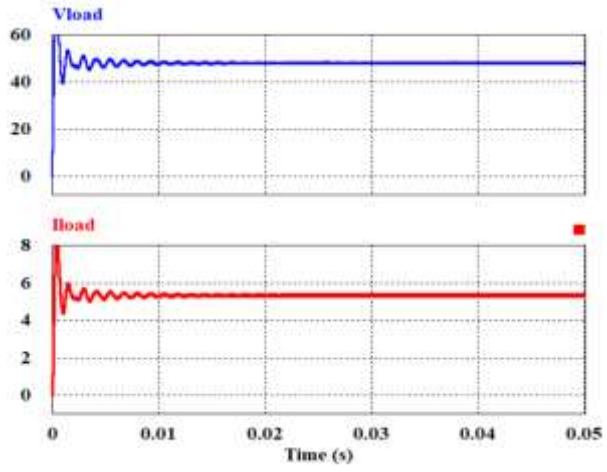


Fig. 19: Load voltage and Load Current of TI-BS Converter for R=9Ω

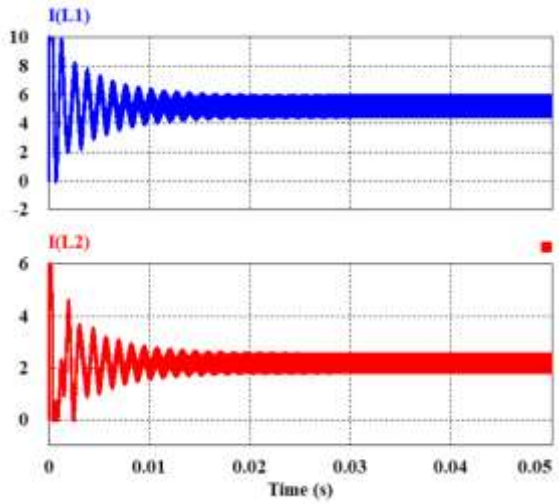


Fig. 20: Inductor Currents of TI-BS Converter for R=9Ω

The open-loop simulations TI-BS dc-dc converter are also performed with a load resistance of 3Ω, these are presented in Figure 21 and Figure 22.

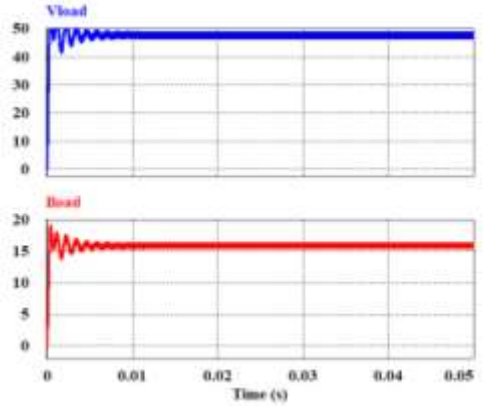


Fig. 21: Load voltage and Load Current of TI-BS Converter for R=3Ω

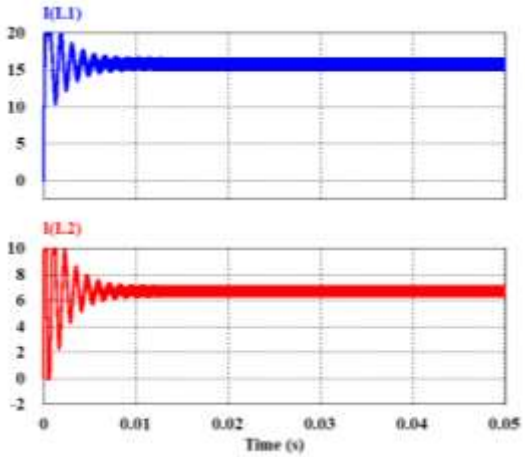


Fig. 22: Inductor Currents of TI-BS Converter for R=3Ω

The converter (V_0&I_0), and (i_{L1}&i_{L2}) are also plotted respectively in Figure 23 and Figure 24, considering the load resistances of 3 Ω during 0 to 30 msec, 6 Ωduring 30 to 60 msec and 9 Ω during 60 to 100 msec. It is observed that all currents are changing but V_0 is constant. Here, the inductor currents which reflect the source currents are affected in each case.

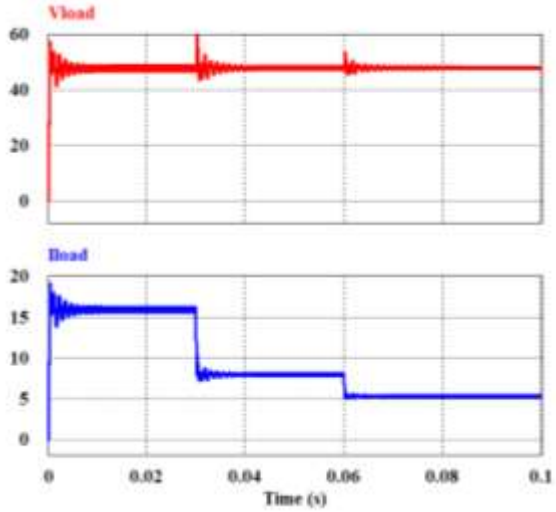


Fig.23: Load voltage and Load Current of TI-BS Converter with Dynamic Load Variations

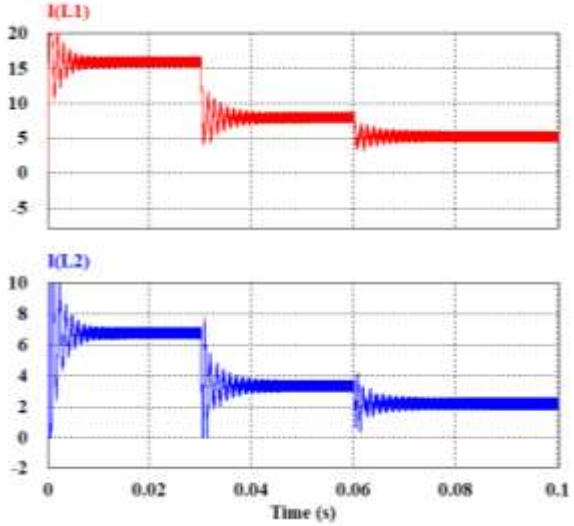


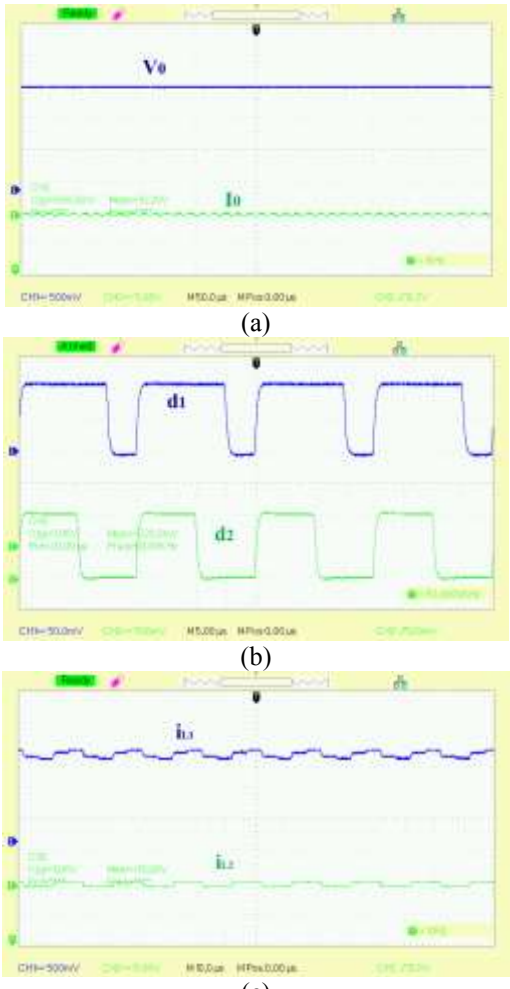
Fig.24: Inductor Currents of TI-BS Converter with Dynamic Load Variations

5.4 Experimental Results

The designed parameters as given in the starting of section-V, the real-time simulation results are captured using OPAL-RT test bench OPEL4510 and it is shown in Figure 25. Hardware-in-the-Loop (HIL) configuration is the Real-time Testing environment, [20], [21] that involves connecting real signals from a controller to a test system that

simulates reality. The real-time simulated results of converter output voltage(V_0), load current(I_0), Duty ratios (d_1 and d_2), and Inductor currents (i_{L1}, i_{L2}) are captured using Digital Storage Oscilloscope (DSO) and these are presented for TIBS converters. Here, V_0, I_0, (d_1 and d_2), (i_{L1} and i_{L2}) are shown using Figure 26(a)-26(c).

Fig. 25: Real Time Simulator Test-Bench OPEL4510



(a)

(b)

(c)

Fig. 26: (a) Output Voltage(V_0) and Load Current(I_0), (b) Duty ratios d_1 and d_2, (c) Inductor currents i_{L1}, i_{L2} for TI-BS Converter

6 Conclusion

TI-BS dc-dc converter is considered to extract the effect of modeling on frequency response characteristics. For these two converters, TFMs are derived by considering leading-edge and trailing-edge DPWM schemes that include time delay effects. The timing diagrams are shown graphically based on definitions of interval-1 and interval-2 DPWM schemes. That resulted in four different types of modulation schemes. For all these cases, with the designed parameters, the transfer functions are obtained and these are presented. The frequency response characteristics are also plotted for all cases in the MATLAB environment. For leading-edge modulation non-minimum phase response is observed and it is proved graphically by plotting the pole zero and Bode plots. The TI-BS converter with leading edge modulation is exhibiting non-minimum phase behavior because of a zero present outside of the unit circle.

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- A. Venkatesh, B. Amarendra Reddy carried out the formal analysis and mathematical modeling of this article.
- A. Venkatesh performed simulations and taken results for this article.
- A. Venkatesh, B. Amarendra Reddy, T. R.Jyothsna wrote this article.
- B. Amarendra Reddy, T. R. Jyothsna reviewed, edited and perform the data correction in this article.
- B. Amarendra Reddy, T. R. Jyothsna supervised this article.

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