A Novel Hybrid PWM Technique for Asymmetric Inverter

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Abstract: - Multi-Level Inverters (MLIs) are achieving broad popularity owing to the rapid development of power semiconductor devices. The capability of MLIs became recognized as a significant aspect of a system heavily reliant on Pulse Width Modulation(PWM) strategy. The conventional high frequency PWM techniques suffer from significant Total Harmonic Distortion (THD) along with power loss difficulties. This work recommends a hybrid PWM technique for lowering the THD and power loss of VSI adding the benefits of level-shift PWM and Phase-shift PWM. A novel form of carrier signals is employed in the proposed hybrid PWM technique. In contrast to existing PWM techniques, the proposed hybrid PWM technique minimizes switching and conduction power losses. In this work, the proposed PWM scheme is employed for asymmetric multilevel inverter. The proposed configuration is also examined using PLECS software to estimate losses and efficiency. The simulation work is done in the MATLAB/Simulink environment and the OPAL-RT(OP4510) test platform is employed to evaluate topology performance.

Key-Words: - Hybrid PWM, Multi-level Inverter, Total Harmonic Distortion, DC-AC conversion, Total Standing Voltage, OPAL-RT(OP4510).

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1 Introduction

Multilevel inverters (MLI) are progressively acquiring significant value in renewable energy conversion and industrial applications due to their superior waveform of output to two-level inverters. The traditional two-level inverter is inadequate for implementation in the applications as mentioned earlier for several unanticipated limitations like higher harmonic distortion, less efficiency, reduced power quality, and so on. Considering these scenarios, MLIs have proven to serve as a viable substitute for an extensive range of purposes, [1],[2].

The traditional MLI configurations with names like Neutral Point Clamped MLI (NPCMLI), Flying Capacitor MLI (FCMLI), and Cascaded H-Bridge MLI (CHBMLI) have become prevalent for industrial applications, [3], [4]. The CHB inverter topology necessitates minimal component count than other conventional inverter topologies for creating an identical level of output. CHB inverters are transitioning from a traditional perspective to real-world applications due to capabilities that include high degree of modularity, and the ability to safely link to medium voltage with superior power quality, [5].

The positive effects of employing higher levels encompass increased effectiveness, minimized filter size, significant power density, and accuracy, along with an expanded application spectrum. Nevertheless, investigators experienced certain obstacles during minimizing component counts like increased rated voltage of switching devices, losses in versatility, reduction in the number of associated states, random demands for bidirectional switches, novel control methodologies, and an enormous prevalence of sources to achieve the predicted levels count from currently topologies, [6], [7], [8], [9].

In [10], the authors compare the conventional CHB (symmetric) configuration to the asymmetric configuration. An arrangement of full and half bridges to lower carrier count to acquire an identical number of levels is illustrated, [11]. A cascaded inverter with a trinary combination of sources is examined for distinct pulse width modulation techniques, [12]. The suggested structure minimizes the demand for bidirectional switches concerning the proper placement of dc sources with switches, [13].

An eleven-level inverter with minimal components and five sources is investigated, [14]. Various levels of cascaded inverters considering the aspects of harmonic distortion and fewer device

counts for electric vehicle applications are suggested, [15]. In [16], author recommends a unique eleven level inverter utilizing reduced switches, minimizing control complexity and cost reduction. Analysis of various modulation schemes for distinct levels is offered under regulating loads, [17]. Hybrid PWM, Conventional PWM as well as stair case PWM are contrasted for the study of THD, switching losses, and lower order harmonic in the case of fifteen -level inverters, [18].

A nine-level MLI structure using minimal switching and dc sources is proposed, and the results are evaluated, [19]. To address the challenges associated with the nine-level inverter, a seventeen-level MLI was proposed and executed, as well as increasing the number of levels without the impact of component ratings, [20]. A comparison of various PV-inverter topologies is simulated to minimize leakage current variation, [21]. Packed E-cell configuration utilizing nearest level modulation for PV applications is investigated through OPAL-RT test bed, [22]. Typhoon Hardware-in -loop simulator results are mentioned for the nine-level inverter, [23]. An improvised asymmetrical configuration using fundamental switching modulation is investigated, [24]. A (2n+1) level inverter is demonstrated with capacitor voltage balancing ability, [25]. A novel MLI structure is developed utilizing unidirectional and bidirectional switches, [26].

Various modulation techniques are indicated in Figure 1. Modulation techniques are categorized as High Frequency Scheme (HFS) or Low Frequency Scheme (LFS) based on the frequency of the carrier. LSPWM and PSPWM techniques are HFS methods typically recommended for medium-voltage applications. In contrast to PSPWM, LSPWM method power losses are not distributed uniformly among the cells, but THD is minimal. By taking the merits of both methods a new method (PLSPWM) is proposed.

Subject to the level of output voltage developed CHBMLI is generally categorized as symmetric or asymmetric. Those are (i) equal voltage cascaded MLI(ECHBMLI), where all input voltages are in equal magnitude, (ii)natural sequence cascaded MLI(NSCHBMLI), where all input voltage follows arithmetic progression each is differed by one, (iii) binary cascaded MLI(BCHBMLI), where successive input voltages are doubled,(iv)trinary cascaded MLI(TCHBMLI), in which successive input voltages are tripled,(v)quasi-linear cascade MLI(QCHBMLI), where all input voltages are kept constant so that the anticipated resulting voltage is reached.

In this work, QCHBMLI topology is presented using the PLSPWM technique. The suggested work offers the following benefits:

- The implementation of the application to PLSPWM has been successful, which is simple and easy to set up with minimal switching stress.
- It works well for any variety of loads.
- Four devices operate at fundamental frequency, reducing switching losses and improving effectiveness.
- The work outlines a new cascade inverter and open-loop system that is tested through the OPAL-RT simulator.

The rest of the work is organized as follows. Section 2 discusses the proposed topology, including its operating modes and modulation technique. Section 3 addresses the voltage stress and loss analysis. Section 4 compares the proposed topology to other topologies. Section 5 provides simulation, thermal modeling, and OPAL-RT results to help to understand the performance of the proposed topology. Section 6 about the work's conclusion.

2 Proposed Topology

Figure 2 shows the planned H-bridge configuration, it has three voltage sources and twelve switches that are IGBTs in antiparallel with diodes. The subsections that follow describe the switching states and operating modes of the 11-level configuration.

2.1 Operating Modes

A QCHBMLI arrangement operating mode is depicted in Figure 3. The first voltage source(V_1) is assumed as the base source, while the other two voltage sources (V_2 &V_3) are of equal magnitude and double the value of the base source. The switches that are linked to voltage sources (V_2 &V_3) have equal voltage ratings, while other switches' ratings are different. Table 1 displays the switching pattern for producing various output levels. The following is an explanation of the modes of operation.

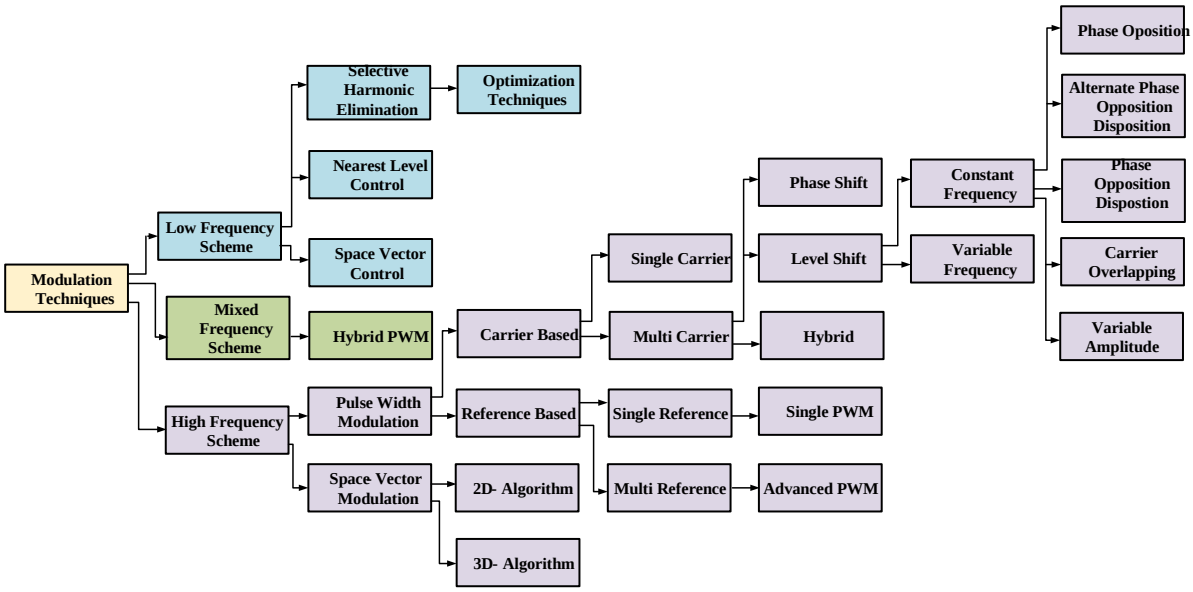


Fig. 1: Various Modulation Technique

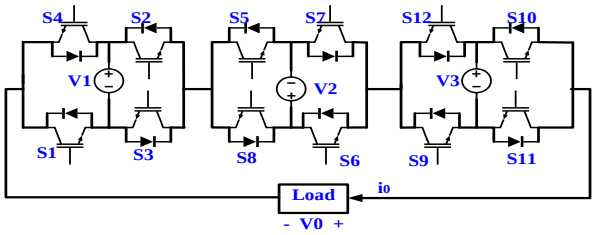
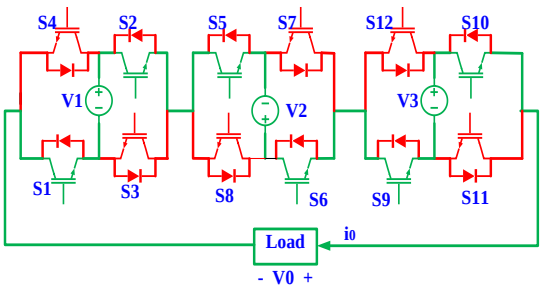
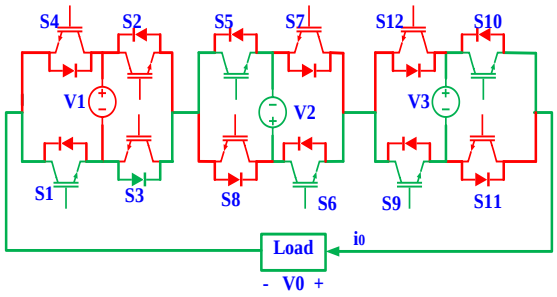


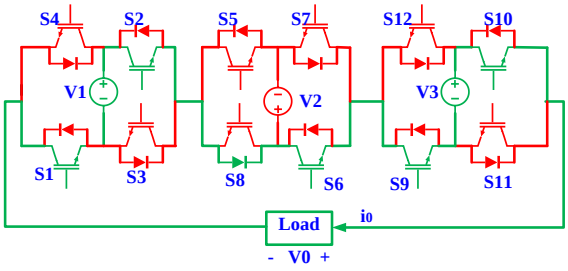
Fig. 2: The basic Model of Topology



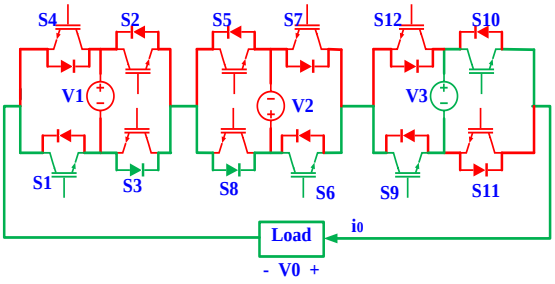
(a). $V0=+5V_{in}$



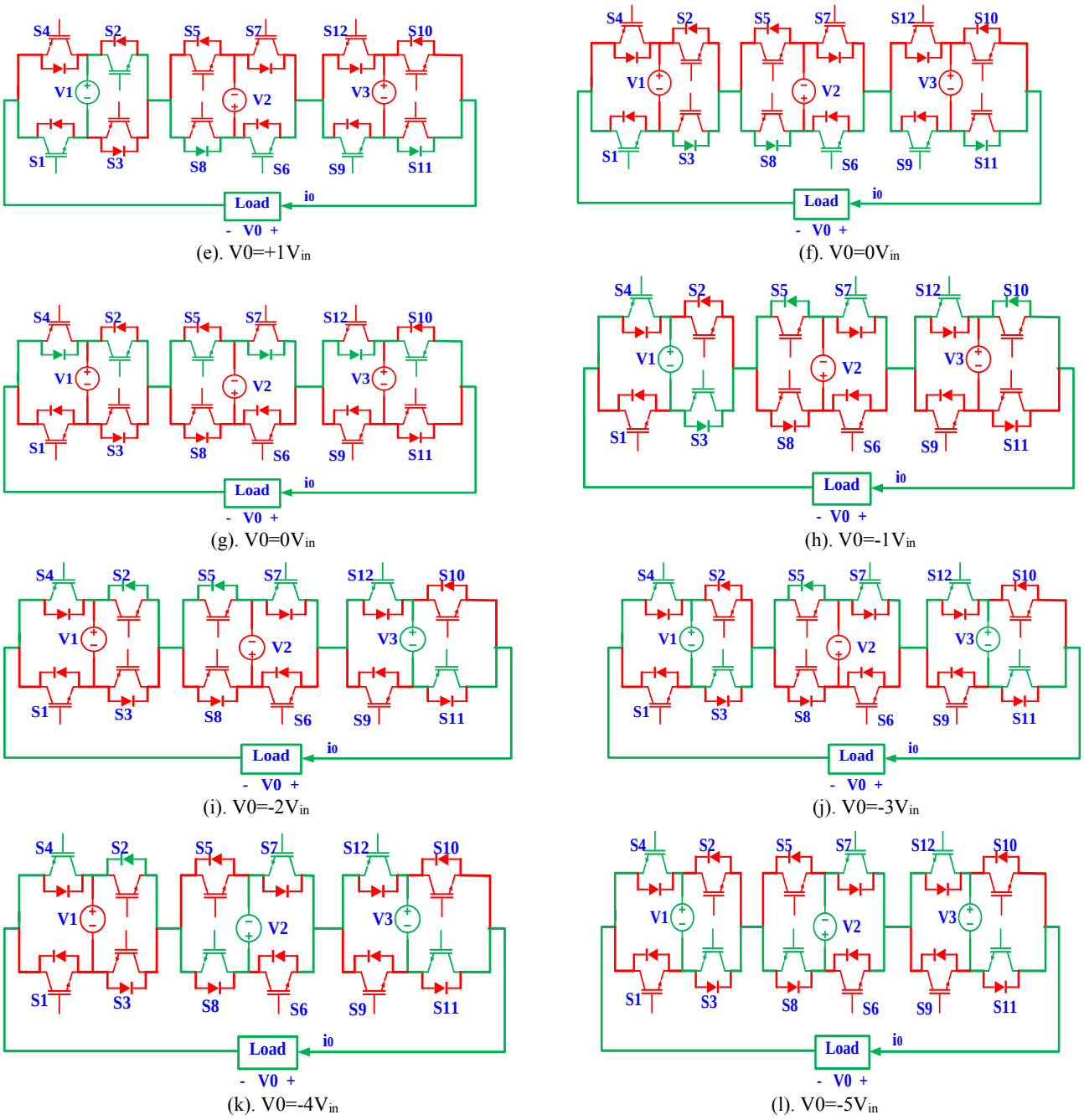
(b). $V0=+4V_{in}$



(c). $V0=+3V_{in}$



(d). $V0=+2V_{in}$



(e). V0=+1V_{in} (f). V0=0V_{in}

(g). V0=0V_{in} (h). V0=-1V_{in}

(i). V0=-2V_{in} (j). V0=-3V_{in}

(k). V0=-4V_{in} (l). V0=-5V_{in}

Fig. 3: Operating Modes of Topology

±5V_{in}: To Provide $+5V_{in}$ as output Voltage, S_1, S_2, S_5, S_6, S_9, and S_{10} create conduction path to link the source with load as depicted in Figure 3(a). In the same fashion $-5V_{in}$ appears across the load by turning on switches S_3, S_4, S_7, S_8, S_{11}, and S_{12} respectively as illustrated in Figure 3(l).

±4V_{in}: As illustrated in Figure 3(b), using the conductivity of devices S_1, S_3, S_5, S_6, S_9 and S_{10} load is connected to source and $+4V_{in}$ appears across load. To provide $-4V_{in}$ across the load, S_2, S_4, S_7, S_8, S_{11}, and S_{12} switches conduct and load is in series with the source as shown in Figure 3(k).

±3V_{in}: S_1, S_2, S_5, S_6, S_9 and S_{11} conduct as shown in Figure 3(c) to produce $+3V_{in}$ as the output voltage level. Utilizing switching devices S_3, S_4, S_7, S_8, S_{10}, and S_{12} conduction in the order depicted in Figure 3(j) to achieve an output voltage level of $-3V_{in}$.

±2V_{in}: To obtain $+2V_{in}$ as the output voltage level, the switch's respective conduction is depicted in Figure 3(d) and Table 1. Conduction of the switches is shown in Figure 3(i) to produce $-2V_{in}$ as the voltage level.

±1V_{in}: Switches operate in the manner shown in Figure 3(e) & mentioned in Table 1 to produce

$+1V_{in}$ as voltage level. To get $-1V_{in}$ as voltage level, the path of conduction is given in Figure 3(h).

$0V_{in}$: To achieve null output voltage level in this mode of operation, either S_1, S_3, S_6, S_8, S_9, and S_{11} conduct or S_2, S_4, S_5, S_7, S_{10}, and S_{12} conduct, as shown in Figure 3 (f&g) respectively.

Table 1. Switching Modes

Switching State	Output Voltage
S_1-S_2-S_5-S_6-S_9-S_{10}	$+5V_{in}$
S_1-S_3-S_5-S_6-S_9-S_{10}	$+4V_{in}$
S_1-S_2-S_5-S_6-S_9-S_{11}	$+3V_{in}$
S_1-S_3-S_6-S_8-S_9-S_{10}	$+2V_{in}$
S_1-S_2-S_6-S_8-S_9-S_{11}	$+1V_{in}$
S_1-S_3-S_6-S_8-S_9-S_{11}	$0V_{in}$
S_3-S_4-S_5-S_7-S_{10}-S_{12}	$-1V_{in}$
S_2-S_4-S_7-S_8-S_{10}-S_{12}	$-2V_{in}$
S_3-S_4-S_7-S_8-S_{10}-S_{12}	$-3V_{in}$
S_2-S_4-S_7-S_8-S_{11}-S_{12}	$-4V_{in}$
S_3-S_4-S_7-S_8-S_{11}-S_{12}	$-5V_{in}$

2.2 Proposed Hybrid PWM

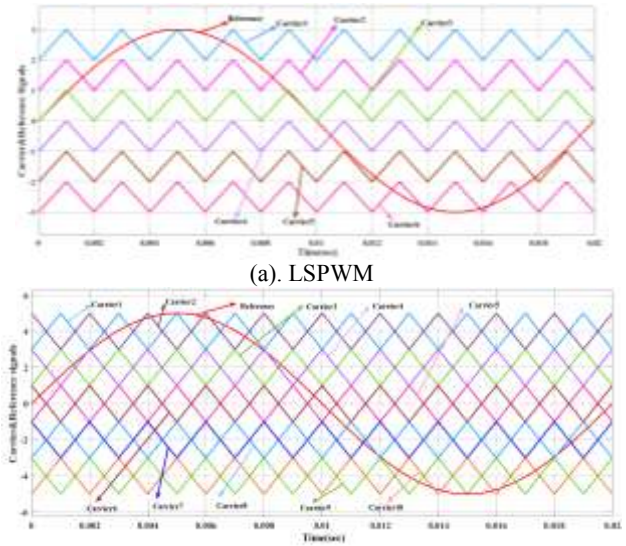
Figure 4 indicates the LSPWM scheme and proposed PLSPWM scheme. For both the cases reference wave amplitude and frequency are A_{ref} and f_{ref} respectively. Since it is an eleven-level inverter, it demands ten carriers and one reference to send gating pulses to switches. For LSPWM modulation index (m_a) is represented as

$$m_a = \frac{A_{ref}}{A_{carrier}} \tag{1}$$

where A_{ref} and $A_{carrier}$ are amplitudes of reference and carrier respectively. In LSPWM, ten carriers formed by keeping an equal magnitude of $A_{carrier}$ with each other and level shifted. Like LSPWM, for PLSPWM the magnitude of the output is decided by using modulation index (m_a), which is indicated as

$$m_a = \frac{A_{ref}}{B_{carrier}} \tag{2}$$

where $B_{carrier}$ is carrier amplitude. For instance, Cr_1, Cr_2, Cr_3, Cr_4 magnitudes lies between ($3B_{carrier}$-$5B_{carrier}$), ($5B_{carrier}$-$3B_{carrier}$), ($B_{carrier}$-$3B_{carrier}$), ($3B_{carrier}$-$B_{carrier}$) respectively. In the same fashion other carriers are arranged as indicated in Figure 4(b). For the PLSPWM case, all the carriers are maintaining equal magnitude and they are phase shifted by π radians. Therefore, this method is level as well as phase shifted. By utilizing the advantages of both LSPWM and PSPWM switching losses will be reduced and %THD becomes minimal.



(a). LSPWM

(b). PLSPWM

Fig. 4: PLSPWM technique of eleven-level inverter

Gating pulses are formed in this modulation scheme employing the comparison of reference waves to carrier waves. Ten pulses are developed after the comparison. Employing the logic provided in Table 1, these ten pulses generate signals to switches (S_1-S_{12}) shown in Figure 5.

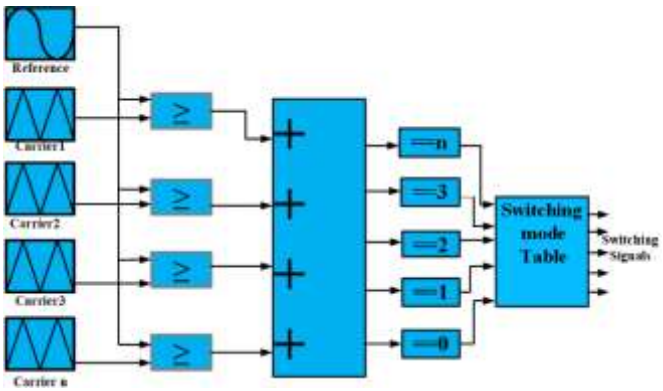


Fig. 5: Switching Logic implementation

The peak value of the reference wave can be altered to modify the magnitude of the modulation index (m_a). The reference wave along with output waves perform at the identical fundamental frequency (50Hz). Frequency modulation can differ through modification of the carrier frequency. If carrier frequency($f_{carrier}$) rises, the harmonic shifts to a greater order, lowering the size of the filter. Higher carrier frequency($f_{carrier}$), leads to a raise of switching losses. As an outcome, the carrier frequency is restricted to certain standards, and the carrier frequency(*carrier*) of this topology is confined to 4kHz.

3 Voltage Stress and Loss Analysis

3.1 Voltage Stress

The peak voltage stress of switching devices related to sources (V_2 &V_3) have identical values and relating to source(V_1) are different for this configuration. The maximum voltage stress of switches is shown in equations (3), (4), and (5).

$$V_{S_1} = V_{S_2} = V_{S_3} = V_{S_4} = V_1 = V_{in} \quad (3)$$

$$V_{S_5} = V_{S_6} = V_{S_7} = V_{S_8} = V_2 = 2V_{in} \quad (4)$$

$$V_{S_9} = V_{S_{10}} = V_{S_{11}} = V_{S_{12}} = V_3 = 2V_{in} \quad (5)$$

Where V_{Sn} corresponds to the maximum voltage stress of devices when it is a turn-off. For the suggested configuration, the total standing voltage (*TSV*) is represented as (6).

$$TSV = 4*\left(V_{S_1} + V_{S_5} + V_{S_9}\right) = 20V_{in} \quad (6)$$

The proportion of the sum of switch turn-off voltages to peak voltage seems through the load is *TSV* (p.u.). It is 4p.u. in the present state for the proposed topology. Figure 6 portrays a bar chart demonstrating the voltage stress of individual switching devices at various levels. According to Table 1, for the $+5V_{in}$ level, the switches S_1, S_2, S_5, S_6, S_9, and S_{10} are conducting, while the others are non-conducting. As shown in Figure 6, the voltage stress of S_1, S_2, S_3 and S_4 are V_{in}, S_5, S_6, S_7 and S_8 are $2V_{in}$ and S_9, S_{10}, S_{11} and S_{12} are $3V_{in}$ respectively.

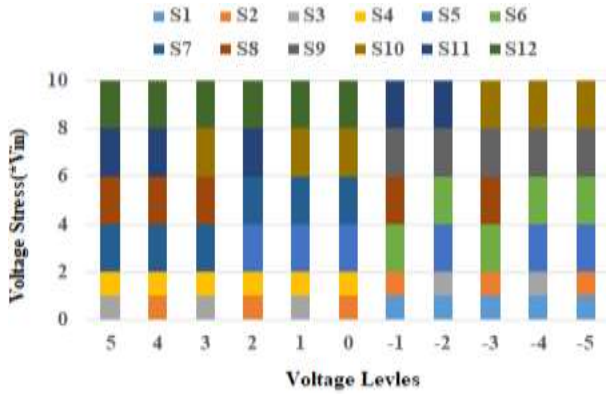


Fig. 6: Bar chart representation of voltage stress

3.2 Loss Analysis

Switching and conduction losses are distinct classifications of power losses experienced by switching devices. Conduction losses are brought on by on-state resistance while switching losses are a result of delays in the switch's on/off processes. It is possible to express the switching loss during the turn-on process as

$$P_{swlturnon}(i) = f_{carrier}\int_0^{t_{on}} v(t).i(t)dt = \frac{1}{6} f_{carrier} * V_{sw,i} * i_{on,i} * t_{on} \quad (7)$$

$$P_{swlturnoff}(i) = f_{carrier}\int_0^{t_{off}} v(t).i(t)dt = \frac{1}{6} f_{carrier} * V_{sw,i} * i_{off,i} * t_{off} \quad (8)$$

In this case, $P_{swlturnon}$ *(i)*, $P_{swltunoff}$*(i)* and V_{sw} stand for the ith switch's turn on, turn off a loss, and off-state switching voltage respectively. Currents during the switch's on- and off-states, respectively, are called I_{on} and I_{off}. In terms of the number of switches on (N_{swon}) and the number of switches off (N_{swoff}), the relationship between carrier frequency ($f_{carrier}$) and modulating frequency (f_m) is

$$N_{swon} = N_{swoff} = \frac{f_{carrier}}{f_m} \quad (9)$$

Total switching losses (P_{sw}) are calculated by summing turn-on and turn-off losses.

$$P_{sw}(Total) = \sum_{i=1}^{N_{sw}}\left(\sum_{j=1}^{N_{on}(i)} P_{swlon}(ij) + \sum_{j=1}^{N_{off}(i)} P_{swloff}(ij)\right) \quad (10)$$

where N_{sw} is the total number of switches of the proposed MLI.

Conduction losses are appeared in a switch during the conduction period due to on-state resistance and voltage drop across the switch. Generalized equation for conduction losses of diode and switch as follows:

$$P_{Dcon} = V_{Don} * i_{Davg} + R_{Don} * i^2_{Drms} \quad (11)$$

$$P_{swcon} = V_{swon} * i_{swavg} + R_{swon} * i^2_{swrms} \quad (12)$$

where P_{Dcon} and P_{swcon} are diode and switch conduction losses, V_{don} and V_{swon} are on-state voltage drops of diode and switch respectively. R_{Don} and R_{swon} are on-state resistances of the diode and switch, i_{Davg}, i_{swavg}, i_{Drms}, and i_{swrms} are average and RMS currents of the switch respectively.

4 Comparison

Table 2 contrasts the proposed topology with distinct new eleven-level configurations. The

comparison aspects are the number of switches, drivers, diodes, capacitors required, DC sources, applied PWM method, operating value of carrier frequency, and type of configuration. In [13], the authors utilize asymmetric configuration with fewer switch counts, requires four sources and operating PWM method is Nearest level modulation (NLM).

Table 2. Comparison with recent topologies

Components	[13]	[16]	[22]	[14]	Proposed
No. of Switches	10	12	8	12	12
No. of Drivers	10	12	8	12	12
No. of Diodes	Nill	Nill	Nill	Nill	Nill
No. of Sources	4	6	3	5	3
No. of Capacitors	Nill	Nill	3	Nill	Nill
PWM method	NLM	LSPWM	NLM	LSPWM	PLSPWM
Carrier Frequency	50Hz	1KHz	50Hz	5KHz	1KHz
Configuration	Asymmetric	Symmetric	Asymmetric	Symmetric	Asymmetric

In [16], authors employ an identical number of switches and the same carrier frequency as proposed topology however it is a symmetric configuration, requires six sources and the operation scheme is Level Shifted Pulse Width Modulation (LSPWM). In [22], authors use a symmetric configuration, a minimal number of switches contrasted to the proposed topology but it requires capacitors. So, voltage balancing plays a vital role in the design of configuration. In [14], it requires the same switch count in contrast to the proposed topology but the sources count is a more and symmetric configuration.

Taking all aspects into consideration, the proposed topology demands only a few components, DC sources, and works well. It exhibits that the proposed topology yields sophisticated results.

Table 3. Simulating Parameters

Component	Values
Input Sources	100V,200V,200V
Loading Scenarios	50 Ω, (100-200mH)
Frequencies	Reference-50HZ, Carrier-1KHz

5 Results and Discussions

5.1 Simulation Results

MATLAB/Simulink is utilized for simulating the execution of an eleven-level operation. Table 3 demonstrates the source voltages for eleven levels categorized as 100V, 200V, and 200V respectively. The load variables in this instance are 50 Ω for resistance and 100mH for inductance. The frequency at which it operates of the suggested inverter is the fundamental frequency(50Hz). The functioning of the inverter according to R-load can be seen in Figure 7. The output current seems to be correlated to the output voltage. Figure 8 represents the inverter's outcomes for eleven-level operations depending on various load situations.

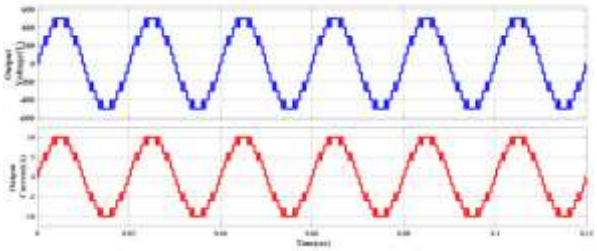


Fig. 7: Waveforms for R-Load

Figure 8 indicates that output voltage remains constant regardless of loading conditions, but current is null during unloading, implying voltage for Resistive loads and delays for inductive loads. Figure 9 depicts variations of waveforms related to inductive load fluctuations. Figure 9 shows that as inductance increases, the current falls due to high inductive load leading to more lagging of current.

Figure 10 presents the resultant voltage as well as current as the modulation index (m_a) alterations. Figure 10 shows that ten carriers are contrasted to one reference for 1,0.9 values, yet the size of the waveform reduces for the 0.9 value. Similarly, for the 0.7 value waveform level is lowered and changed to nine-level. For 0.6 and 0.4 values it functions as a nine-level and five-level respectively. Comparably for a 0.2 value, it is working as a three-level via contrast of two carriers to reference.

Figure 11 represents the resulting waveforms as the reference frequency fluctuates. According to Figure 11, enhancing the reference frequency leads to a rise in load inductance. Since incremental load inductance impacts total load impedance, load current falls as reference frequency goes up. The

proposed topology appears to be suitable for high-frequency performing appliances.

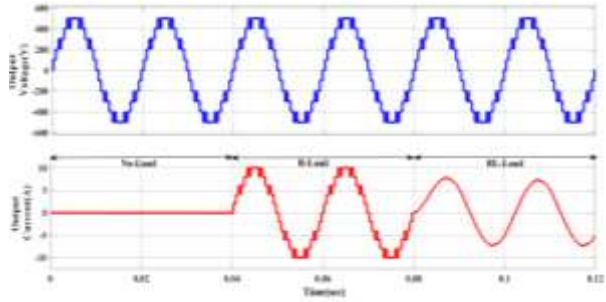


Fig. 8: Waveforms for various Load situations

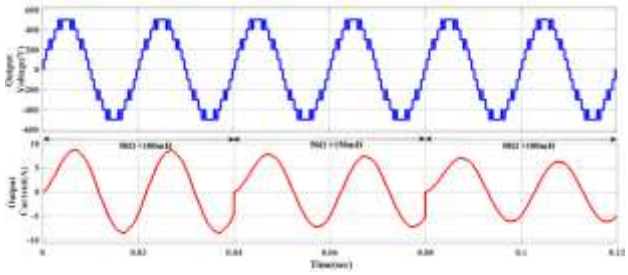


Fig. 9: Waveforms for distinct RL-Loads

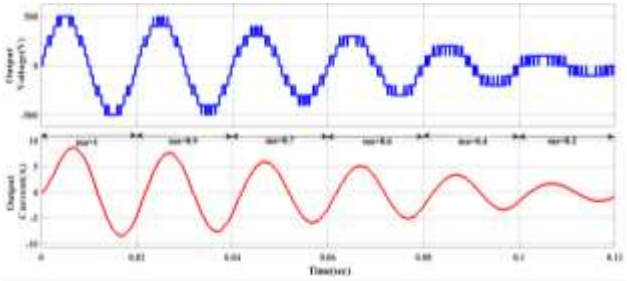


Fig. 10: Resulting waveforms for alteration of modulation index

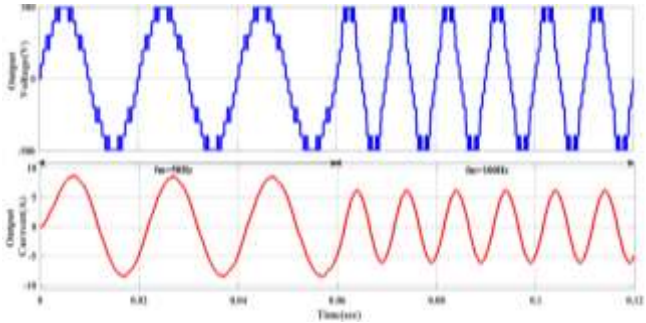


Fig. 11: Load waveforms for fluctuation in reference frequency

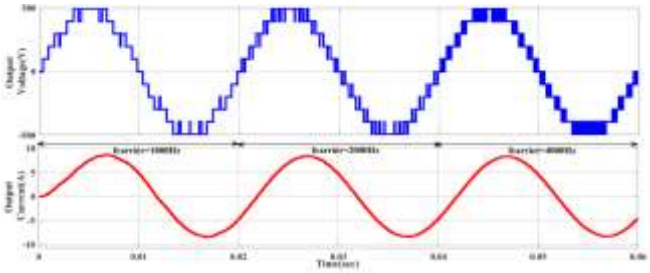


Fig. 12: Load waveforms for carrier frequency alterations

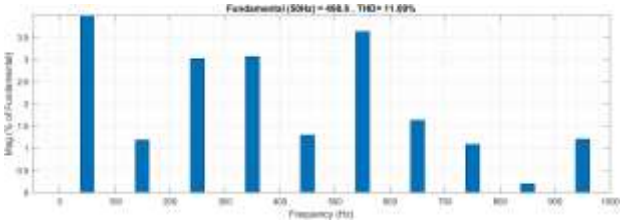


Fig. 13: %THD of resultant Voltage

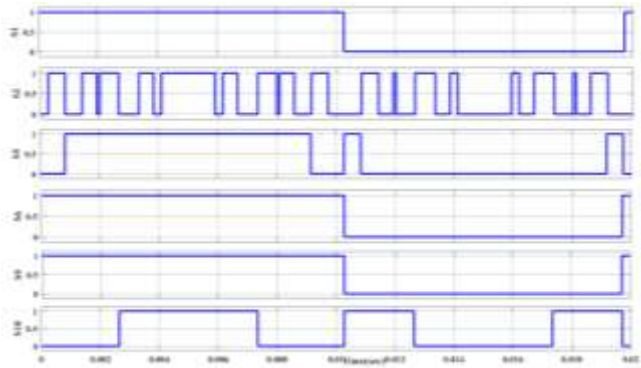


Fig. 14: Switching pattern of devices

Figure 12 depicts load waveforms as the carrier frequency alterations. The pulses count for individual level boosts as a carrier frequency($f_{carrier}$) rises. Consequently, the harmonics shift upwards in order and the size of the filter is reduced. As the carrier frequency ($f_{carrier}$) expands, switching losses elevate due to an increase in pulses count for each voltage level.

Figure 13 shows eleven-level inverter's resultant voltage THD is 11.09% and the fundamental output of 498.8 volts. Table 4 displays the variation of the modulation index related to THD (%) along with fundamental output. Employing PLSPWM scheme %THD is diminished. The switching sequences of devices (S_1, S_2, S_5, S_6, S_9 and S_{10}) are depicted in Figure 14, and the rest are in complementary mode. Figure15 represents the voltage pattern of three bridges. In accordance with the simulation outcome, the suggested inverter works for all conditions of load.

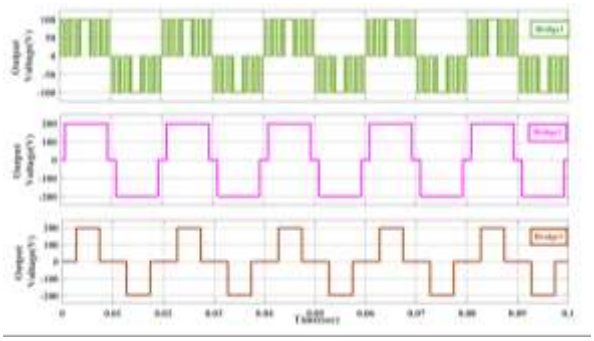
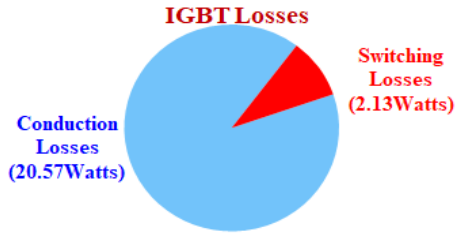


Fig. 15: Voltage across three bridges

Table 4. THD analysis for variation in modulation index

Modulation Index(m_a)	Fundamental Voltage(V)	THD (%)
1	498.8	11.09
0.9	447.8	12.63
0.7	346.3	17.15
0.6	298.4	17.42



(a). IGBT Losses

(b). Diode Losses

Fig. 16: Switching losses

5.2 Thermal Modelling

The objective of the PLECS software is to thermally model devices as per the proposed topology. Figure 16(a) and Figure 16(b) display the percentage of losses of IGBT and Diode considering inductive load respectively. The efficiency of the system is estimated by using just R loads and shown in relation to the output power (0-2000W). As illustrated in Figure 17, the effectiveness ranges from 98.2% to 96.5%. Since the load rises, the efficiency reduces. Since demand grows, conduction losses increase, causing temperatures to rise and efficiency to decrease. Utilizing PLSPWM power converter efficiency is improved and power losses of individual switches is minimized.

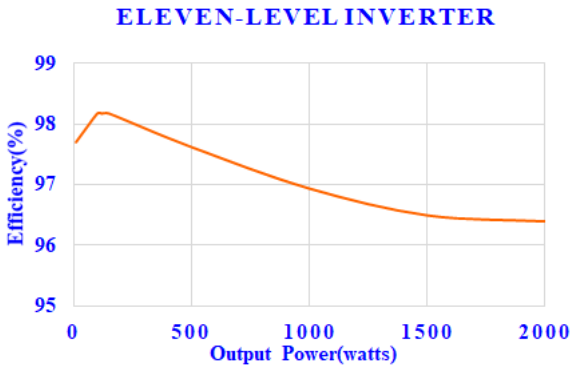


Fig. 17: Efficiency curve

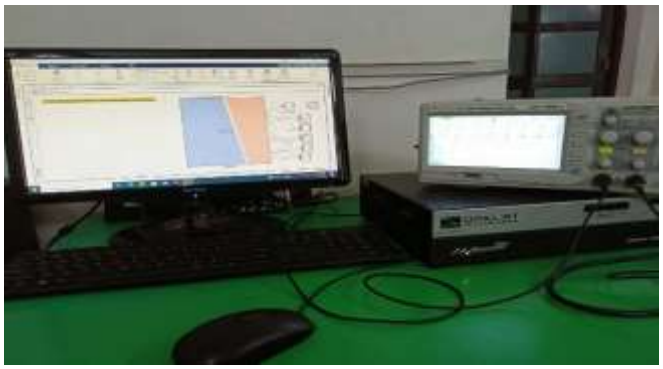


Fig. 18: OPAL-RT Test Bench

5.3 OPAL-RT Platform

Real-time simulations serve as vital to developing and evaluating system performance and certainty since they operate at the identical evaluate as systems in the real world. The OPAL-RT simulator interacts with the Sim Power System in MATLAB/Simulink using the RT-LAB software. The OP4510 pertains to the OPAL-RT RT-LAB and eFPGAsim real-time platforms, in addition to sophisticated Intel processors along with FPGA chips. This multi-rate FPGA-based design enables consumers to design power converters for the HIL program using limited time steps of less than seven seconds for INTEL CPU-based sections for a period of a smaller nanosecond on the FPGA chip. The OP4510 is also suitable for use as a standalone electronic test system with pre-programmed models. The eleven-level configuration is executed by OP4510 as indicated in Figure 18 and represented in this section.

Figure 19 and Figure 20 display waveforms for load impedance as 50 Ω and 50 Ω +100mH for a carrier frequency of 1kHz. Figure 19 shows output current appears like output voltage and Figure 20 shows that output current delays for inductive load respectively.

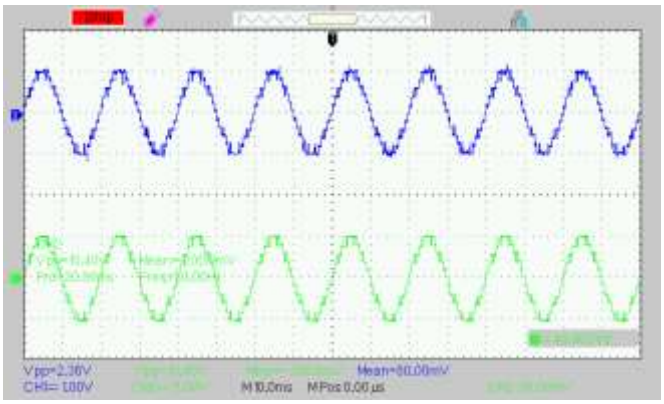


Fig. 19: Output waveforms for Resistive load

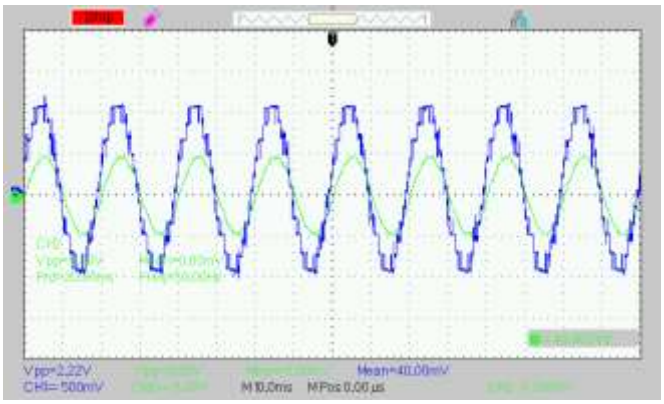


Fig. 20: Output waveforms for RL- load

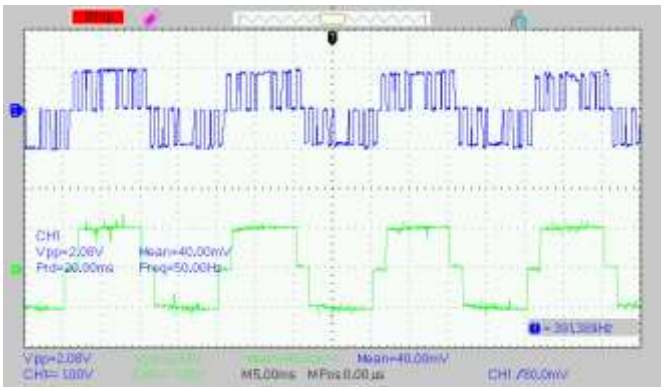


Fig. 21: Output Voltage of Bridge1&2

Figure 21 and Figure 22 depicts the voltage across the three bridges. Voltage across bridge 1,2&3 is like results obtained from simulation results. It appears that real-time simulated outcomes are comparable to MATLAB/Simulink simulated results. Figure 23 indicates the pulses of all the devices. All these real-time results show that the proposed topology performs well suitable for all loading conditions corresponding to the proposed modulation technique, despite the need for additional regulation methods. After observing simulated, thermal modeling and real time implementation outcomes shows that the proposed hybrid PWM improves efficiency by minimizing losses.

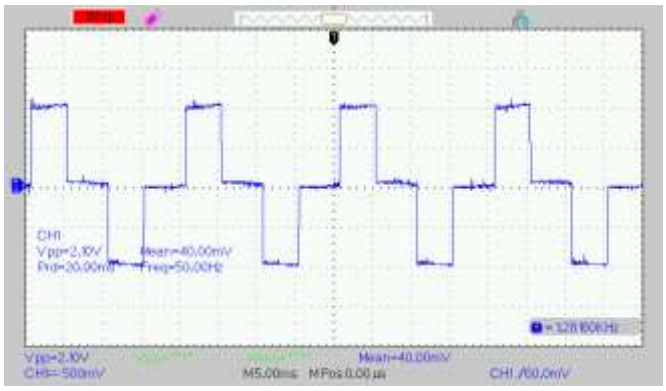
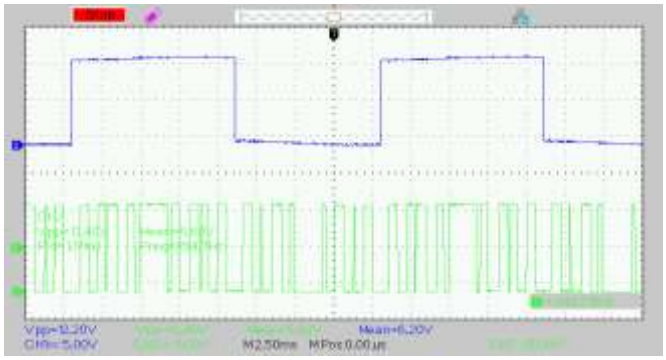
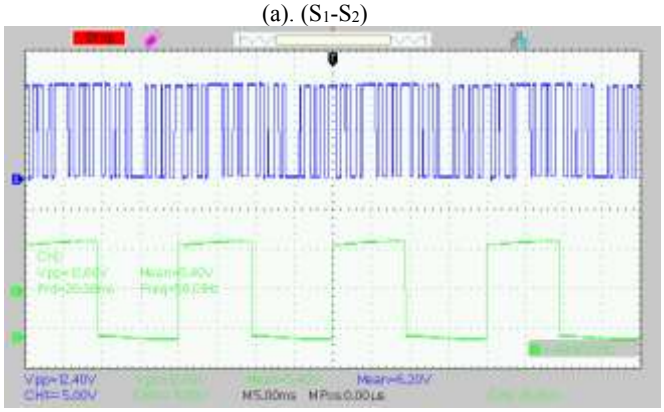


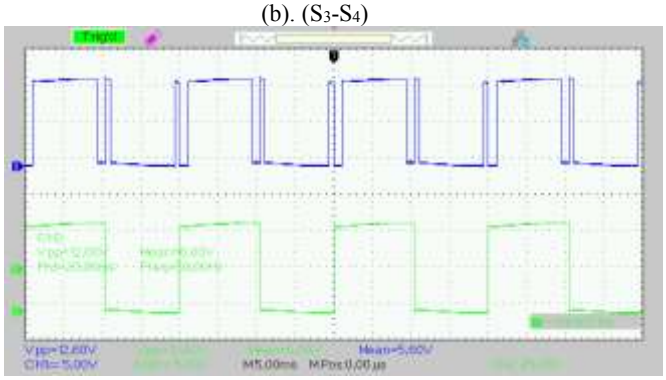
Fig. 22: Output Voltage of Bridge3



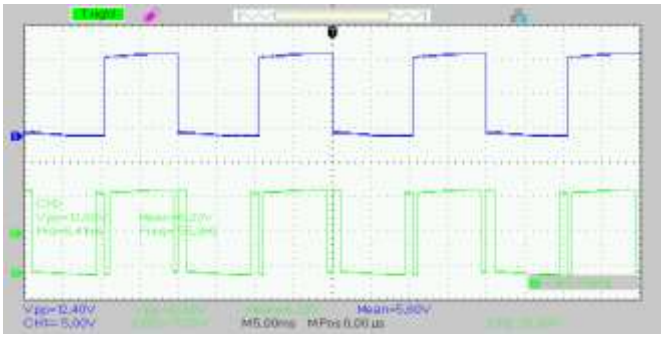
(a). (S_1-S_2)



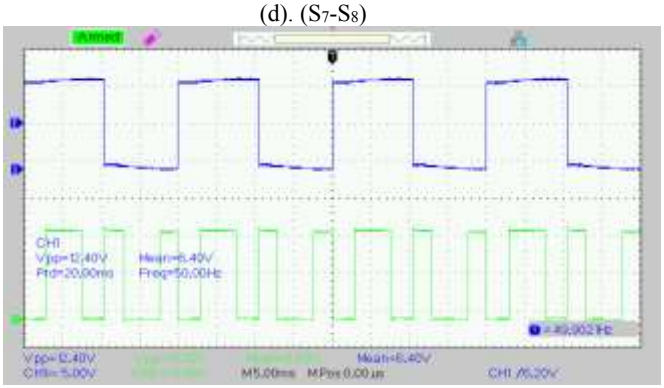
(b). (S_3-S_4)



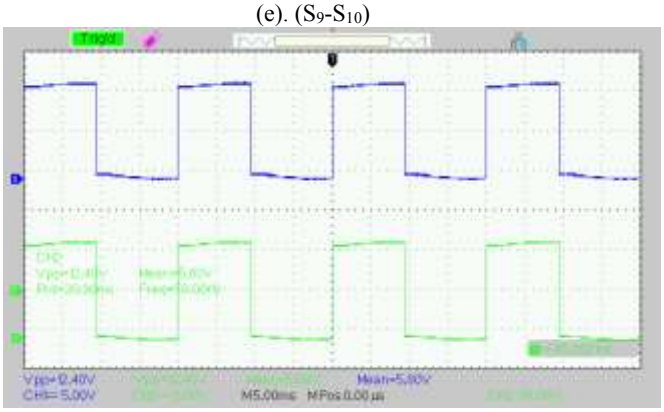
(c). (S_5-S_6)



(d). (S_7-S_8)



(e). (S_9-S_{10})



(f). (S_{11}-S_{12})

Fig. 23: Switching Patterns

6 Conclusion

The present work discusses a new eleven-level inverter with a hybrid PWM technique. The above configuration is simulated in MATLAB/Simulink employing various situations such as load, source voltage, modulation index, reference frequency, and carrier frequency variations. Consequently, the proposed configuration is appropriate for all loading facilities. This proposed design is compared to other topologies in the literature to determine its superior features. The proposed topology employs the fewest switches and components while maintaining an acceptable TSV (p.u.). The overall performance of this configuration is also determined by estimating switch losses with the PLECS software. The most efficient level was determined to be 98.2%. Finally, the successful execution of the configuration is evaluated using the OPAL-RT Test bench, and results are provided. The results suggest that the proposed configuration is efficient. Employing hybrid PWM losses are minimized with improvised efficiency therefore it is preferable for medium voltage applications.

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Conflict of Interest

The authors have no conflicts of interest to declare.