A New Embedded Clock Gating Technique in 8- bit Synchronous Counter with Reduced Switching Activity for Clock Divider Circuit

D. S. SHYLU SAM[1], P. SAM PAUL[2], JOEL SAMUEL[1], VIMUKTH JOHN[1]
[1]Division of ECE,
Karunya Institute of Technology & Sciences,
INDIA

[2]Division of Mechanical Engineering.
Karunya Institute of Technology & Sciences,
INDIA

Abstract: - Counters play an inevitable role in many VLSI circuits such as timers, frequency dividers, memories, and ADC/DAC. Integrating the timing discriminator, Pulse Swallow, and Correlated double sampling are various approaches used in counters for low power consumption. The main objective was to minimize the power consumption and device count. In this work, a new embedded clock gating technique is used in an 8-bit counter to reduce the switching activity. A clock gating circuit and clock buffer network pattern are used in the proposed algorithm to reduce the power consumption of synchronous counters. The proposed counter reduced the unwanted clock activity of all T FFs and noise is reduced to a greater extent thereby reducing the power and the device count. CMOS 45nm technology is used for designing the proposed counter 1.5 supply voltage. Simulated results show the improvement of the proposed approach over other conventional counters in terms of power consumption and device count.

Key-Words: - Synchronous Counters, Embedded clock gating, Reduced device count, Low Power Consumption,45nm CMOS,8-bit Synchronous Counter.

Received: February 8, 2023. Revised: November 19, 2023. Accepted: December 23, 2023. Published: December 31, 2023.

1 Introduction

Synchronization is required to activate all stages simultaneously in a circuit. The authors in, [1], used embedded clock gating in a carry propagation circuit to minimize the switching power and silicon area of their CMOS synchronous counter compared with conventional synchronous counters. A novel pipeline partitioning method was reported in, [2], [3], [4], to improve the speed of digital parallel counters. It has a counting path and state look ahead path and three modules namely the first module to generate the counting states, D type FFs module, and 2-bit counters module. A power-efficient binary counter, [5], [6], [7], [8] and the up-down counter are designed in the reported works. In this work, power consumption in clock distribution is controlled by a novel combinational logic at the input of all FFs. The correlated double sampling (CDS) method, [9], was used to reduce the toggling operation in D FF. Thereby, power consumption is reduced, image quality degradation due to self-heating, and voltage drops in power rails can be reduced in CMOS image sensor (CIS) applications for the CDS counter, [10], [11], [12].

A low-power pulse swallow counter is simulated in 180nm technology, [13]. It consists of a divide by 2/3 pre-scaler, a programmable counter to work in high frequency to reduce power consumption, and a swallow counter, [14], [15], [16], [17]. The programmable counter is designed to work in different frequencies. Quantum dot cellular automata (QCA) for synchronous counters are implemented in, [18]. There are two types of QCA namely 45^{o} cells and 90^{o} cells. A level-sensitive innovative idea with majority and inverter gates is designed for QCA in, [19], [20], [21], [22] and then it is converted from an edge-level converter for the counters to reduce power consumption. A colter counter that works on potential change detection, [23], [24], is designed using Microcells/particles are passed through a sensing channel to obtain the potential change principle. Sensor arrays are required to obtain high throughput in colter counter, [25], [26], [27]. Counter-current chromatography works with 2D and 3D models in helical columns and provides better phase mixing, [28]. Rather than the spiral column, the helical column gives centrifugal force and helps in the optimized design of helical columns, [29]. Scintillation counters along with comparator and multi-vibrator act as a precise time discriminator. A normalized value of input is applied at the zero crossing point rather than a dynamic wide range of input to increase the precision of the scintillating counters, [30]. A synchronous control over the speed of rotors is analyzed by cross-coupling and electromechanical dynamic coupling model. A correlated double sampling (CDS) approach was used in the parallel column of counters. Two's complement arithmetic with 16 transistors is used and obtained a 34% reduction in power consumption and a 2.4 times improvement in the speed of the counter, [31]. Deterministic algorithms with fast state-optimal characteristics are designed for synchronous counting. The propositional satisfiability (SAT) problems are solved by either time-optimal algorithms or non-optimal algorithms. A low-power parallel sampling technique that achieves delay resolution for counter-assisted PLL is implemented. In this, a 2-bit asynchronous counter and a 6-bit synchronous counter are combined to form a hybrid counter to operate at high speed above 4GHz frequency, [32], [33]. CMOS analog counter with the programmable input voltage to produce proportional output concerning input phase is designed, for SPAD pixel arrays. It used a high-resolution avalanche photodiode for image sensors to obtain a factor 3 improvement over the previous designs. Quantum synchronous counters (QSC) with direct mapping flip-flop designs and Quantum dot cellular automata (QCA) inherent characteristics are combined to overcome long wire and area-related constraints and to improve cost function and delay in QCA. Exponential smoothing and counter-based algorithms are combined to form counter synchronization (C- Sync) in changing neighboring conditions in wireless sensor networks (WSN). Synchronization leads to the reduction in the duty cycle thereby reducing energy consumption in WSN. A pre-amplifier with 12 channels is designed in ASIC for gas counters and avalanche photodiodes. Gain and Equivalent low optimum noise charge (ENC) are analyzed for the pre-amplifier. An observation of the literature works reveals the scope for improvement in the architecture of synchronous counter. In this work, a modified clock buffer network is proposed for 8-bit synchronous counter. The novelty lies in the embedded clock gating circuit which is distributed from the master clock to T FF to enable one TFF and to get the count. The clock buffer network is changed suitably to eliminate the unwanted activity of all FFS all the time in the counter operation, remove noise in the clock edges of the master clock, and thereby obtain substantial improvement in power, device count, and circuit complexity for the synchronous counter. CMOS 45nm technology is used for designing the 8-bit counter and simulated results show promising results for the proposed approaches.

The rest of this paper is organized as follows: Section 2 deals with various conventional methods for counter design. Section 3 illustrates the proposed methodology for the 8-bit synchronous counter. Section 4 describes the simulated results obtained for the proposed 8-bit counter and the comparison with other works. Section 6 concludes the work done.

2 Conventional Synchronous Counters

2.1 Clock Gating Embedded into Carry Propagation Circuit

The circuit diagram of Clock Gating embedded into the Carry Propagation Circuit is shown in Figure 1 A 16-bit synchronous counter is designed with 16 FFs and 4 local clock generators. It works on the synchronous timing principle and conditional pulse. At each stage output of FF is given to the local clock generator and its output is inverted and fed to the input of FF for toggling operation. The 16-bit synchronous counter is obtained by four sub-blocks where each sub-block has 4 FFs and one local clock generator to maintain the speed and decrease the number of pass transistors required in the design. The speed of the counter decreases if more than five pass transistors are used in each sub-block. The clock gating counter is also compared with conventional non-clock gated counters and conventional clock gated counters where the device count decreased by 15% and power consumption is 64% by embedding the clock gating in a carry propagation circuit. Redundant transitions are reduced in this method by decreasing the number of transistors in the design.

The Clock Cycle Time (T_{CYCLE}) of Clock Gating embedded into Carry
Propagation Circuit synchronous counter is:

$$T_{CYCLE} \geq T_{D\_MAX} + T_{P\_MIN} + T_{CQ\_MAX} \quad (1)$$

T_{D_MAX} is the worst-case propagation delay,
T_{CQ_MAX} is the worst-case clock storage elements

clock to output delay and T_{P_MIN} is the minimum pulse width.

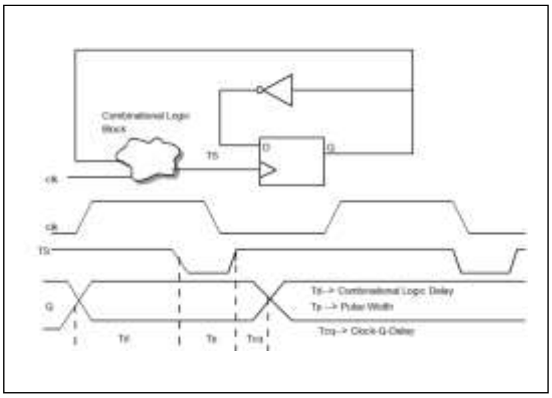


Fig. 1: Conditional pulse-based synchronous timing principle

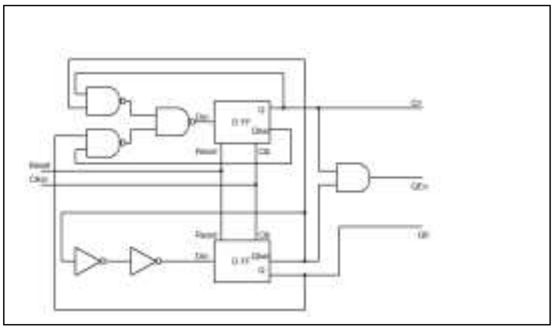


Fig. 2 Hardware schematic – Counting Path

2.2 State Look-Ahead based Digital Parallel Counter

Counting operations are done by the logic in the counting path as shown in Figure 2 and the look-ahead path generates future states and prepares the counting path for future counting. Decoders in the look-ahead path initiate the early overflow and state look-ahead logic is responsible for pipelining the early overflow detection. The state equation for the counter is derived from the early overflow pipelining equation.

The maximum allowable m-bit counter size (CS) is given by:

$$CS = m + (2*(2m-1)) \tag{2}$$

The number of early overflow (EO) states is:

$$EO = 2^m - 1 \tag{3}$$

The clock period (T_{CLKIN}) of 8 bit parallel counter with a counting path and the look-ahead path is given by:

$$T_{CLKIN} > T_M + T_{AND} + T_{setup\text{-}hold} \tag{4}$$

Where T_M is the module access time, T_{AND} is the delay of AND gate and $T_{setup\text{-}hold}$ is the DFF setup time plus hold time. Pipelined counting path and state look-ahead path concurrently activate all modules and provide all counting states without rippling effects. The design avoids long chain detectors for larger-width parallel counters. An increase in fan-out leads to a drop in counter frequency at the rate of $\log_{6.5}N$ where N is the width of the parallel counter. The drop in the logarithmic frequency makes the parallel counter a faster counter. However, the area requirements and power requirements increase for each doubling of the clock frequency. In this design clock frequency is made independent of the width of the counter, thereby all modules are activated simultaneously by the clock frequency. The parallel counter has three modules separated by D FFs. The counter output is in radix-2 representation and can be read without any decoding process. The counter design does not have any count latency as in other normal counters.

2.3 Clock Gating Cascaded T Flip-flop Synchronous Counter

A cascaded T FF arrangement which concentrates on the next state output is designed. Power contribution is controlled by properly designing the excitation of T FF. Thereby power consumption during transitions of T FF output can be controlled. A clock buffer network with several repeaters provides the master clock to all T FFs. This not only distributes the clock to all T FFs in the arrangement but also controls the clock skew. The clock buffer network has threefold advantages namely decreasing the load on the master clock, the number of buffer levels is reduced and power dissipation is minimized. By placing an additional clock gating circuit consisting of OR gates, the logic is extended for the up-down counter. The design can also be extended to the digital block of successive approximation register type ADC.

The clock activation and input for T FF for the up-down arrangement are given below.

$$Clk_n = T_n.\ (Q_{n-1} + Q_{n-1}') \tag{5}$$

$$T_n = UP \prod Q_i + DOWN' \prod Q_j' \tag{6}$$

2.4 Correlated Double Sampling (CDS) Low Power Counter

The counter is proposed by D FF (master and slave). The output of master INT toggles in the conventional counter whereas in the CDS counter by using an AND gate and pulse generator, the togging operation is controlled. This technique reduces the power consumption by 50%. Multiplexers are used to provide up-down counting operations. Edge triggering is followed for D FFs in CDS low power counter for CMOS image sensor (CIS) applications. The single slope in Column-Parallel ADC provides digital CDS operation. The non-uniformities of CIS pixels and ADC lead to fixed pattern noise and can be reduced by the digitally correlated double sampling method.

A detailed investigation of counter obligates before considering the power reduction. This survey gives way to a deeper perspective of various approaches to cope with power advancements in the fields. The counter investigation mandates the following parametric requirements that arise to be factors of consideration in various Problems related to counters as discussed below in Table 1. Evolutionary approaches such as correlated double sampling and look-ahead path in addition to counting path are used for counters in circuit complexity problems. However, the power consumption is very large in those approaches compared with other algorithms. In our work, an improved clock gating and clock buffer network from the master clock is proposed and simulated using CMOS 180nm technology. In this design, a 3-level buffer network is proposed to distribute the clock for each T FF stage in an 8-bit counter. These methods save more power than the other conventional schemes without clock gating.

3 Proposed Method

In this work, a cascaded structure of T FFs for the core functionality of the counter is proposed. Transmission gate FFs are used in the design. A control transistor and AND gate work as an efficient combinational circuit for clock gating of the FFS in the proposed synchronous counter to obtain a substantial gain in power consumption. In conventional counters, D FFs are used to latch the input state to the output state. But, in the proposed counter T FF concentrates on the activity of the next state output. Power consumption occurs at both T=0 and T=1 transitions of the T FF in which the power consumption of T FF at T=0 is eliminated by properly designing the characteristic function of T FF. This controls the clock of the counter and hence reduces the power consumption. As the switching activity is reduced the power consumption is reduced to a greater extent. T FF is a preferred choice in synchronous counters. This combinational circuit with a control transistor and AND gate acts as the clock gating for the counter. The master clock is controlled by the control MOS transistor which in turn is activated by the preceding FFs. Table 1 shows the various techniques in synchronous counters.

Table 1. Various Techniques in Synchronous Counters

Ref.	**Technique used**	**Switching Power**	**Area/ Device Count**	**Latency**	**Technology**
[1]	Clock gating embedded in Carry propagation circuit	Minimized	Minimized	-	180nm
[2]	Pipeline methodology with counting path and look-ahead path	Increases	Increases	Minimized	180nm
[3]	Cascaded Structure of T FFs, Clock Buffer Network	Low	Minimized		45nm
[4], [11]	Correlated Double Sampling, column-parallel CMOS, 2's complement arithmetic	Low	-	Reducing toggling, Speed increases	180nm
[5]	N Pulse Swallow Counter	Low	-	High Frequency	180nm
[6], [15]	Quantum dot Cellular Automata counter	Low	More	High Speed	-
[7]	Coulter Counter	-	-	High throughput	-
[9]	Scintillating Counter with integrating timing discriminator	-	-	Time walk 200ps	180nm
[12]	The time-optimal algorithm, the non-optimal algorithm	-	-	Speed increases	-
[13]	Fractional N counter Assisted PLL	Low	Jitter Less	High Speed	65nm
[14]	Programmable Voltage Step	Low	Low	High spatial resolution	350nm
[17]	12 Channel Pre-amplifier shaper	Low	-	Low noise charge	350nm

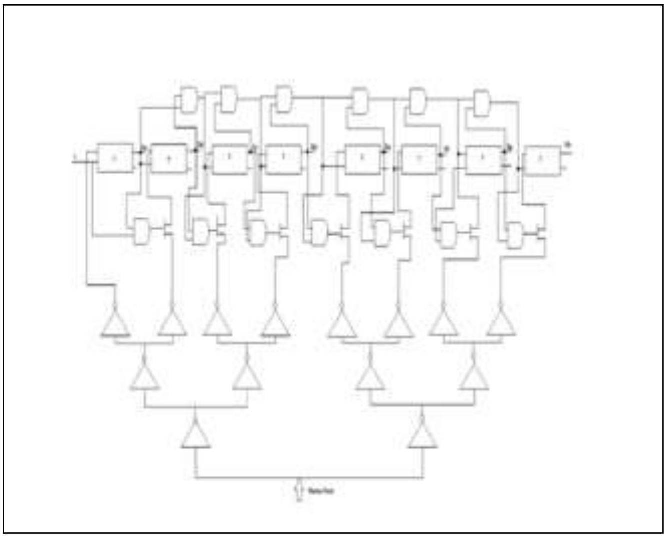


Fig. 3: Block diagram of the 8-bit counter

The block diagram of the proposed 8-bit counter is depicted in Figure 3. TA, TB, TC, TH are the 8 stages of T FFs in the counter. The AND gates from 1 to 7 take inputs from the previous stage output and next stage input clk respectively. i.e. AND1 inputs are from FF1 output and TB clk input, AND2 inputs are from FF2 output and TC clk input, AND3 inputs are from FF3 output and TD clk input, AND4 inputs are from FF4 output and TE clk input, AND5 inputs are from FF5 output and TF clk input, AND6 inputs are from FF6 output and TG clk input, AND7 inputs are from FF7 output and TH clk input. The active condition of the clock and the respective FF status are given in Table 2 and Table 3 for all 256 states of the counter. The clock gating is introduced by MOS transistors with a high threshold by which any unwanted electrostatic charges can be eliminated. This is achieved by disabling the clock signals to the unused logic circuits. Hence the redundant switching power and gate count are reduced to a greater extent. Hence the clock equations for each stage in the proposed 8-bit counter are given by:

$Clk_2 = T_1 . Q_1$; $Clk_6 = T_5 . Q_5$

$Clk_3 = T_2 . Q_2$; $Clk_7 = T_6 . Q_6$

$Clk_4 = T_3 . Q_3$; $Clk_8 = T_7 . Q_7$

$$Clk_5 = T_4 . Q_4; \quad T_{i+1} = Q_i . Q_{i-1} \qquad (7)$$

The clock buffer network is designed to apply the clock to individual stages of the proposed counter with the help of a master clock. This clock buffer network supplies the clock to the clock gating circuit which minimizes the clock skew of the entire counter. Clock buffer network along with the clock gating circuit reduces the power consumption of the proposed 8-bit counter.

4 Results and Discussion

Various block of the proposed counter is designed and simulated to form 8-bit counter designed in a 45nm CMOS process as shown in Figure 4. Functional and Performance verification of synchronous counter is done using Cadence Virtuoso tool as shown in Figure 5. The NMOS transistors in the proposed 8-bit counter are designed with W/L as 120nm/45nm. Table 2 shows the flip-flop active transitions (count: 0 to 127) for the 8-bit counter.

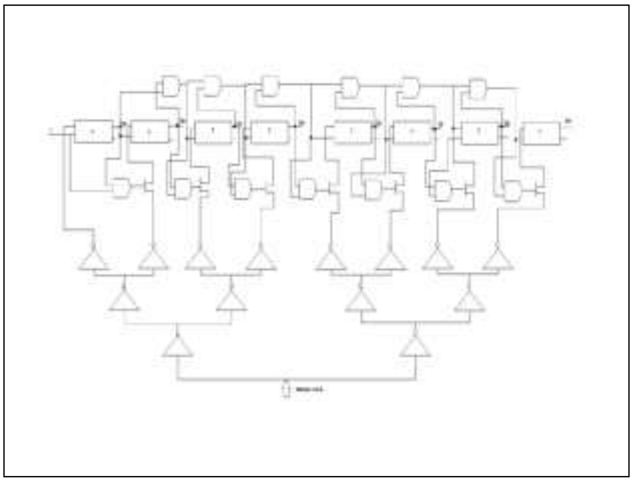
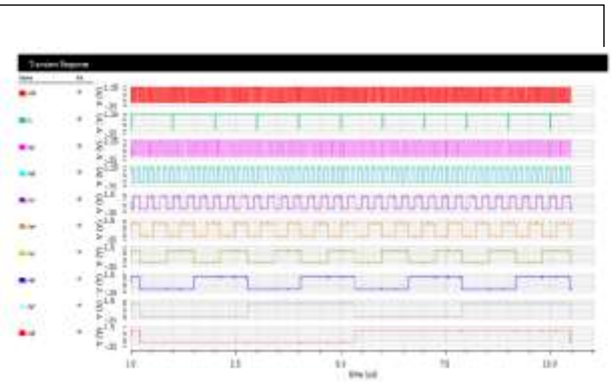


Fig. 4: Schematic of 8-bit counter



Fi

Table 2. Flip-flop active transitions (count: 0 to 127) for 8-bit counter

Output	Active FF	Output	Active FF	Output	Active FF	Output	Active FF
00000000	FF 1	00100000	FF 1	01000000	FF 1	01100000	FF 1
00000001	FF 2	00100001	FF 2	01000001	FF 2	01100001	FF 2
00000010	FF 1	00100010	FF 1	01000010	FF 1	01100010	FF 1
00000011	FF 3	00100011	FF 3	01000011	FF 3	01100011	FF 3
00000100	FF 1	00100100	FF 1	01000100	FF 1	01100100	FF 1
00000101	FF 2	00100101	FF 2	01000101	FF 2	01100101	FF 2
00000110	FF 1	00100110	FF 1	01000110	FF 1	01100110	FF 1
00000111	FF 4	00100111	FF 4	01000111	FF 4	01100111	FF 4
00001000	FF 1	00101000	FF 1	01001000	FF 1	01101000	FF 1
00001001	FF 2	00101001	FF 2	01001001	FF 2	01101001	FF 2
00001010	FF 1	00101010	FF 1	01001010	FF 1	01101010	FF 1
00001011	FF 3	00101011	FF 3	01001011	FF 3	01101011	FF 3
00001100	FF 1	00101100	FF 1	01001100	FF 1	01101100	FF 1
00001101	FF 2	00101101	FF 2	01001101	FF 2	01101101	FF 2
00001110	FF 1	00101110	FF 1	01001110	FF 1	01101110	FF 1
00001111	FF 5	00101111	FF 5	01001111	FF 5	01101111	FF 5
00010000	FF 1	00110000	FF 1	01010000	FF 1	01110000	FF 1
00010001	FF 2	00110001	FF 2	01010001	FF 2	01110001	FF 2
00010010	FF 1	00110010	FF 1	01010010	FF 1	01110010	FF 1
00010011	FF 3	00110011	FF 3	01010011	FF 3	01110011	FF 3
00010100	FF 1	00110100	FF 1	01010100	FF 1	01110100	FF 1
00010101	FF 2	00110101	FF 2	01010101	FF 2	01110101	FF 2
00010110	FF 1	00110110	FF 1	01010110	FF 1	01110110	FF 1
00010111	FF 4	00110111	FF 4	01010111	FF 4	01110111	FF 4
00011000	FF 1	00111000	FF 1	01011000	FF 1	01111000	FF 1
00011001	FF 2	00111001	FF 2	01011001	FF 2	01111001	FF 2
00011010	FF 1	00111010	FF 1	01011010	FF 1	01111010	FF 1
00011011	FF 3	00111011	FF 3	01011011	FF 3	01111011	FF 3
00011100	FF 1	00111100	FF 1	01011100	FF 1	01111100	FF 1
00011101	FF 2	00111101	FF 2	01011101	FF 2	01111101	FF 2
00011110	FF 1	00111110	FF 1	01011110	FF 1	01111110	FF 1
00011111	FF 6	00111111	FF 7	01011111	FF 6	01111111	FF 8

Table 3. Flip-flop active transitions (count: 128 to 255) for 8-bit counter

Output	Active FF	Output	Active FF	Output	Active FF	Output	Active FF
10000000	FF 1	10100000	FF 1	11000000	FF 1	11100000	FF 1
10000001	FF 2	10100001	FF 2	11000001	FF 2	11100001	FF 2
10000010	FF 1	10100010	FF 1	11000010	FF 1	11100010	FF 1
10000011	FF 3	10100011	FF 3	11000011	FF 3	11100011	FF 3
10000100	FF 1	10100100	FF 1	11000100	FF 1	11100100	FF 1
10000101	FF 2	10100101	FF 2	11000101	FF 2	11100101	FF 2
10000110	FF 1	10100110	FF 1	11000110	FF 1	11100110	FF 1
10000111	FF 4	10100111	FF 4	11000111	FF 4	11100111	FF 4
10001000	FF 1	10101000	FF 1	11001000	FF 1	11101000	FF 1
10001001	FF 2	10101001	FF 2	11001001	FF 2	11101001	FF 2
10001010	FF 1	10101010	FF 1	11001010	FF 1	11101010	FF 1
10001011	FF 3	10101011	FF 3	11001011	FF 3	11101011	FF 3
10001100	FF 1	10101100	FF 1	11001100	FF 1	11101100	FF 1
10001101	FF 2	10101101	FF 2	11001101	FF 2	11101101	FF 2
10001110	FF 1	10101110	FF 1	11001110	FF 1	11101110	FF 1
10001111	FF 5	10101111	FF 5	11001111	FF 5	11101111	FF 5
10010000	FF 1	10110000	FF 1	11010000	FF 1	11110000	FF 1
10010001	FF 2	10110001	FF 2	11010001	FF 2	11110001	FF 2
10010010	FF 1	10110010	FF 1	11010010	FF 1	11110010	FF 1
10010011	FF 3	10110011	FF 3	11010011	FF 3	11110011	FF 3
10010100	FF 1	10110100	FF 1	11010100	FF 1	11110100	FF 1
10010101	FF 2	10110101	FF 2	11010101	FF 2	11110101	FF 2
10010110	FF 1	10110110	FF 1	11010110	FF 1	11110110	FF 1
10010111	FF 4	10110111	FF 4	11010111	FF 4	11110111	FF 4
10011000	FF 1	10111000	FF 1	11011000	FF 1	11111000	FF 1
10011001	FF 2	10111001	FF 2	11011001	FF 2	11111001	FF 2
10011010	FF 1	10111010	FF 1	11011010	FF 1	11111010	FF 1
10011011	FF 3	10111011	FF 3	11011011	FF 3	11111011	FF 3
10011100	FF 1	10111100	FF 1	11011100	FF 1	11111100	FF 1
10011101	FF 2	10111101	FF 2	11011101	FF 2	11111101	FF 2
10011110	FF 1	10111110	FF 1	11011110	FF 1	11111110	FF 1
10011111	FF 6	10111111	FF 7	11011111	FF 6	11111111	FF 8

Table 3 shows the Flip-flop active transitions (count: 128 to 255) for 8-bit counter. The detailed transitions are shown in Table 1 & 2. Based on the rising edge of the clock pulses and T-Flip-flop input (Input=1) the flip-flop toggles and the counter counts from 000 00000 to 11111111. The simulation result is shown in Figure 5 the proposed 8-bit counter is performed using HSPICE with a supply voltage of 1.5 V at room temperature with process parameters of frequency 1GHz and observed a power consumption of 69.07µW. The master clock supplies the clock to all stages of T FF in the 8-bit counter through the clock buffer network. This technique activates only the required T FF stage to generate the next counter-state output as depicted in Table 2 and Table 3. For the next count 00000010 in the proposed counter, the FF2 clock is provided from the master clock and appropriately FF2 comes to the active condition. Similarly for the next count to be 00100000 in the proposed counter FF6 clock is provided from the master clock via the clock buffer network and appropriately FF6 comes to active condition. But in this methodology, all T FFs need not be active all the time and hence power consumption of the proposed 8-bit counter is reduced. The proposed counter is simulated for various supply voltages from 0.8V to 1.5V and the respective power consumption is shown in Table 4. As the VDD value is increased the power consumption also increases in the 8-bit counter with a clock gating circuit and clock buffer network connected to a master clock to activate T FF for sequential counting as shown in Equation (8). Table 4 shows the simulated Results for the Proposed 8-bit

Counter. Simulated results show that the designed counter consumes 12.06 µW at 1V supply.

$$P = CVDD^2 \quad (8)$$

Table 4. Simulated Results for Proposed 8-bit Counter

VDD (V)	Power Consumption
0.8	337.8nW
0.9	714.1nW
1.0	2.123µW
1.1	5.76µW
1.2	12.06µW
1.5	69.07µW

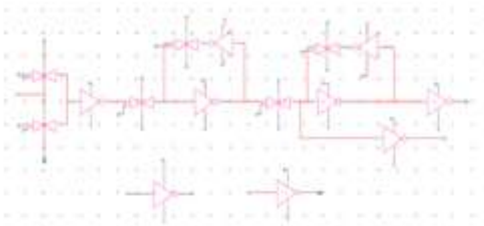


Fig. 6: Schematic of each flip-flop using transmission gates

Thus the master clock which drives the 8 stages of T-FF offers three-fold advantages in the proposed synchronous counter. The 8-bit counter needs 3-level clock buffer networks as repeaters to activate the respective T-FF for the next state count of the counter. By this technique, the edge rates of the clock are avoided at the input of the clock gating network. This, in turn, reduces the noise at the rise time and fall time of the clock. The combination of the clock buffer network and clock buffer network act as the combinational network to reduce the power consumption at all stages of T-FFs are not active all the time. By multi-level clock buffer network, power optimization takes place in the proposed 8-bit clock gating synchronous counter. Thereby unwanted flip-flop clock activity is reduced, device overhead is reduced and circuit complexity is reduced. The internal schematic of each stage T FF using transmission gates is shown in Figure 6.

4.1 Performance Comparison of various Synchronous Counters

The comparison of power consumption and device count of various counters is shown below. The results show that conventional counters with the clock gating technique show reduced device count overhead compared with conventional counters with non-clock gating. Meanwhile, the proposed counter provides a significantly reduced power consumption and device count. Table 5 shows the comparison of the proposed 8-bit counter with other reported works.

Table 5. Comparison of our proposed 8-bit Counter with other reported works

Work	Technology	VDD (V)	Power Consumption	Device Count
Saleh et.al [2]	150nm	1.5	13.89mW	510
Alioto et.al [18]	180nm	1.8	2.21mW	160
Kakarountas et.al [19]	600nm	5	21.3mW	286
Yeh et.al [20]	150nm	1.5	7.64mW	373
Raghava Katr eepalli et.al [44]	45nm	1.0	16.81 µW	-
Young-Won Kim et .al [45]	180nm	1.8	4.7mW (Measured 5.3mW)	517
Aloisi et .al [46]	180nm	1.8	1.7mW (Measured 1.9 mW)	607
Proposed Counter	45nm	1.2/ 1.5	12.06µW 69.07µW	- 346

In the proposed counter, the clock buffer network is efficiently embedded for better performance. The performance of the proposed counter is increased with the conventional counters[21-23]. Table 5 shows the comparison results for the power consumption of various counters. Among various counters, the proposed counter with T FFs provides the best performance in terms of power and device count and it is suitable for clock divider circuits.

5 Conclusion

In this work, a novel clock gating technique is proposed for the synchronous counter. It is a fusion of a clock gating network with a clock buffer network. The master clock is driven by three levels of repeaters for the 8-bit counter. The clock gating technique in the synchronous counter is introduced to obtain the benefits of minimum power consumption and device count in synchronous counters. In the proposed counter T FF concentrates on the activity of the next state output. This controls the clock of the counter and hence reduces the power consumption. As the switching activity is reduced the power consumption is reduced to a greater extent. T FF is a preferred choice in synchronous counters. When compared with the other conventional work the proposed counter consumes less power consumption. Based on the performance, the proposed counter can be used in Analog-to-Digital Converter (ADC), and clock divider applications. The proposed 8-bit counter at 1.5V supply consumes a power of 69.07μW. Simulated results show significant positive results for the proposed 8-bit synchronous counter. The proposed clock-gated 8-bit counter is much more efficient than many of the conventional counters with and without clock clock-gating circuit.

Acknowledgement:
The authors would like to give sincere thanks to the staffs of VLSI Lab, Division of ECE, School of Engineering and Technology, Karunya Institute of Technology and Sciences for providing the Cadence software tool to complete this work.

References:

[1] Young Kim Won, Kim Seong –Joo , Oh Hyuk-Jae, Park Suk-Yoon,Kim Woo Jong, Park Kwang-Il, Kong Sun-Bai, and Hyun Young,Low-Power CMOS Synchronous Counter With Clock Gating Embedded Into Carry Propagation.*IEEE Transactions On Circuits And Systems—II: Express Briefs*: 56(8), 2009, pp.649-653.

[2] Hafeez Abdel Saleh, Member, IEEE, and Ross Gordon Ann, A Digital CMOS Parallel Counter Architecture Based on State Look-Ahead Logic, *IEEE Transactions On Very Large Scale Integration (VLSI) System*,19(6),2011, pp.1023-1033.

[3] Katreepalli Raghava, Haniotakis Th. (2018). Power efficient synchronous counter design, *Computers and Electrical Engineering*. https://doi.org/10.1016/j.compeleceng.2018.01.001

[4] Kim –Seok Jong, Yoon Jin-O, and Deok Choi Byong, Low-Power Counter for Column-Parallel CMOS Image Sensors, *IEEE, APCCAS*: 2016, 978-1-5090-1570.

[5] Kuo Chi Ko, Wu Ji Feng. A 2.4-GHz/5-GHz Low Power Pulse Swallow Counter in 0.18-μm CMOS Technology, 2006, 1-4244-0387-1.

[6] Abutaleb M.M, Robust and efficient quantum-dot cellular automata synchronous counters, *Microelectronics Journal*, 2018, 61, pp.6–14.

[7] Chen Yu, Guo Jinhong, Muhammad Hamidullah, Kang Yuejun, Ary K Sunil,CMOS-compatible silicon-nanowire-based Coulter counter for cell enumeration, *IEEE Transactions On Biomedical Engineering*,2015,0018-9294.

[8] Guana Y.H., Heuvel den van Remco,The three-dimensional model for helical columns on type-J synchronous counter-current chromatography, *Journal of Chromatography A*,2011,5108– 5114.

[9] Jochmann W. Michael,A CMOS Integrated Timing Discriminator Circuit for Fast Scintillation Counters, 45(3),1998, pp. 740-744.

[10] Huang Zhilong, Song Guiqiu, Sun Mengnan Li Yiming,Synchronous control of two counter-rotating eccentric rotors in nonlinear coupling vibration system, *Mechanical Systems and Signal Processing*, 2018, pp. 68–83.

[11] Lee D and Han G,High-speed, low-power correlated double sampling counter for column-parallel CMOS imagers, *Electronics Letters*, 43(24),2007, pp.1362-1364.

[12] Dolev Danny, Heljanko Keijo, Järvisalo Matti, .Korhonen H Janne, Lenzen Christoph, Rybicki Joel, Suomela Jukka, Wiering Siert, Synchronous counting and computational algorithm design, *Journal of Computer and System Sciences*, 82 ,2016, pp.310–332.

[13] Liu Supeng, Student Member, IEEE, and Zheng Yuanjin,A Fractional-N Counter-Assisted DPLL With Parallel Sampling ILFD, *IEEE Journal of Solid-State Circuits*,51(6), 2016, pp. 1361 -1373.

[14] Panina Ekaterina, Pancheri Lucio, Betta Dalla Franco Gian, Massari Nicola, and Stoppa David, Compact CMOS Analog Counter for SPAD Pixel Arrays, *IEEE Transactions On Circuits And Systems—II*:Express Briefs,61(4),2014, pp. 214-218.

[15] Sangsefidi Milad, Yoosefi, Elnaz Abedi, Dariuh, Karimpour Morteza, High speed and low-cost synchronous counter design in quantum-dot cellular automata, *Microelectronics Journal*, 73, 2017, 0026-2692, 2017, pp.1-11.

[16] Ng Poh Kok, Tsimenidis Charalampos, Woo Lok Wai, C-Sync:Counter-based synchronization for duty-cycled wireless sensor networks, *Ad Hoc Networks*, 2017, pp.51–64.

[17] Yeom J. Y., Defendi I., Takahashi . H, Zeitelhack . K, Nakazawa .M, and Murayama. H , A 12-Channel CMOS Preamplifier-Shaper-Discriminator ASIC for APD and Gas Counters, *IEEE Transactions on Nuclear Science*, 53(4), 2006, pp.2092-2096.

[18] Alioto .M, Mita. R, and Palumbo. G 2006 Design of high-speed power-efficient MOS current-mode logic frequency dividers, *IEEE Trans. Circuits Syst. II*, Expr. Briefs, 53 (11), 2006, pp.1165–1169.

[19] Kakarountas A. P., Theodoridis G., Papadomanolakis K. S, and Goutis C, A novel high-speed counter with counting rate independent of the counter's length, *in Proc. IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, UAE,2003, pp.1164–1167.

[20] Yeh . C, Parhami . B, and Wang, Designs of counters with near minimal counting/sampling period and hardware complexity, in *Proc.Asilomar Conf. Signals, Syst., Comput*,2000, pp.894–898.

[21] Zhang Z, He Y, A low error energy-efficient fixed-width booth multiplier with sign-digit-based conditional probability estimation. *IEEE Trans Circuits Syst II Express Briefs*, 65(2), 2018, pp.236–40.

[22] D.S.Shylu ,D.Jackuline Moni,P.Sam Paul, D.Nirmal,A Novel architecture of 10-bit 40MSPS low power pipelined ADC using a simultaneous Capacitor and Op-amp sharing Technique, *Silicon*, 14 (9), 2022,pp. 4839-4847.

[23] Shylu D.S., Jackuline Moni D,A 1.8V 22mW 10 bit 165 MSPS Pipelined ADC for Video Applications, *WSEAS Transactions on Circuits and systems*, 2014,13, 343-355.

[24] Shylu Sam, D.S., Sam Paul, P., Elizah, J., Nithyasri, Snehitha, Singh, A., Vijendra A Novel low power 2-D to 3-D Array Priority Encoder using Split-Logic technique for Data Path Applications, *WSEAS Transactions on Systems and Control*, 17, art. no. 5,2022, pp. 42-49.

[25] Raghava Katreepalli, Haniotakis Th.. Power efficient synchronous counter design, *Computers and Electrical Engineering*, 2019, 75, pp. 288-300.

[26] Young-Won Kim,Joo-Seong Kim,Jae-Hyuk Oh,Yoon-Suk Park,Jong-Woo Kim,Kwang-II Park,Bai-Sun Kong,Young-Hyun Jun,Low Power CMOS Synchronous Counter with Clock Gating Embedded with Carry Propagation. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2009, 56(8).pp.649-653.

[27] W. Aloisi and R. Mita,Gated-clock design of linear-feedback shift registers, *IEEE Trans. Circuits Syst. II, Exp. Briefs*,2008, 55(6), pp. 546–550.

[28] Bhowmik, D. Deb, S.N. Pradhan, B.K. Bhatta charyya,Reduction of noise using continuously changing variable clock and clock gating for IC chips, *IEEE Trans Compon Packag Manuf* Technol, 2016, 6 (6), pp. 886-896.

[29] Q. Wu, M. Pedram, X. Wu,Clock-gating and its application to low power design of sequential circuits,*IEEE Trans Circuits Syst I*,2006, 47 (3), pp. 415-420.

[30] J.P. Hu, T.F. Xu, Y.S. Xia,Low-power adiabatic sequential circuits with complementary pass-transistorlogic,*IEEEWSCAS05*, USA , 2005,pp. 1398-1401.

[31] M. Gautam, U. Nirmal, R. Jain, Low power sequential circuits using improved clocked adiabatic logic in 180nm CMOS processes 2016 *International conference on research advances in integrated navigation systems (RAINS*), Bangalore 2016, pp. 1-4.

[32] Bhargave, S. Uniyal, P. SheokandLow power adiabatic 4-bit johnson counter based on power-gating CPAL logic, *Second international innovative applications of computational intelligence on power, energy and controls with their impact on humanity (CIPECH),* Ghaziabad ,2016, pp. 297-301.

[33] A. Thakur, R. MehraPower and speed efficient ripple counter design using 45 nm technology,*IEEE 1st International conference on power electronics, intelligent control and energy systems (ICPEICES),* Delhi ,2016, pp. 1-4.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

- D.S.Shylu Sam is involved in design, analyses of the proposed work.
- P.Sam Paul helped in Manuscript preparation.
- Joel Samuel simulated the design in Cadence.
- Vimukth John simulated the design in Cadence.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

On behalf of all authors, we state that there is no conflict of interest.

Creative Commons Attribution License 4.0 (Attribution 4.0 International, CC BY 4.0)

This article is published under the terms of the Creative Commons Attribution License 4.0
https://creativecommons.org/licenses/by/4.0/deed.en_US