Analysis and Design of an Active Rectifier for Wireless Power Transfer in 90 nm CMOS Technology

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Abstract: - In this paper, an analysis and design of a new active rectifier used for wireless power transfer applications using 90 nm CMOS technology are presented. The proposed architecture of the active rectifier has mainly been chosen to improve the VCE and the PCE and also to eliminate the need for large on-chip capacitors. The proposed circuits eliminate the drop needed for conduction by replacing diode-connected nMOS devices with others controlled by an active circuit. The new architecture of the active rectifier has been designed, simulated, and laid out by Cadence Virtuoso using TSMC 90nm technology. The input range is 0–5 V, and the output voltage is 2.14 V, with the VCE and the PCE values of 82.9% and 86.2%, respectively. The layout utilizes a compact space of 0.0597 mm2 within the TSMC CMOS 90 nm technology.

Key-Words: - Active rectifier, wireless power transfer, VCE, PCE, RCC, VCR.

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1 Introduction

Wireless power transmission (WPT) day after day continues to seduce more and more applications in many fields. From the typical one of charging electrical vehicles to the most emergent technologies like the IoT. Especially when it gives the promise of disabling the need for physical connectors or wires to get power. The WPT technology possesses the potential to redefine the way that electrical power can be transmitted. However, the rectification process, which consists of converting the ondulated current (AC) received wirelessly from a remote source into a direct current (DC), may have a very deep impact on the global performance of WPT systems. The traditional passive rectifiers used to be widely employed in WPT, but they have been abandoned because of their limitations in terms of lower efficiency and sensitivity to load variations, [1], [2], [3], [4], [5]. Nowadays, new active rectifiers have been emerging as a cutting-edge solution to overcome all these challenges and improve the global performance of WPT systems. The new active rectifiers use, in addition to semiconductor devices, control algorithms to regulate efficiently the flow of energy. These ameliorations and techniques offer higher efficiency and improved adaptability to large load variations. In this context, this paper will deal with the new concept of active rectifiers used in WPT systems, delve into their principles, explain their advantages, and also present the probable potential applications of this innovative technology. In addition, this paper will unveil the essential role of active rectifiers in advancing the field of WPT, paving the way for more and more efficient, versatile, and better wireless charging solutions in our modern era, [6]. [7], presents the most basic structure of rectifiers, the full-wave bridge, where diodes are simply replaced by diode-connected MOSFET elements. Though this topology is simple and easy to implement, it presents a major inconvenience: It requires at least the double threshold voltage, Vtn, of an nMOS device since we are crossing two diode-connected MOS devices in the conduction path for each single cycle of the input signal. Gate cross-coupled and fully gate cross-coupled topologies are improvements over the conventional full-wave rectifier, [8], [9], [10], [11], [12], [13], [14], [15]. In the gate cross-coupled rectifier, two diodes of the conventional rectifier are replaced by two gate cross-coupled MOS devices working as switches, where the voltage drop for every cycle is reduced to one threshold voltage. Similarly, in the full gate cross-coupled rectifier, all diodes are replaced by switches; hence, the voltage drop is further reduced to twice the conduction drop

for every cycle. Despite having the least voltage drop, this topology suffers from the problem of reverse charge leakage. This occurs when the input AC amplitude is less than the output rectified voltage, causing the conducting pass devices to be on simultaneously, resulting in current flowing backward from the output to the input, [16], [17], [18], [19], [20].

All of the above-discussed topologies suffer from either a large voltage drop or significant power loss, which limits their use in low-power and low-voltage devices. Popular techniques for achieving higher efficiency include using gate cross-coupled rectifiers in combination with passive or active circuitry to control the other two pass devices. In passive rectifiers, additional circuitry, including a bootstrap capacitor, is employed to reduce or eliminate the threshold voltage, as discussed in this paper, [21], [22]. However, the use of on-chip bootstrap capacitors limits their applicability when the chip area and speed are highly important. In contrast, active rectifiers utilize active circuitry to control pass devices. This approach increases both the voltage conversion efficiency (VCE) and power conversion efficiency (PCE) by ensuring that the pass devices operate in the linear region, resulting in reduced conduction losses and the complete elimination of reverse current flow, thereby reducing power loss. However, active rectifiers are not without their challenges. The primary issue is the startup of the active circuit, as there is no regulated supply during this phase.

2 Design

In this work, an active rectifier is chosen, primarily for better VCE and PCE and secondarily to avoid the use of large on-chip capacitors. [23], [24], [25], [26], discuss the same active rectifier topology with a slight difference in active circuitry. [23], implements a comparator with compensation for the delay of the comparator's output falling, whereas, [24], [25], [26], implements a comparator with compensation for both the falling and rising delays of the comparator's output at the expense of added circuit complexity and power consumption. [23], has been used here thanks to its simple design.

Fig. 1a, Fig. 1b, and Fig. 2 show the CMOS implementation of the conventional full-wave bridge rectifier, gate cross-coupled rectifier, and proposed active rectifier in [23]fier, and proposed active rectifier in [23]. The issues with Fig. 1a and Fig. 1b have already been briefly mentioned above. Although Figure 1b is a significant improvement of Fig. 1a, it is still not a favorable topology concerning the chosen design technology. In the gate cross-couple rectifier shown in Fig. 1b, the cross-coupled pMOS transistors act as switches, so the only voltage drop across them is the conduction drop because of channel resistance. However, the other two nMOS transistors are diode-connected, which means that they have at least a Vtn drop across them, implying that Vin ≥ Vdc + Vth for conduction.

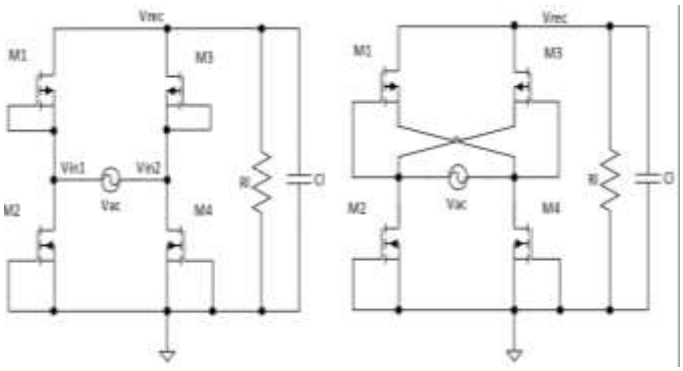

Fig. 1: Rectifier topologies: (a) conventional and (b) gate cross-coupled topologies

The proposed active circuit in Fig. 2 is an improvement of that in Fig. 1b; this circuit eliminates the Vtn drop needed for conduction by replacing the diode-connected nMOS with devices controlled by the active circuit, as shown in Fig. 3. The active circuit is a four-input comparator that turns on nMOSes quickly when Vin ≥ Vrec and turns off rapidly to prevent the flow of current.

To illustrate the operation of the comparator, consider the case when $V_{in1} > V_{in2}$, i.e., $V_{in1} > 0$and $V_{in2} < 0$. During this half cycle, the comparator D_1 output is low, turning off M_{n2}. Additionally, Mp1 is reverse biased, resulting in no current flow path along Mn2 or Mp1. For simplicity, assume Vin = Vin1 - Vin2. When Vin reaches Vtp, Mp3 turns on, shorting Vin1 to Vrec. When Vin > Vrec, the D2 output becomes high, turning on Mn4 and initiating the conduction path for the first half cycle, which starts charging Cl. When Vin reaches its maximum, it begins to decrease, and when Vin < Vrec, conduction stops since the output of D2 is low and Mn4 is off. As Vin further decreases below Vtp, Mp3 is also off. In this manner, the rectifier in Fig. 2 conducts currents during the positive half cycle, eliminating the Vtn drop observed in Fig. 1b. Now, the only drop is the conduction drop due to the channel resistance of the two pass devices along the conduction path. This drop is much smaller because during conduction, both devices operate in the linear region with low resistance. The operation is similar

when Vin2 > Vin1, with Mn4 and Mp3 off, while Mn2 and Mp1 charge Cl.

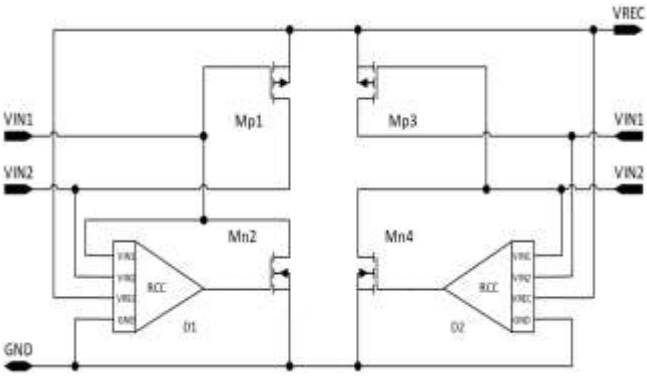

Fig. 2: Gate cross-coupled full-wave active rectifier

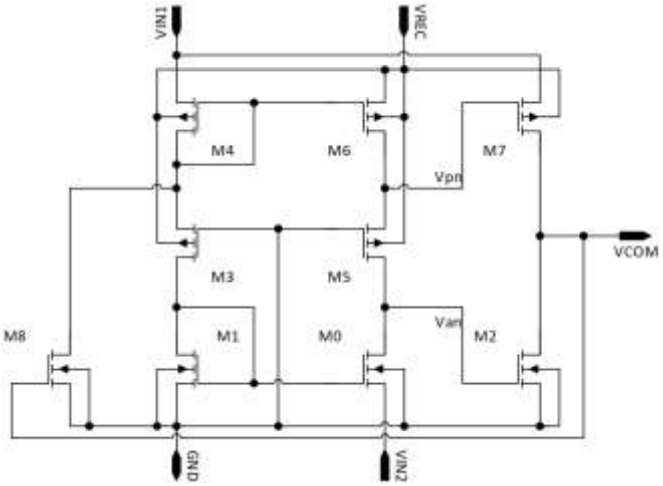

Fig. 3: Comparator circuit, RCC

Fig. 3 shows the implementation of the four-input comparator D_2 used in Fig. 2, as proposed in, [19]. It is designed to self-power and bias because no steady-state supply is available at start-up. M_1, M_2 and M_7 monitor voltages across M_{n4}, i.e.,$M_{n2} - V_{gnd}$, and M_3, M_4 and M_8 monitor voltages across M_{p3}, i.e., $V_{in1} - V_{rec}$. Therefore, when $V_{in1} - V_{rec} \geq V_{n2} - V_{gnd}$, which means $V_{in} > V_{rec}$, the output of D_2 is high, and M_{n4} is activated instantly. However, when $V_{in} < V_{rec}$, the output of the comparator is delayed, which causes M_{n4} to conduct in the reverse direction, leading to a significant reduction in the power delivered to the load. M_8 is introduced to overcome this problem by adding offset currents to increase V_{an} and V_{pn} faster, causing the output to decrease faster and turn off M_{n4} before $V_{in} < V_{rec}$. This reverse current control technique compensates for the comparator delay and increases the power efficiency of the rectifier.

Fig. 3 depicts the implementation of the four-input comparator D2 used in Fig. 2, as proposed in, [19]. It is designed for self-powering and biasing since no steady-state supply is available at startup. M1, M2, and M7 monitor the voltage across Mn4, i.e., Mn2-Vgnd, while M3, M4, and M8 monitor the voltage across Mp3, i.e., Vin1-Vrec. Therefore, when Vin1-Vrec ≥ Vn2-Vgnd, which implies Vin > Vrec, the output of D2 becomes high, and Mn4 is instantly activated. However, when Vin < Vrec, the output of the comparator is delayed, causing Mn4 to conduct in the reverse direction, resulting in a significant reduction in the power delivered to the load. M8 is introduced to overcome this issue by adding offset currents to reach Van and Vpn faster, causing the output to decrease faster and turning off Mn4 before Vin < Vrec. This reverse current control technique compensates for the comparator delay and increases the power efficiency of the rectifier.

The design parameters for the rectifier are listed in Table 1. The dimensions of the pass devices are initially calculated using the square law current equation and the device parameter values given in the technology documents. They are later optimized with a simulation tool to ensure that the rectifier can deliver the needed current. Since nMOS pass devices do not need to have the same device size as pMOS devices to deliver the same current, the optimal size ratio equation from, [27], [28], [29], [30], is used to determine the sizes of the nMOS pass devices. Although the maximum load for this work is 10 mA, it is always simulated with an additional 0.5 mA of load. This extra current accounts for the fact that the RCC is self-powered, and the LDO, which will follow this rectifier, will be powered by V_rec. Similarly, the value of the ripple rejection capacitor is chosen to be 100 nF. This size of the filter capacitor is calculated based on the capacitor's current–voltage relationship, with the assumption of keeping the peak–to-peak ripple voltage below 5 mV while delivering 11 mA of current.

Table 1. Rectifier design parameters

Parameters	Values
Wn/Ln , Wp/Lp	720 µm/280 nm, 1.2 mm/280 nm
Rectifier area	TBA mm2
Input AC magnitude Load current Ripple rejection capacitor	13.56 MHz 10.5 mA 100 nF

3 Simulation Results

The proposed architectural design has been simulated in Cadence Virtuoso using TSMC 90 nm technology. Fig. 4 displays the layout of the proposed rectifier, and the surface area of this architecture was measured to be 0.0597 mm².

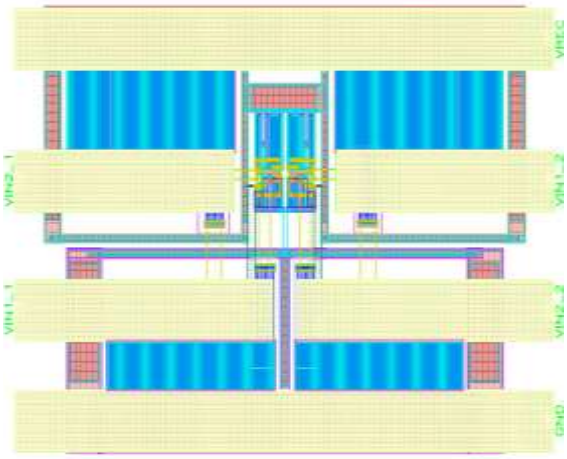

Fig. 4: Layout of the proposed rectifier

3.1 Transient Performance

Fig. 5 presents both pre- and post-layout results for the input voltages V_{in1} and V_{in2} and the output voltage V_{rec} for one cycle of AC input. A closer view of the rectified output is shown in Fig. 6. The voltage drops of approximately 60 mV in the layout account for the voltage drop due to the resistance of the high-current conduction path.

Fig. 7 shows the simulation results showing voltages at rectifier inputs and the output rectified voltage along with the corresponding current waveform through rectifying MOSs. When comparing schematic and post-layout results, two important observations can be made from the plots. The first is the reduction in the peak diode current in the post-layout result. This is because of the channel resistance of the rectifying diodes, as well as the additional resistance of the high-current conducting path in the layout. In the schematic (Fig. 2), the paths are ideal wires with no resistance and hence a higher peak current. Second, the reverse leakage current is more pronounced in the post-layout simulation. This is because a wide path runs over the drain and source of the rectifying diodes, creating a larger parasitic capacitance. This causes a slight delay in turning off the diodes.

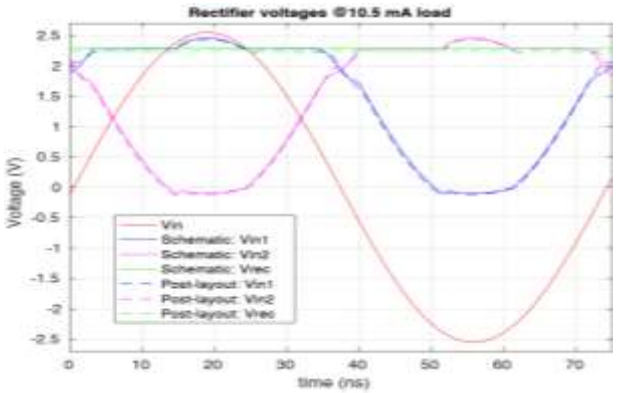

Fig. 5: Voltage waveforms for the pre- and post-layout positions

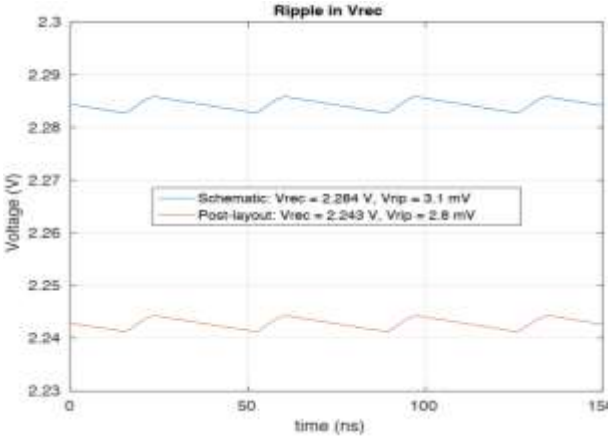

Fig. 6: Rectified outputs for pre- and post-layout

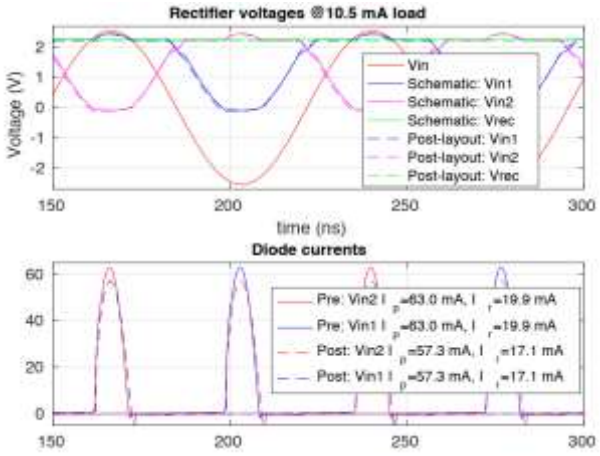

Fig. 7: Voltage and current waveforms of the rectifier

3.2 DC Performance

Similarly, Fig. 8 shows the PCE, the ratio of the power delivered to the load to the average power from the source; the VCE, the ratio of rectified DC, V_{rec} to the peak AC input, $|V_{in}|$concerning the magnitude of the peak AC input signal. $|V_{in}|$ is gradually increased in peak magnitude in steps of 50 mV, and VCE and PCE are calculated for every step. The plot shows that both the PCE and VCE are

much lower for input AC amplitudes less than 1.8 V. This can be explained by the fact that the needed bias current and gate drive voltage for the RCC circuit are not achieved for smaller inputs.

Table 2 comparatively summarizes the performance of the pre-and post-layout results of the design. The layout design is described in the appendix. The layout is symmetrical with four, instead of two, inputs, as seen in the test bench (Fig. 4). This is done to make the current conducting path equal, which results in an equal drop in voltage when it reaches the rectifying MOSs. Similarly, the paths from the pad to the rectifier inputs are mask-blocked for random metal fill to avoid interlayer coupling. The high-current conduction routes are designed with a wide parallel path of many higher-level metal layers to reduce the resistance in the conduction path.

Table 2. Rectifier performance summary

Parameters	Schematic	Post Layout
Rectified DC	2.28 V	2.14 V
Ripple Vpp	3.1 mV	2.8 mV
Peak diode current	63 mA	57.3 mA
PCE	84.5%	82.9%
VCE	88.6%	86.2%

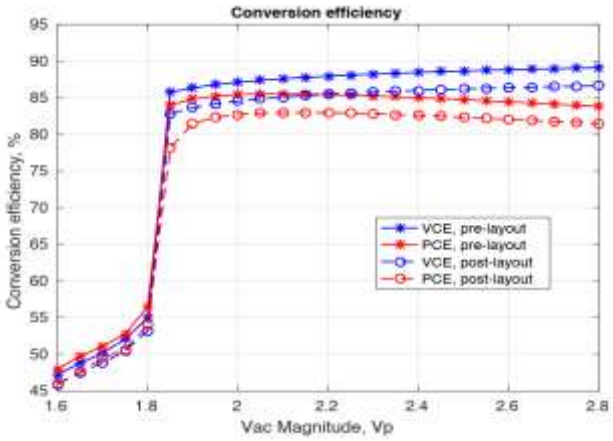

Fig. 8: Voltage and power conversion efficiency

4 Conclusion

An active rectifier for wireless circuits, designed and layouted in 90 nm CMOS technology, is compact, energy-efficient, and cost-effective. The proposed active rectifier consists of several blocks (gate cross-coupled full-wave active rectifier and comparator circuit, RCC) to generate an output voltage of 2.14 V. The input voltage ranges from 0 to 5 V. The power conversion efficiency (PCE) and voltage conversion ratio (VCR) are higher than 84.5% and 86.6%, respectively, over a wide voltage range (from 1.6 V to 2.8 V), the chip area is only 0.0597 mm². This work is suitable for wireless power transfer.

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Conflict of interest

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