Design of Low Power SAR ADC with Novel Regenerative Comparator

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Abstract: - This paper introduces two low-power design techniques for a successive approximation register (SAR) analog-to-digital converter (ADC) used in transmitting physiological signals. The first technique is called dual split switching, involving the use of a one-sided charge-scaling digital-to-analog converter (DAC) to minimize switching energy by reducing leakage in a dual transmission gate. The second technique, known as the set and reset phase, determines the amplification and comparison phases of the comparator. This approach reduces the delay time of the comparator through the use of a folded cascode pre-amplifier and a regenerative latch. The design includes a Serial-in-Parallel-Out (SIPO) N-bit register and SAR, implemented using negative edge-triggered D flip-flops (DFFs). To optimize power consumption, the supply voltage of the SAR ADC is set to 500 mV. The concept of a variable threshold is utilized throughout the design to enable operation with this lower supply voltage. The SAR ADC is designed to support a sampling rate of up to 1 Msps (mega-samples per second). The circuit is implemented using standard UMC180nm technology. According to the test results, the power consumption of the SAR ADC is only 29.06 uW, and the achieved sampling rate is 5 Ksps (kilo-samples per second). The maximum differential non-linearity (DNL) is measured to be +0.9/−0.82 least significant bits (LSBs).

Key-Words: - SAR-ADC, charge scaling, delay, transmission gate, supply voltage, DNL.

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1 Introduction

There has recently been a growing interest in the development of wireless communication-based biomedical applications, [1], [2]. Extensive research has focused on acquisition boards for Electrocardiogram (ECG) and Electroencephalogram (EEG) signals, resulting in excellent outcomes for biomedical applications, [2]. The primary role of a biosignal procurement board is to capture weak amplitude and frequency biosignals from the human body, amplify them, and transmit them in digital form, [3], [4]. To ensure the continuous transmission of physiological signals, it is crucial to extend battery life, reduce device size for implantation on the human body, and maintain high data accuracy, [5], [6].

As advanced CMOS processes offer benefits such as smaller feature sizes and operation at lower threshold voltages, leakage currents play a dominant role in power consumption, [7]. Therefore, in addition to accommodating a lower supply voltage, minimizing leakage power is essential to achieve optimal power efficiency. High data accuracy is particularly crucial when wirelessly transmitting physiological signals, as neural signals have low amplitudes (less than 100 uV) and frequencies ranging from a few Hz to below 100 Hz, [8]. Physiological signals are pure analog signals captured from the human body using transducers. The successive approximation register (SAR) type analog-to-digital converter (ADC) is a vital component in analog signal processing, [9], [10]. SAR ADCs are available with resolutions ranging from 8 to 18 bits and sampling rates up to 50 Msps, [11]. SAR ADCs are well-suited for transmitting physiological signals compared to other ADC architectures, [12], as depicted in Figure 1.

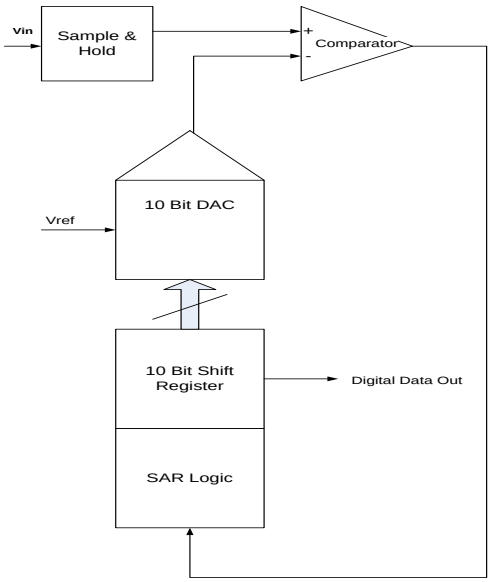

Fig. 1: Proposed SAR ADC Architecture

It is recommended to utilize a 0.5V bulk-driven folded-cascoded OTA for creating an energy-conserving polyphonic signal transformation system, [13]. The machine-readable data obtained from the SAR ADC is stored in a low-power 16x16 SRAM array, [14]. Small capacitance values are employed in the charge redistribution digital-to-analog converter (DAC) with a one-sided split capacitor set to enhance transition time and minimize space. Following additional control measures suggested in references, [15], the DAC operates in two states: the data acquisition state and the transition stage. Additionally, this study introduces a uniquely designed, extremely energy-efficient comparator created to function in the sub-threshold zone. During the restorative stabilization period, adaptable body effect control is applied to operate the transistor in the weak accumulation region, reducing leakage current using a 500 mV supply voltage. Various optimization techniques have been implemented in the ADC blocks to curtail power usage, [16].

In Section II, the proposed SAR ADC is presented, providing an overview of its architecture and operation. Section III presents a detailed description of the circuit design for each block of the ADC. The measurements of the proposed design's outcomes are presented in Section IV, along with a comparison to previous works in the field. Section V summarizes the results and discusses potential future study directions to bring the work to a close.

2 Proposed Strategy for Energy Conservation

2.1 Variable Threshold CMOS (VTCMOS)

In the existing setup, the critical potential is managed by continuously tuning the bulk bias potential of the MOS transistor. The adaptable bulk bias regulating circuit facilitates the production of substrate voltages for nMOS and pMOS transistors. The circuit employs a transmission gate using the VTCMOS strategy, as illustrated in Figure 3b. This configuration allows for energy optimization due to the lower V_{DD} voltage and a high turnaround time due to the lower V_{TH} threshold voltage. The bulk bias regulating circuit generates an increased bulk bias potential for the pMOS transistor and a decreased bulk bias potential for the nMOS transistor when the device is in standby mode. Consequently, the body effect causes the levels of the terminal potential (V_{THn} and V_{THp}) to rise in the standby state. As the terminal potential rises, the sub-threshold leakage current exponentially declines. This design technique significantly reduces leakage energy consumption during idle mode. However, it should be noted that as technology scales down, the effectiveness of the VTCMOS technique becomes compact, or the V_{TH} values are lowered.

2.2 Dual Split Switching

The dual split switching technique is implemented using a 2:1 multiplexer (MUX) design. In the electric potential adjustment DAC, a 2:1 MUX is employed to switch between the input electric potential (V_{in}) and the reference electric potential (V_{ref}). The main component utilized in the MUX structure is the transmission gate, [17].

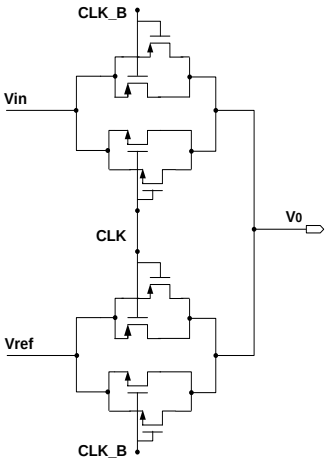

Fig. 2: 2:1 Mux with dual transmission gates and a mechanism for decreasing on-resistance

In this configuration, two NMOS and PMOS transistors are arranged in a shunt configuration, as illustrated in Figure 2b. This arrangement ensures the minimum feasible on-resistance and sampling inaccuracy. The length and width of the transistors are set in a 2:1 ratio. As mentioned earlier, the transmission gate operates using the VTCMOS strategy, as depicted in Figure 2. This technique optimizes the performance of the transmission gate, reducing power consumption and enhancing overall efficiency.

3 Model features of SAR ADC

In Figure 1, the SAR ADC architecture adheres to a standard ADC design, but crucial modules within the SAR ADC incorporate low-power optimization techniques. Notably, the Variable Threshold MOS (VTCMOS) technique and dual transmission gate technique are applied to operate transistors in the sub-threshold region, reducing leakage current and minimizing on-resistance in the transmission gates. The subsequent sections will delve into the detailed design process of these blocks.

3.1 Comparator

In ADC and other electronic devices, the energy-efficient regenerative comparator circuit plays a crucial role. The main goal is to design a preamplifier regenerative comparator circuit with increased transition time and reduced power consumption, [18], [19]. The schematic for the suggested circuit is shown in Figure 3a. The comparator operates in two phases: the pre-amp phase (reset) and the fluctuating comparative cycle (set). Further reduced on-resistance toggles S1 and S2 are integrated, as illustrated in Figure 3b. These switches are powered by distinct timing intervals.

During the reset cycle, switch S2 is closed, while switch S1 is unconnected. This structure enhances the voltage variation between both signal inputs by 40.4dB, thanks to the single-stage folded amplifier. In the set phase, switches S1 and S2 open and close, allowing the regenerative comparator circuit to compare both signal inputs during the chosen collecting periods. These initializations and reinitialization approaches help reduce non-systematic and variance errors during the analog-to-digital conversion process. A logic high level (1) is indicated when Vin > Vref, and a logic low level (0) is indicated when Vin < Vref in the response signal.

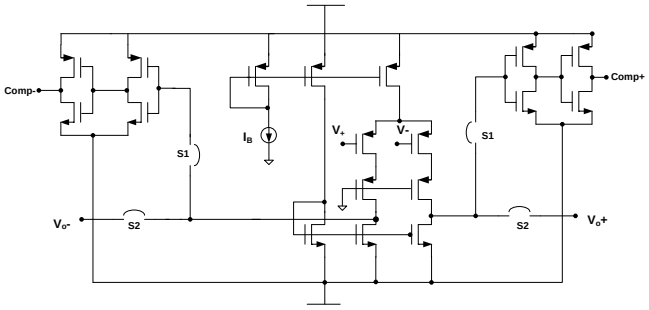

Fig. 3a: Preamplifier Regenerative Comparator Circuit Schematic

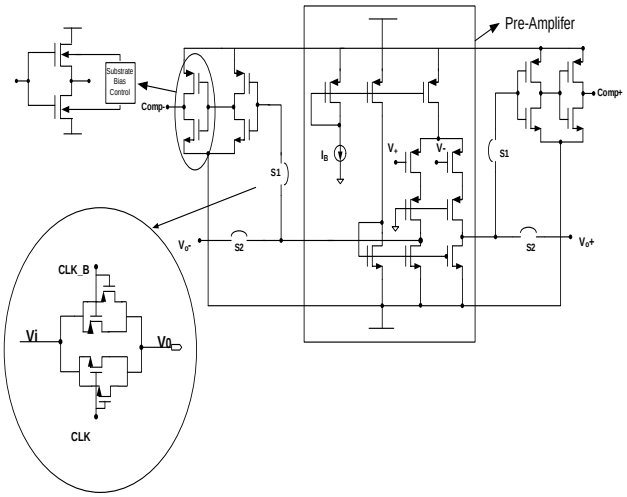

Fig. 3b: Switches based on transmission gates with low on resistance

The proposed design employs a folded cascode operational transconductance amplifier (OTA) as the preamplifier, as illustrated in Figure 3b, [20]. Transistors T_5 and T_6 implement the present scaling approach, delivering differential currents through a current mirror composed of transistors M_{b1}, M_{b2}, and M_{b3}. These asymmetrical currents are then received by the output stage for voltage-to-current conversion. Table 1 shows the transistors T_1–T_6 and operate in the weak inversion region with an appropriate width-to-length (W/L) ratio.

The overall electrical usage of the comparator is 1.8 uW, considering a rail-to-rail supply voltage of 500 mV. The current scaling technique generates a small current difference between M_4 and M_6, contributing to the comparator's operation. Output impedances are increased to achieve proper current scaling, and source-degenerated current mirrors are formed with transistors M_5 and M_6. Resistors R_2 and R_3 set the currents in the regenerative circuit.

To maintain a small difference between the currents in M_3 and M_4 and the currents in M_5 and M_6 relative to the currents in M_1 and M_2, a current scaling ratio is established. The currents in the folded branch transistors (M_3 and M_4) are set to one-

third of the differential input pair current ($I_B/3$), while the currents in M_5 and M_6 are set to $8I_B/7$. The current scaling ratio between transistors M_{b1} and M_{b2} is 7:1 ($2I_B/14$) to save power in the bias circuit. Resistors R_2 and R_3 are instrumental in achieving these current ratios, with the ratio between R_1 and either R_2 or R_3 set at 1:50.

Table 1. Pre-amplifier Design

Devices	Width/Length	I_D	Conducting Region
T1:T2	20um/180nm	393nA	Subthreshold
T3:T4	50um/180nm	393nA	Subthreshold
T5:T6	10.02um/200nm	505nA	Subthreshold

To minimize glitches during switching and prevent signal loss, we employ a transmission gate-based switch to change amplifier and converter operations. To reduce the on-resistance of the transmission gate, we connect additional low-W/L ratio pMOS and nMOS transistors in parallel with the existing gate. This configuration lowers the on-resistance while ensuring proper signal integrity during switching operations.

3.2 Sample and Hold

To collect and retain the signal, we utilize a CMOS transmission gate and a capturing capacitor. To mitigate electric potential injection errors, we incorporate a dummy switch, as depicted in Figure 4. The unused switch is controlled by the reversed clock signal and serves to absorb the electric potential injection caused by the sampling switch. By using this dummy switch, we eliminate unwanted glitches, contributing to improved performance.

To further enhance the ADC design and minimize differential non-linearity (DNL) and integral non-linearity (INL), connect a buffer at the end of the sample and hold the circuit. The buffer aids in increasing the continuity of the ADC by compensating for any variations or distortions introduced during the sampling and holding process, resulting in a more accurate conversion of the analog signal to digital form.

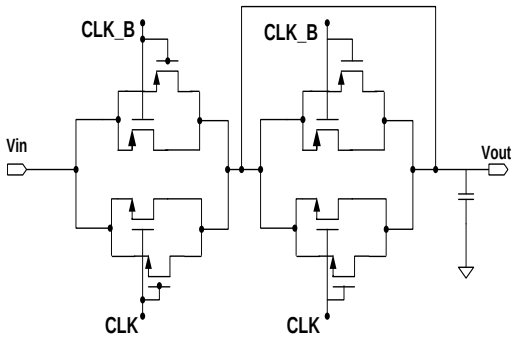

Fig. 4: Circuit for a sample and hold with a dummy switch

3.3 Digtal to Analog Converter (DAC)

In the design of a 10-bit charge-scaling capacitive DAC, a combination of two 5-bit charge-scaling sub-DACs is used, along with a scaling capacitor C_s, as illustrated in Figure 5. The scaling capacitor C_s is connected in series between the LSB (Least Significant Bit) array and the MSB (Most Significant Bit) array. This series of combinations of scaling capacitors starts with the LSB array and terminates with the MSB array.

The accuracy of the DAC is dependent on the scaling capacitor C_s, since it serves as the terminating capacitor between the LSB and MSB arrays. The value of C_s determines the overall scaling factor of the DAC and affects the linearity and precision of the output digital representation. Proper sizing and calibration of C_s are crucial to ensuring accurate and reliable conversion of the analog input signal to its corresponding digital code.

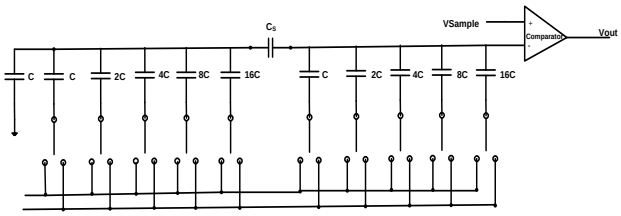

Fig. 5: Regenerative comparator and suggested digital-to-analog converter

The area of the DAC is directly proportional to the size of the unit capacitor used. Based on simulation test results, the value of the unit capacitance is determined to be 62.5 fF. To enhance linearity and reduce comparator offset errors, the folded cascode operational amplifier discussed in the previous section is utilized as a buffer in the DAC. This operational amplifier helps to improve the linearity of the DAC output. Figure 6 illustrates the sampling circuit designed with a simple transmission gate using the Variable Threshold CMOS (VTCMOS) technique. By operating the

transmission gate with a variable threshold voltage, as shown in Figure 3b, the VTCMOS technique is employed. The total capacitance on the left side of the scaling capacitor is 2 nF, while on the right side of the scaling capacitor, it is 2.62 nF.

The DAC module contributes to approximately 40% of the overall power intake of the ADC due to its varying power usage. During changing events, the charging phase of the capacitances releases additional heat in the circuit. However, the swapping technique minimizes switching energy by reducing the on-resistance of the transmission gate, as described in subsequent parts. The power analysis of all the modules can be seen in Figure 6, providing insights into the power consumption distribution in the ADC design.

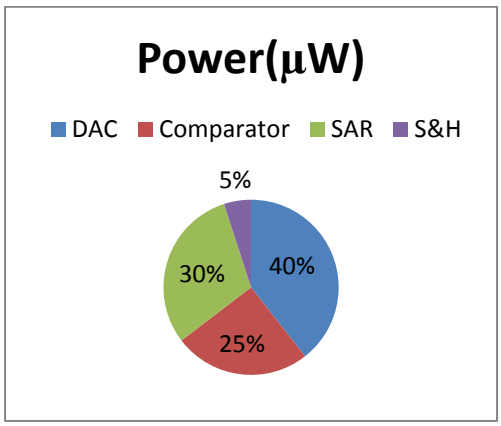

Fig. 6: Power measurement of ADC Blocks

In the design of the ADC, the performance of the DAC is judged based on several metrics, including differential nonlinearity (DNL) and integral nonlinearity (INL). These metrics help assess the linearity and accuracy of the DAC's output. DNL is stated to be a variation between actual step width of the DAC output and the ideal value of 1 LSB (Least Significant Bit). It measures the deviation of each step from the ideal value. A DNL value of 0 indicates perfect linearity, where each step is exactly 1 LSB. Positive or negative deviations from 1 LSB indicate nonlinearity.

In this paper, despite the ADC design targeting a small quantity of signal use, such as physiological signals, efficiency metrics, including DNL, are evaluated to ensure an efficient ADC design. Figure 8 provide an overview of the performance metrics, indicating the importance of achieving accurate and linear conversion of analog signals to digital form.

$$1\ LSB = \frac{V_{FSR}}{2^N}$$

$V_{FSR}$is the whole scale range, and N is the ADC's precision. The recommended ADC resolution is ADC is 10 bit and $V_{FSR} = 100mV$, so 1 LSB value is 100uV.

$$DNL = \left[\frac{V_{D+1} - V_D}{V_{LSB\ IDEAL}} - 1\right],$$
$$where\ 0 < D < 2^{N-2}$$

3.4 SAR Control Logic

The successive approximation register (SAR) ADC architecture offers the advantage of zero latency compared to other ADC architectures. The basic building block used in the SAR control logic is a D Flip-Flop (DFF), which is designed with a low on-resistance transmission gate using the Variable Threshold CMOS (VTCMOS) technique, as explained in the previous sections.

The gate-level circuit diagram of the SAR control logic is depicted in Figure 7. DAC linearity shows in Figure 8. This control logic plays a crucial role in the operation of the SAR ADC. It facilitates the comparison and decision-making process during the successive approximation conversions. By using DFFs with low-resistance transmission gates, the SAR control logic ensures efficient and accurate conversion of the analog input signal.

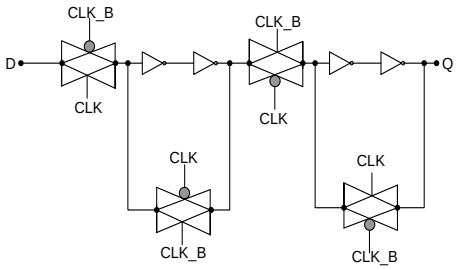

Fig. 7: D Flip-Flop Gate Level Circuit Proposal in SAR Control Logic

The SAR ADC architecture, with its zero latency and the incorporation of low - low-resistance transmission gates in the control logic, offers an effective solution for achieving high-speed and accurate analog-to-digital conversion.

4 Test Results

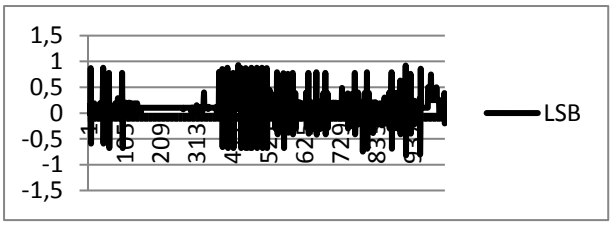

Fig. 8: Measured DNL

The block diagram of the ADC was developed in the UMC180nm CMOS process and tested. Figure 10 shows a full schematic view in the cadence virtuoso editor. The sampling frequency is 40 kS/s, and the power supply voltage is 0.5 V. Figure 9 and Figure 11 shows the ADC output and DAC output.

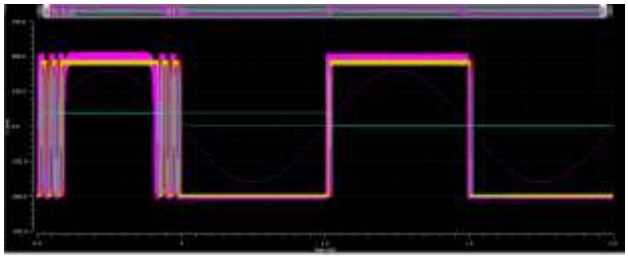

Fig. 9: Measured ADC output for 100Hz sine wave input

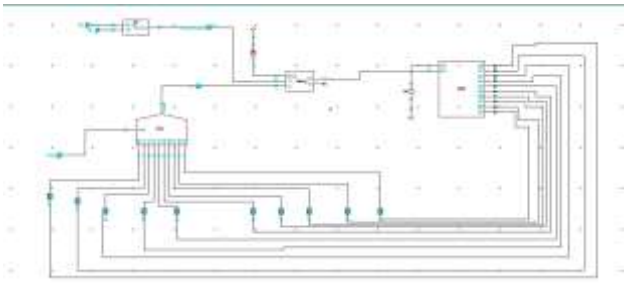

Fig. 10: Proposed Schematic design in Cadence UMC180nm Technology

Fig. 11: Measured 10-bit DAC output

Table 2. Key Parameters of Proposed SAR ADC

Design	**SAR**
Supply Voltage	0.5
Power consumption[uW]	29.06
Technology[nm]	180
Resolution[Bits]	10
F_{sample} [Msps]	Up to 1
DNL(max)	+0.9/−0.82 LSB
INL	0.94LSB

5 Conclusion

The presented SAR ADC is a 10-bit architecture that operates with a 100mV reference voltage (V_{ref}). It incorporates a dual split switching network in the digital-to-analog converter (DAC) to minimize switching energy. The DAC is designed with low-power techniques to ensure efficient operation as proven by the DNL and INL from Table 2. The key component, the regenerative comparator, operates in the subthreshold region with low offset to achieve high performance. Furthermore, the SAR logic is designed with low power consumption and utilizes negative edge-triggered flip-flops. This design choice helps reduce power consumption while maintaining the functionality of the ADC. The ADC operates at a supply voltage of 500mV, further contributing to low power consumption. The measurement results validate the effectiveness of the design, with the ADC consuming only 29.06uW of power. This low power consumption makes the ADC suitable for power-constrained applications.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed to the present research, at all stages from the formulation of the problem to the final findings and solution.

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Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.