Fault Identification in Modified Hybrid Digital Pulse Width Modulation using Triple Modular Redundancy

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Abstract:- In this paper, the fault analysis is performed for the identification in the Modified Hybrid Digital Pulse Width Modulation by making use of the Triple Modular Redundancy method. The developed algorithm is real time implemented using the Xilinx Artix 7 FPGA device. The Modified Hybrid Digital Pulse Width Modulation is designed for the purpose of minimizing the Turn-ON and Turn-OFF delays in the triggering event of the generated Digital Pulse Width Modulation. Though additional compensatory circuits are added for the delay reduction, the area utilization is still low when implemented in FPGA device. Also, the Triple Modular Redundancy consists of three times of MHDPWM signal generation to check for the fault occurrence. For the sake of validating the fault identification, the majority voter circuit is used that could find the error at the earliest. The proposed method is checked for errors by inducing within the VHDL code and trailed with multiple duty cycle values. The proposed fault identification method is validated for VLSI parameters such as area, delay and power.

Key-Word: - Triple Modular Redundancy, Digital Pulse Width Modulation, Fault Identification, Field Programmable Gate Array, delay, triggering event, area, power, MHDPWM.

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1 Introduction

Faults happen in real time circuits due to several reasons such as interference, noise, and environmental issues. The major concern in the occurrence of fault is the inoperability of devices connected in the circuit. The faults can be classified as Permanent Fault and Temporary Fault based on the size and repair time of the faults.
In digital circuits, the faults occurrence can exhibit errors as the value flows from the input to the output and thus degrades the operation of the circuit. Though there are different testing algorithms for digital designs that can check for errors, quarantine and correct the errors by making use of the generated test patterns. The above stated algorithms consume time and diminish the working of the circuit under test. To eradicate these, the redundancy structure is employed that considers the repetitive circuit structure and permits concurrent manipulation. The error is evaluated in the redundancy circuit by considering of the majority of the three replicated circuits as the correct output for the circuit under test. The redundancy method utilized is referred as Triple Modular Redundancy (TMR) and can be extended for 5MR or NMR algorithm.

The TMR process selects the best output among the three possible combination of the design under test by making use of the voter element block. The TMR has increased efficiency and reliability in terms of permanent and timing errors, [1]. The advent of heterogeneous system has paid way for the accurate identification of errors along with correction in the field of semiconductor technology, [2]. The absence of voter element in TMR has enhanced speed in signal propagation, clocking and reduced number of transistors in circuit, [3]. The decrease in the internal error in signal propagation is attained using the ATMR that uses pass transistor implementation in design for voter element, [4]. The thrust in error mask is highlighted using specific compiler for the ATMR technique, [5]. The area optimization and low loss in reliability is achieved using the STMR technique, [6].

The redundancy circuit is designed with the Quade Shape NAND logic to guarantee secure working of the voter element, [7]. The secondary fault inducer fused with the mission-critical process can aid in the finding of persistent error in digital logics, [8]. The inclusion of FPGA in the redundancy techniques can enhance the time period by 30% and has low area utilization than the advanced methods, [9]. The reduction in the Neutron checking is possible using the FPGA based TMR circuit by 26 times than the conventional circuit, [10]. The power consumption is decreased by 44% for complex digital design when implemented in real applications, [11]. The influence of TMR and its merits in real time usage is minimal in fields such as power converters. The correctness of the not logic is ensured using the tolerable PWM signal that consists of dual redundancy control circuit, [12]. The identification of errors in switches of the power inverter is accomplished by the utilization of redundant algorithm, [13]. The hybridization of the redundancy algorithms can enhance the reliability of the design and in parallel regularization of buck converter device, [14]. The TMR based Digital Pulse Width Modulation exhibits good performance with low power and area utilization, [15].

As technology develops, faults can affect several memory bits because circuitry is spaced closer together on a smaller area. With the decreasing size of technology, there is a greater likelihood of numerous faults occurring, necessitating the correction of multiple errors instead of single error. The proposed method concentrates on the error correction which plays a vital role in the performance of the Modified Hybrid Digital Pulse Width Modulation Generator with the Triple Modular Redundancy algorithm. To analyse the performance of the proposed method, the fault is induced in the MDPWM algorithm and validated for correctness in the output by making use of the majority circuit. The presented method is implemented using the Xilinx FPGA device (Artix-7) and evaluated for performance analysis such as power, area, and delay. Compared with the existing methods, proposed operation consumes low power and covers minimum area and delay.

2 The Proposed Method: Triple Modular Redundancy based Modified Hybrid Digital Pulse Width Modulation

The proposed method includes the fault identification of modified hybrid digital Pulse Width Modulation signals by using the Triple Modular Redundancy is very fast and more accurate as it is can easily identify different types of faults. The fault identification of the proposed method is developed using the structural style of the VHDL code. This section discusses about the internal structure of the MHDPWM and proceeded by the application of the TMR concept in the developed MHDPWM generator.

i)Modified Hybrid Digital Pulse Width Modulation

The Pulse Width Modulation Generator is utilised to control the closed loop converter circuit with the adjustment of duty cycle. The conventional PWM requires a sinusoidal signal overlapped with the high frequency carrier triangular signal for its generation and exhibits demerits such as accuracy in regulation of the converter and delay in time transient response. To overcome these issues, the Digital Pulse Width Modulation is prioritised over the PWM signals. There are basically three types of DPWM namely Counter based DPWM; Delay line based DPWM and Hybrid based DPWM. The CDPWM is developed with the counter circuit, DDPWM is designed using the multiplexer circuit and HDPWM uses both the counter and multiplexer circuit. The drawbacks of the DPWM methods is the time delay presence in the TURN ON and TURN OFF of the Pulse duration of the DPWM signal. This triggers to the development of the Modified DPWM techniques such as Modified CDPWM, Modified DDPWM and Modified HDPWM. Though the Modified CDPWM and Modified DDPWM can be used for the reduction of the TURN ON and TURN OFF delays, in this proposed work, the Hybridization of the MCDPWM is used

for the TURN OFF delay and the MDDPWM is used for the TURN ON delay and thus it is referred as Modified Hybrid DPWM generator.

The MHDPWM is developed with the resolution of 2^{10} bits that consists of two parts as MCDPWM and MDDPWM with resolution of 2^5 bits each. The MCDPWM has the counter with the resolution of 2^{10}(0 to 1023 bits) and to generate the inputs of the SR-FF, the DC and the counter value overlapped is taken as SET_C and the initial 0 value is taken as $RESET1_C$. Concurrently, at the enable of the SET_C signal, the reverse counter (UP counter) is enabled to overlap with the same DC value to give the second $RESET2_C$ signal. To consider both the $RESET_C$ signal events, the OR gate is utilized in the generation of $RESET_C$. By considering all the $RESET_C$ events from the MCDPWM, the TURN-OFF Delay is reduced. The second block in the MHDPWM is the MDDPWM circuit that consist of 1024:1 Multiplexer for the select line has 10 bit in design resolution is connected to the ring counter with the 1024 D-FFs. The duty cycle value is considered as 2^{10} bits of resolution for the select line of the primary multiplexer and the 1-Dutycycle with the resolution of 2^{10} bits is given to the secondary multiplexer to generate the $RESET_D$ and $SET1_D$ respectively. The $SET2_D$ is obtained from the F_{clk} signal and logical OR gate is used with the $SET1_D$ to produce the SET_D. The overall SET is derived by the logical OR operation of the SET_D and SET_C along with the overall RESET as logical OR of the $RESET_C$ and $RESET_D$. The MDDPWM is used to reduce the TURN ON delay in the DPWM generated signals. Figure 1 depicts the block diagram of the proposed MHDPWM circuits with the resolution of 2^{10} bits.

ii) Triple Modular Redundancy

Triple Module Redundancy (TMR), [3], is a very common fault tolerance technique. This technique can be used to protect circuits against radiation effects. The principle is: triplicate the hardware and add a voter in the outputs. In this paper we are only using TMR in memory elements. All memorisation elements are tripled and its respective outputs are connected to a voter. The voter will select the output of the majority of the components. So, if one component fails, the error will not be reflected in the voter output.

The Triple Modular Redundancy, quite common fault tolerant technique used to defend the circuit in opposition to radiation effects. Redundancy is one of the method in the generation and design of digital pulse width modulation and it falls into three major classification namely modified counter based digital pulse width modulation, modified delay line based digital pulse width modulation and modified hybrid digital pulse width modulation. TMR is used to find the majority out of the three outputs are correct. The TMR is based on the concept of chronometer where the best out of the three executed outputs are valid or not. To validate the majority of the output, the majority gate is utilised with the majority number of 1's in the input sequence. The TMR is fault tolerance circuit that can be extend to N- number say N-Modular Redundancy (NMR). The demerit of the redundancy form is the area occupancy in real time due to the repetitive blocks of the circuit under test. The usage of redundancy form of validation is acceptable with the software concepts as area occupancy is not an issue in virtual mode.

iii) Triple Modular Redundancy based Modified Hybrid Digital Pulse Width Modulation

The proposed method includes the design of fault identification in the Modified hybrid Digital Pulse Width Modulation generator using the TMR methodology. The TMR has thrice the circuitry of the MHDPWM that is under testing and checks for errors by comparing the majority of correctness in the output. The three outputs of the MHDPWM is indicate the fault by utilising the voter element in the TMR algorithm. For example, if the erroneous signal is present in any one of the three outputs, then the corrected value is considered using the concept of majority outputs as correct and error free. Overall, the proposed method recognises the fault free output from the three MHDPWM under the TMR structure of validation. Figure 2 shows the block diagram of the proposed Fault identification using the TMR for MHDWPM. The 2^{10} bits of duty value is given as input to the MHDPWM signals from the TMR with similar frequency to identify the erroneous output among the three signals.

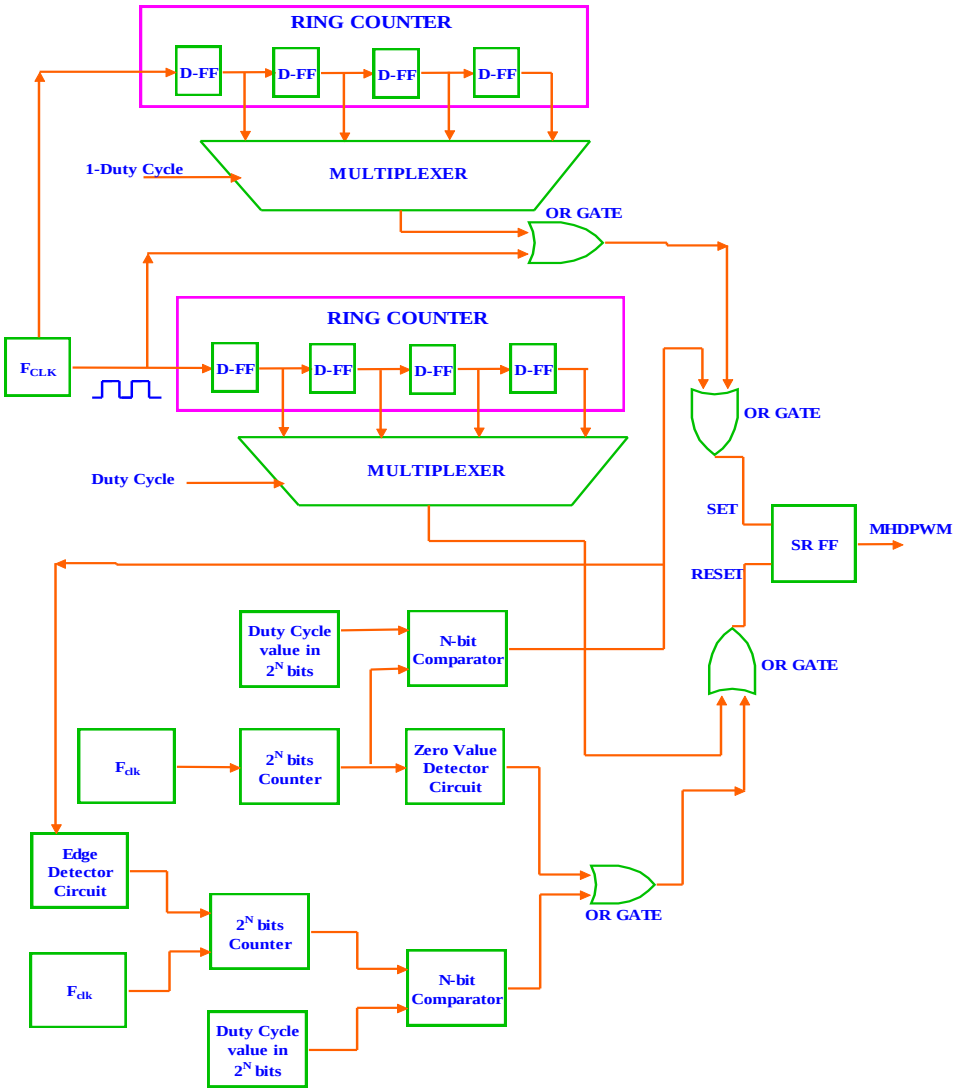

Fig. 1: Block Diagram of the Modified Hybrid Digital Pulse Width Modulation

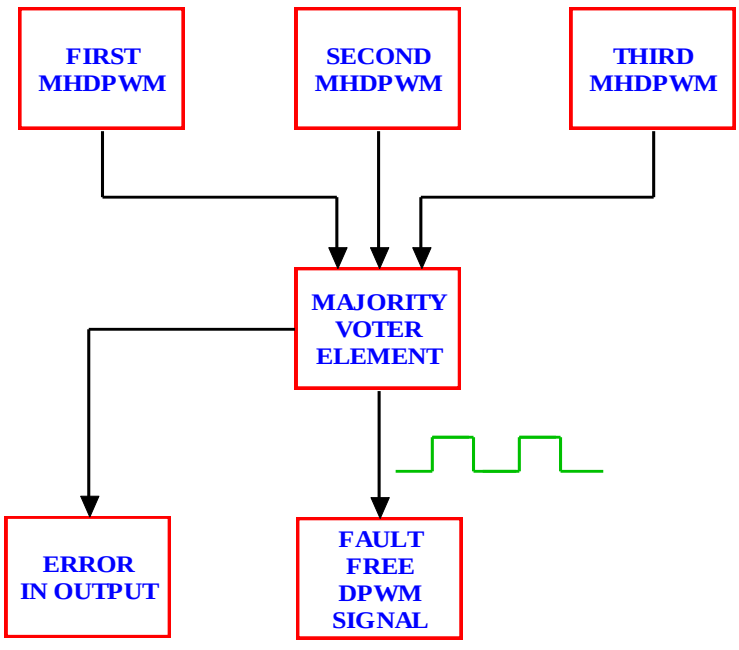

Fig. 2: Block Diagram of the proposed Tripler Modular Redundancy for the MHDPWM

3 Results and Discussion

The Proposed TMR based MHDPWM is developed using the VHDL code and simulated using the MODELSIM software. The proposed design includes in the generation of three MHDPWM for the identification of errors. The Majority voter element is utilised to produce the majority (at least 2 out of 3 outputs) to be the same after execution. The simulation output of the proposed method is depicted in the Figure 3. From the simulation output it is observed that the suggested approach detects the three MHDPWM's fault-free output to determine which of the three signals is in correct. Figure 4 shows the RTL schematic which is an intermediate representation of logic circuits that can carry out a specific micro-operation and transmit the results to the same or different registers of the proposed method using the Xilinx Vivado Tool with the selected Artix-7 FPGA (Package: xc7a100tcsg324).

RTL Schematic for the internal block for the individual MHDPWM design which verifies the functionality of each RTL module at any time is given in the Figure 5. The elaborated schematic diagram can be attained by implementing the synthesized code for the proposed method is shown in Figure 6. The power report which can be generated after the post synthesized which dissipates 2.597W of Dynamic Power and 96% as on chip power. Also 0.884W, 0.700W, 1.013W power dissipates for Signals, Logic, I/O respectively as given in Figure 7. As a consequence, implementation can be executed using Artix-7 FPGA device which dissipates the Dynamic power of 2.031W and 95 % as on-chip power as given in Figure 8. Also 0.430W, 0.681W, 0.920 W power dissipates for Signals, Logic, I/O respectively. The developed VHDL code for the proposed method is converted to the IC Layout using the Cadence Tool which is used to design, verify and implement cutting edge VLSI digital circuits.

The conversion process requires three different tools to be utilized namely INCISIVE, GENUS and INNOVUS. Figure 9 and Figure 10 display the RTL schematic for the proposed method using the GENUS tool and INNOVUS tool subsequently which delivers the detailed report of the proposed Triple Modular Redundancy for MHDPWM. The parametric analysis of Power and Timing report for the proposed method are given in Table 1 and Table 2 respectively. The Total power dissipation is approximately 1.997W with the internal power of 1.8856W which provides 94% from total power, leakage power of 0.03838W which produce 3.66% from total power and switching power of 0.07326W which produce 1.92 % from total power. It can be seen from Table 1 sequential circuits can render internal power of 1.802W, switching power of 0.0201W and leakage power of 0.0276W respectively. Similarly combinational circuits render power of 0.083W as internal power, 0.0530W as switching power and 0.0106W as leakage power in due course. Therefore, the proposed TMR based MHDPWM design dissipates low power of 1.997W in Cadence tool compared with 2.031W in Xilinx tool. It is noticed from Table 2 that the time design summary shows the estimated total of WNS(ns) of -0.222 and TNS (ns) of -0.730 respectively for the proposed system.

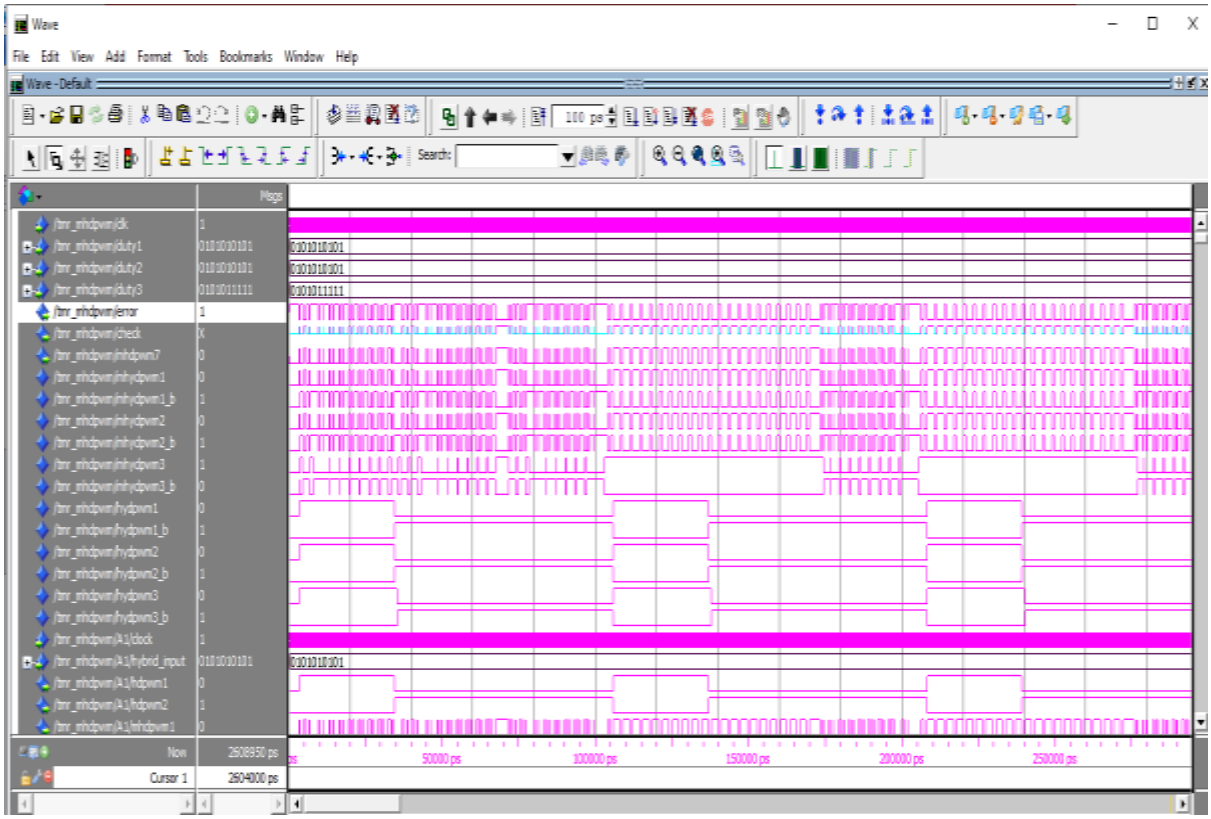

Fig. 3: Simulation output of the proposed TMR based MHDPWM design

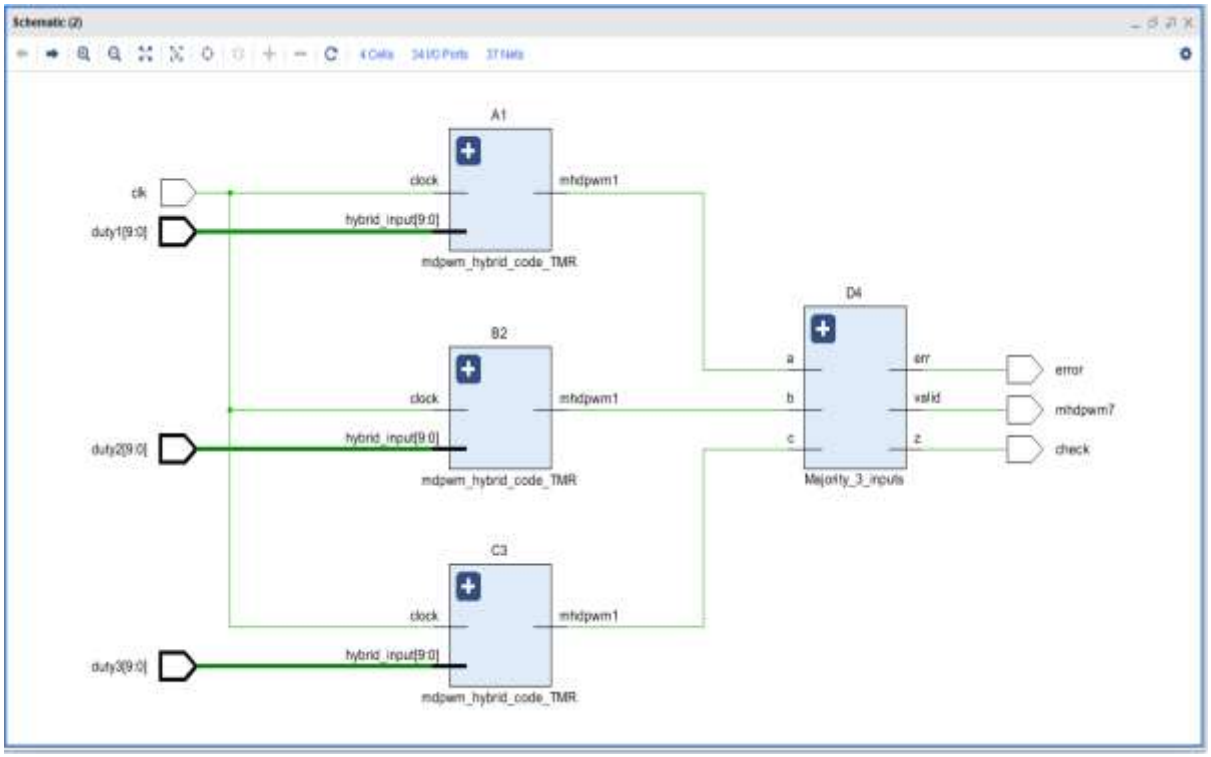

Fig. 4: RTL Schematic for the proposed TMR based MHDPWM

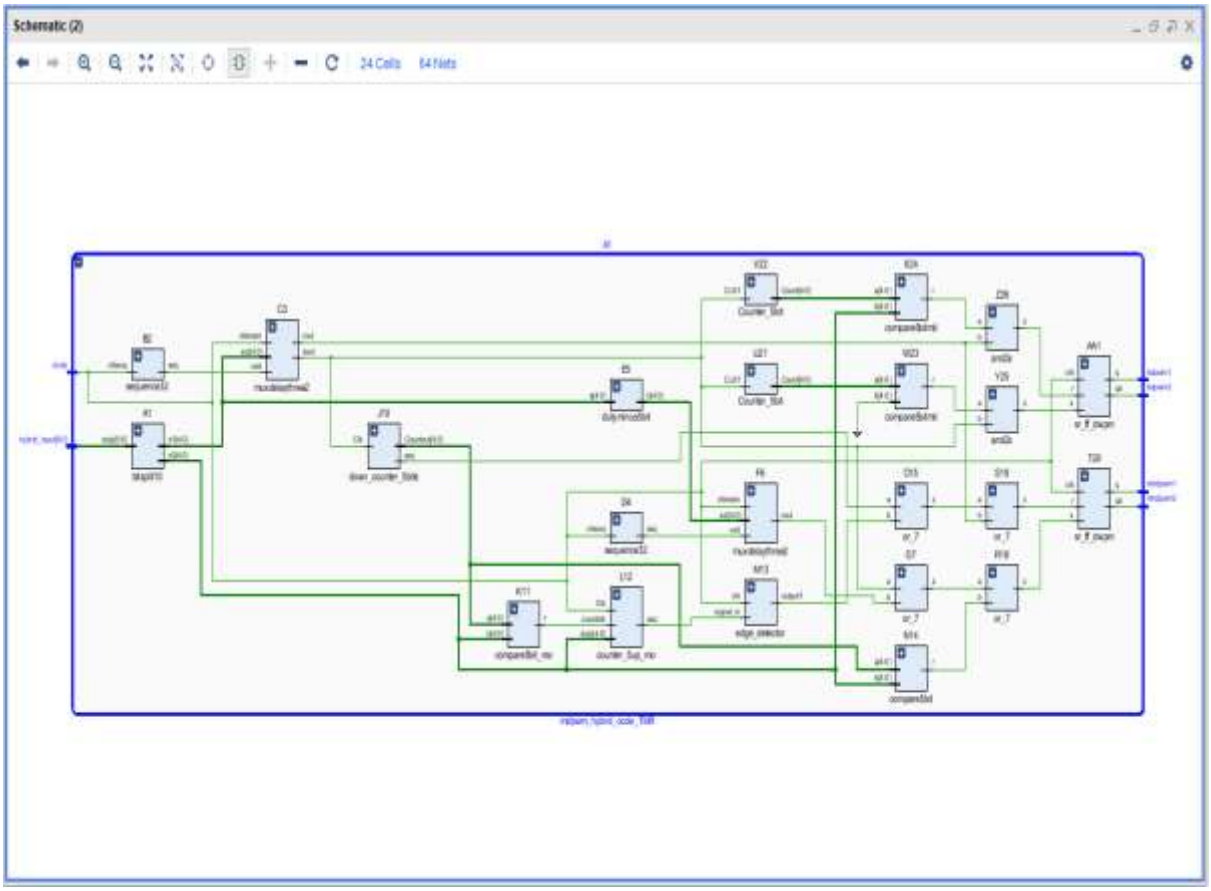

Fig. 5: RTL Schematic for the internal blocks of the MHDPWM design

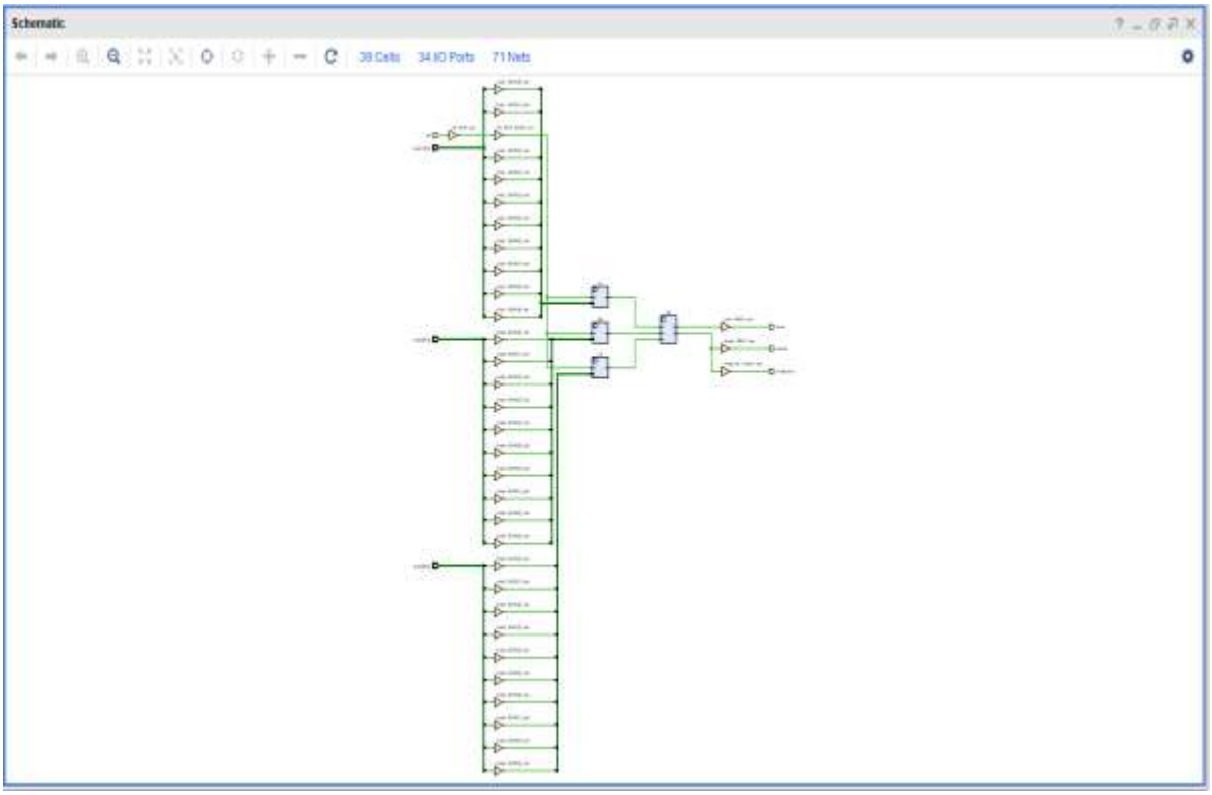

Fig. 6: Elaborated Design for the proposed TMR based MHDPWM

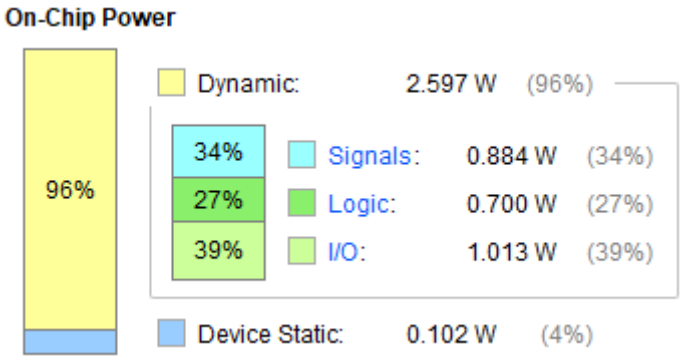

Fig. 7: Post-synthesized Power Report for the proposed TMR based MHDPWM

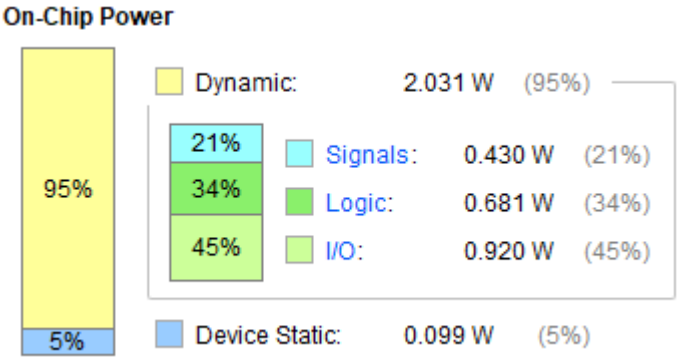

Fig. 8: Post-Implementation Power Report for the proposed TMR based MHDPWM

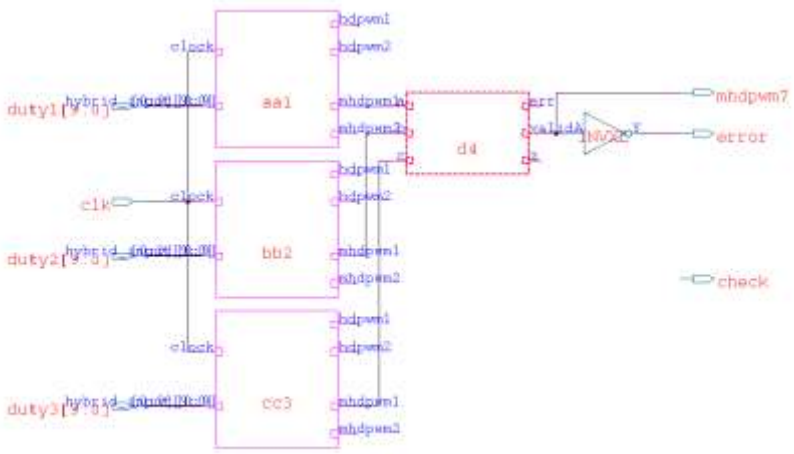

Fig. 9: RTL Schematic for the proposed TMR based MHDPWM using the GENUS-Cadence Tool

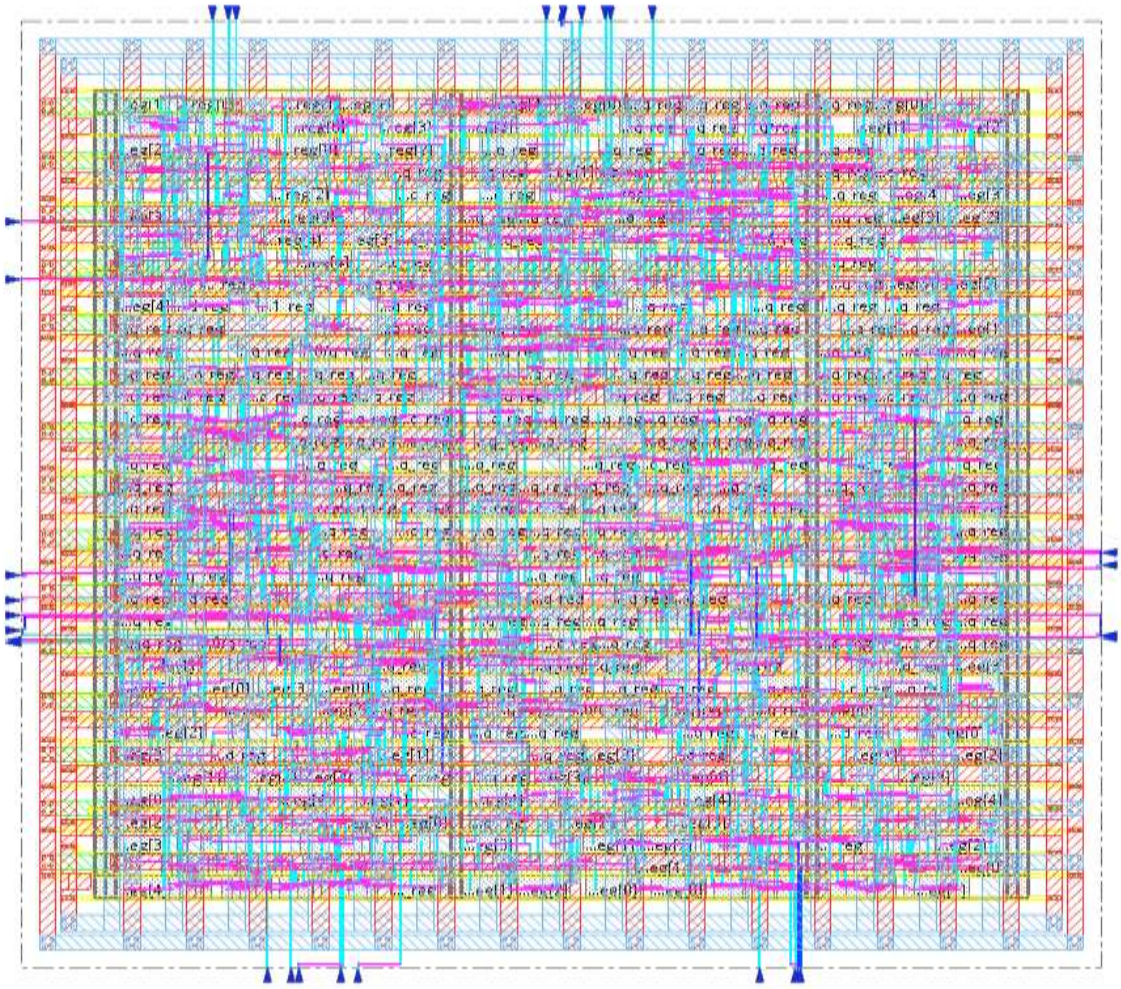

Fig. 10: Layout for the proposedTMR based MHDPWM using the INNOVUS-Cadence Tool

Table 1. Power Analysis Report for the proposed TMR based MHDPWM using the GENUS Cadence Tool

Total Power

Total Internal Power:	1.88557076	94.4102%
Total Switching Power:	0.07326021	3.6681%
Total Leakage Power:	0.03837885	1.9216%
Total Power:	1.99720982	

Group	Internal Power	Switching Power	Leakage Power	Total Power	Percentage (%)
Sequential	1.802	0.02018	0.02769	1.85	92.63
Macro	0	0	0	0	0
IO	0	0	0	0	0
Combinational	0.08342	0.05308	0.01069	0.1472	7.37
Clock (Combinational)	0	0	0	0	0
Clock (Sequential)	0	0	0	0	0
Total	1.886	0.07326	0.03838	1.997	100

Table 2. Power Analysis Report for the proposed TMR based MHDPWM using the GENUS Cadence Tool

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------------------------------------------------------
          timeDesign Summary
------------------------------------------------------

Setup views included:
 Worst

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.222  |  0.072  | -0.222  |
|           TNS (ns):| -0.730  |  0.000  | -0.730  |
|    Violating Paths:|    6    |    0    |    6    |
|          All Paths:|   252   |   252   |   21    |
+--------------------+---------+---------+---------+
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4 Conclusion

The proposed TMR based Modified Hybrid Digital Pulse Width Modulation has been developed using the VHDL code and verified successfully. The proposed method could be utilized in the identification of hardware faults in the DPWM signals in real time. For the purpose of validation, the Xilinx Artix 7 FPGA board has proven to be feasible and analyzed for the parametric evaluation of Power, area and delay. The proposed method dissipated low power of 2.031W in Xilinx tool and 1.997W in Cadence tool. The IC layout for the proposed method has been developed using the cadence tool and could be processed for the physical fabrication. Future work could be directed towards the Machine Learning to model the power converters fused with the Triplicate Modular Redundancy to analyze the performance and identify multiple faults in the power converter control methodologies.

References:

[1] Fatemeh Sadat Mireshghallah, Mohammad Bakhshalipour, Mohammad Sadrosadati, and Hamid Sarbazi-Azad, "Energy-Efficient Permanent Fault Tolerance in Hard Real-Time Systems", in *IEEE Transactions on Computers*, Vol. 68, No: 10, pp.1539-1545, October 2019, https://doi.org/10.1109/TC.2019.2912164.

[2] Haomiao Su, Tiejun Lu, Changlei Feng, Lei Chen, "Triple module redundancy reliability framework design based on heterogeneous multi-core processor", in *Procedia Computer Science*, Vol.183, pp.504–511, 2021, https://doi.org/10.1016/j.procs.2021.02.090.

[3] Aibin Yan, Zhelong Xu, Kang Yang, Jie Cui, Zhengfeng Huang, Patrick Girard, Xiaoqing Wen, "A Novel Low-Cost TMR-Without-Voter Based HIS-Insensitive and MNU-Tolerant Latch Design for Aerospace Applications", *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 56, Issue 4, August 2020, pp.2666-2676 https://doi.org/10.1109/TAES.2019.2951186.

[4] Tooba Arifeen, Abdus Sami Hassan and Jeong-A Lee, "A Fault Tolerant Voter for Approximate Triple Modular Redundancy", in *Electronics*, Vol. 8, No. 3, 332, https://doi.org/10.3390/electronics8030332.

[5] Tooba Arifeen, Abdus Sami Hassan, and Jeong-A Lee, "Approximate Triple Modular Redundancy: A Survey", in *IEEE Access*, Vol. 8, pp: 139851- 1398567, 2020, https://doi.org/10.1109/ACCESS.2020.3012673.

[6] Yao Rui, Chen Qinqin, Li Zengwu, Sun Yanmei, "Multi-objective evolutionary design of selective triple modular redundancy systems against SEUs", *Chinese Journal of Aeronautics*, Vol. 28, Issue 3, June 2015, pp.804-813, https://doi.org/10.1016/j.cja.2015.03.005.

[7] Mohammed Hadifur Rahman, Shahida Rafique, Mohammad Shafiul Alam, "A Fault Tolerant Voter Circuit for Triple Modular Redundant System" in *Journal of Electrical and Electronic Engineering*, Vol. 5, No. 5, pp. 156-166, 2017, https://doi.org/10.11648/j.jeee.20170505.11.

[8] Shubham C. Anjankara, Dr. Mahesh T. Kolteb, Ajinkya Pundc, Pratiksha Kolted, Ankita Kumare, Pranav Mankarf, Kunal Ambhore, "FPGA Based Multiple Fault Tolerant and Recoverable Technique Using Triple Modular Redundancy", in *Procedia Computer Science*, Vol. 79, pp.827-834, 2016, https://doi.org/10.1016/j.procs.2016.03.109.

[9] Solomon Banteywalu, Baseem Khan, Valentijn De Smedt and Paul Leroux, "A Novel Modular Radiation Hardening

Approach Applied to a Synchronous Buck Converter", in Electronics, Vol. 8, No. 5, 513; 2019, https://doi.org/10.3390/electronics8050513.

[10] Matthew J. Cannon, Andrew M. Keller, Corbin A. Thurlow, Andres Perez-Celis and Michael J. Wirthlin, "Improving the Reliability of TMR with Nontriplicated I/O on SRAM FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 67, No. 1, pp.312-320, January 2020, https://doi.org/10.1109/TNS.2019.2956473.

[11] Solomon Mamo Banteywalu, Getachew Bekele, Baseem Khan, Valentijn De Smedt and Paul Leroux, "A High-Reliability Redundancy Scheme for Design of Radiation-Tolerant Half-Duty Limited DC-DC Converters", in *Electronics*, Vol. 10, No. 10, 1146, 2021, https://doi.org/10.3390/electronics10101146

[12] F. Troni, C. Concari, A. Toscani, G. Buticchi, G. Franceschini, "Fault tolerant PWM generation with doubleredundant logic" in *WIT Transactions on Engineering Sciences*, Vol. 87, pp.495-502, 2014, http://dx.doi.org/10.2495/AMITP20130581.

[13] Soban Ahmed, Arslan Ahmed Amin, Zaeema Wajid and Faizan Ahmad, "Reliable speed control of a permanent magnet DC motor using fault-tolerant H-bridge", in *Advances in Mechanical Engineering*, Vol. 12, No. 10, pp:1–14, 2020, https://doi.org/10.1177/1687814020970311.

[14] Jeffrey Prinzie, Karel Appels and Szymon Kulis, "Optimal Physical Implementation of Radiation Tolerant High-Speed Digital Integrated Circuits in Deep-Submicron Technologies" in *Electronics*, Vol. 8, No. 4, 432, April 2019, https://doi.org/10.3390/electronics8040432.

[15] Joseph Anthony Prathap, Maruthi Pottella, Srikanth Thammisetti, Sainath Rachakonda, "FPGA based design of Triple Modular Redundancy for Hybrid Digital Pulse Width Modulation Generator", in *Management Innovation and Technologies Magazine*, Vol. 11, No. 2, pp.2249-2259, May 2021, http://dx.doi.org/10.47059/revistageintec.v11i2.1885.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

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Conflict of Interest

The authors have no conflicts of interest to declare.