A Fast Transient, 24 mA Switched Capacitor Boost Regulator in 40 nm CMOS Technology

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Abstract: - This work presents a fast transient boost converter in 40nm CMOS technology. The converter is fully integrated and utilizes MOS+ MOM capacitors to minimize the area. The unique pseudo-6-bit Analog to digital converter helps the system achieve its fast trainset load changes. The design also utilizes 32-phases of operation to achieve small ripples though it uses a relatively small output capacitor. The converter generates a 3 V supply from a 1.8 V input and achieves a fast transient response of 1mA to 24mA, and vice versa, in 100 ps with an undershoot and overshoot not exceeding 4% of the regulator's output and ripples less than 40mV peak-to-peak.

Key-Words: - fast transient, boost converter, switched capacitor regulator, integrated capacitors, power management

Received: April 14, 2022. Revised: February 21, 2023. Accepted: March 15, 2023. Published: April 25, 2023.

1 Introduction

Fully integrated power management has become a very important topic for modern System on Chips (SOCs). Many SOCs use different voltage rails for different blocks. Previously Power Monument Units (PMUs) were completely external chips that took up precious space on the Printed Circuit Board (PCB). As technology advanced, designers started integrating PMUs into the SOCs, but leaving the bulky capacitors and inductors on the PCB. Having those "external components" on the PCB was still waste in the area and accessing those "external components" needed dedicated pads on the chip. Moving away from using any "external components" will save both PCB area and cost by reducing the pin count or reusing the free pin in new functionality in the SOC.

Linear Drop-Out regulators (LDOs) are the most popular power management system used in SOCs, [1], [2]. LDOs can achieve fast transient responses without using any external capacitors. Unfortunately, LDOs operation is limited to only Buck operation, where the needed rails are lower than the input rail. To have a boost operation, the output rail is higher than the input rail. We can only use switched regulators. There are 3 kinds of switched regulators: 1) Inductor-based regulators, 2) capacitor-based regulators, and 3) hybrid regulators which use both inductors and capacitors for the regulation.

Inductor-based regulators and hybrid regulators use inductors which are usually an external bulky component that takes up a large area on the PCB. On the other hand, capacitor-based regulators, also known as Switched-capacitor) SC regulators can be fully integrated and only use capacitors available in Complementary Metal Oxide Semiconductor (CMOS) technology.

SC regulators typically have two types of capacitors, a flying capacitor and an output capacitor as shown in Figure 1. Flying and output capacitors can be external capacitors, [3], where the capacitors are on the PCB, and other designs can utilize integrated capacitors and eliminate the need for an external component, [4], [5], [6]. Usually, SC regulators use very large capacitors, in the range of nFs, which makes their area very large. Usually, they utilize both MOS + MOM capacitors, [7], and in other designs, they add MIM capacitors as well, [6]. MIM capacitors are not available in all technologies and when available, it is usually through an extra mask which increases the cost.

The next section will discuss the proposed SC boost regulator and its circuits, followed by section 3 which will present the simulation results and compare our design to the state of the art. This is followed by the conclusion of the work in section 4.

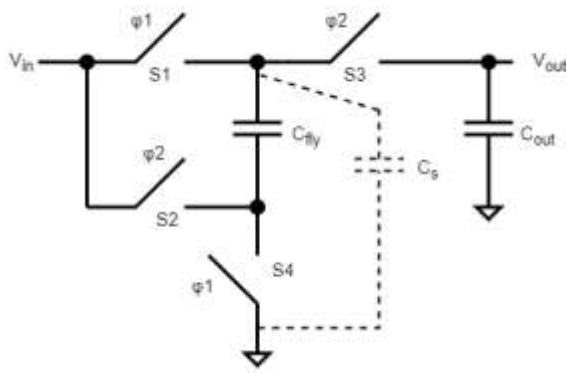


Fig. 1. SC doubler circuit

2 Circuit Description

The proposed charge pump-based SC regulator is shown in Figure 2 which consists of 5 groups of charge pumps. Each group consists of 32 charge pumps, each operated by two complementary phases out of the 32 phases used in the system. The system also utilizes a pseudo-6-bit analog to digital converter (ADC) which helps the system increase its transient response by detecting the droop on the output voltage, using a resistor divider from the output, resulting from the increased load which prompts the system to increase the number of engaged charge pumps to reduce the drop. When the system detects a large drop, this signals a large load, and extra charge pumps are engaged to restore the output level. The number of charge pumps engaged is dependent on the load. The system also uses a small 120pF capacitor to reduce the ripples. 1 group of the charge pumps is Always ON (AON) while the other 4 groups are controlled by the ADC. The following subsections will go through the system blocks in more detail.

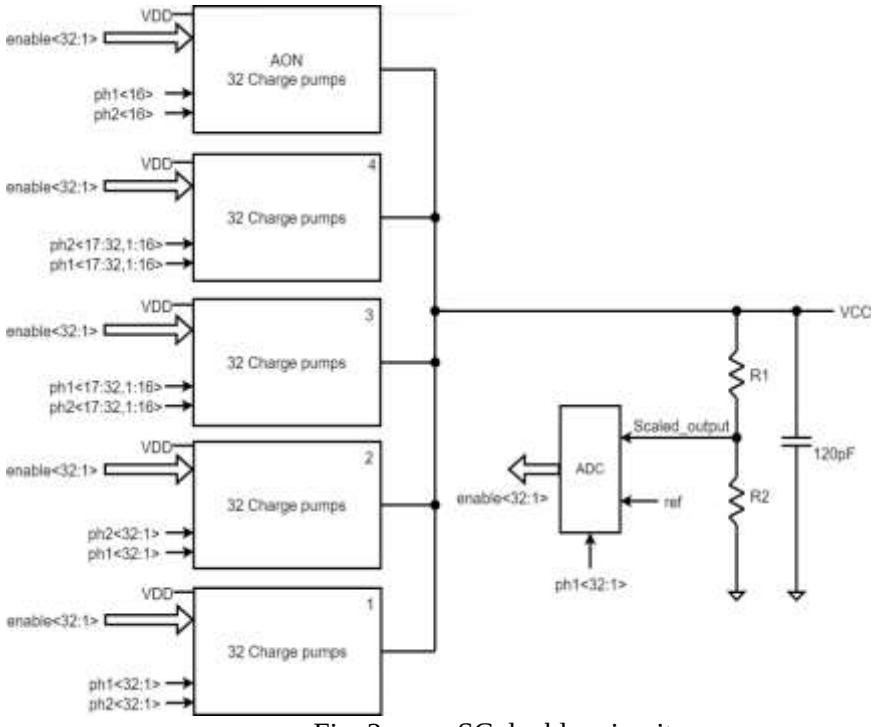


Fig. 2. SC doubler circuit

2.1 Charge Pump

As mentioned before, each group consists of 32 charge pumps connected in parallel. A Dickson charge pump, [8], is utilized in the system. A simple Dickson charge pump also called a doubler, is shown in Figure 1. The doubler utilizes one flying cap and one output cap, plus 4 switches. During φ1, the flying capacitor (C_{fly}) is connected between V_{in} and the ground. During φ2, the capacitor is connected between V_{in} and V_{out} such that the bottom plate of the capacitor is connected to V_{in}. Since the voltage drop on the flying capacitor (C_{fly}) is Vin, V_{out} is "pumped" to $2*V_{in}$ to maintain the voltage on the capacitor. The output can be described using the following equation:

$$V_{out} = \left(\frac{N}{1+\alpha} + 1\right) * V_{in} - R_{out} * I_{load} \quad (1)$$

Where V_{out} is the charge pump output, N is the number of stages, α is the stray capacitance to the total capacitance ratio, Vin is the charge pump input, R_{out} is the output resistance of the charge pump and I_{load} is the load current of the charge pump. For a single stage and zero load or sufficiently light loads, V_{out} (maximum output value without regulation) tends to be limited by the stray capacitance to the total capacitance ratio.

The charge pump circuit is based on the work of [9], and is described in [10], with the schematic shown in Figure 3. The capacitors Cm1, Cm2, Cl1, Cl2, Cl3, and Cl4 are implemented using MOS capacitors (specifically PMOS) but drawn as a simple capacitor for simplicity. Output capacitor utilizes MOS +MOM configuration to increase the capacitor density. When PU is high and PUz is low (the circuit is enabled), Cm1 and Cm2, which are the main charge pump capacitors, are charged through MN1 and MN2. The toggling of Phi1 and Phi2 makes the nodes VCC1 and VCC2 switch between VDD and 2*VDD. Cl1 and Cl2 (as well as Cl3 and Cl4) act as level translators that ensure MN3-MN5 switches between VDD and 2*VDD. The extra logic created by the NAND ensures MN3-MN5 are switched off before Mp1-MP4 are turned on. VCC is connected to VCC1 and VCC2 when they are charged to 2*VDD in a differential operation. MN6/MN7 are used to turn the charge pump off by discharging all the capacitors (Cm1, Cm2, Cl1, Cl2, Cl3, and Cl4).

For reliability concerns, only 3.3 V devices are used (2.5 V devices with 3.3 V overdrive) in the design.

2.2 Pseudo-ADC

The resistor divider generates a scaled version of the output (half the output is used in the design) and feeds it to the pseudo-6-bit ADC. The ADC compares the scaled version to its reference voltage and based on the digital code generated, the system can increase or decrease the number of charge pumps needed by the system. When the output load starts increasing, the output voltage will start to decrease. This decrease will be detected by the ADC and extra charge pumps will be enabled to support the increased load. Because of the utilization of 32 phases, the ADC can enable extra charge pumps needed resulting in a fast transient response.

The schematic of the pseudo-ADC is shown in Figure 4. The resistor ladder is used to generate six voltage levels to compare the output voltage. The reference current comes from a Bandgap (BG) and the ladder must use the same unit resistor in the BG. Some programmability is added to change the output voltage if needed. The ADC also has 32 dynamic comparators, shown in Figure 5, [11]. Each comparator uses 1 phase of the 32 phases used by the system. The exact phases and references of the 32 comparators are listed in Table 1.

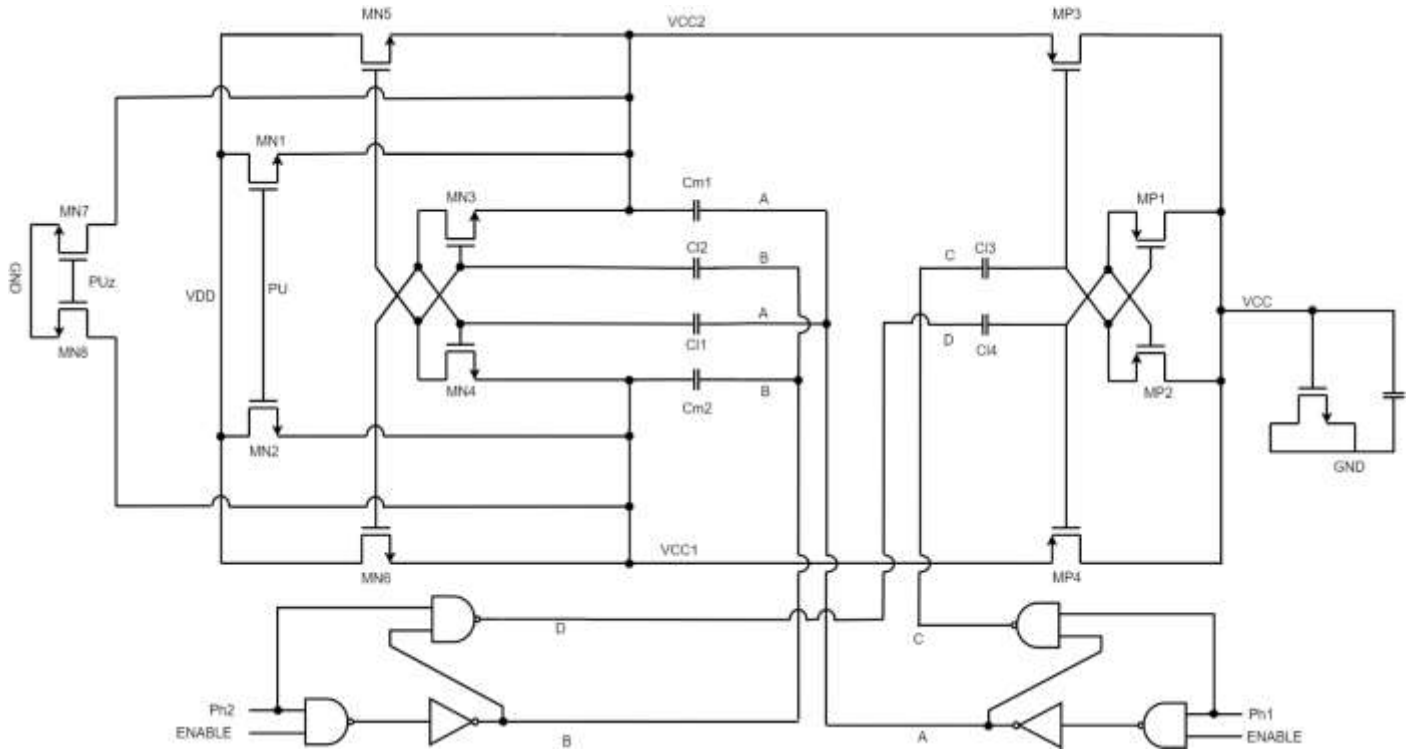


Fig. 3. SC doubler circuit

When CLK is high, MN1 is turned on while MP1 and MP2 are turned off. If Vinp is higher than Vinn, this will cause a higher current to pass through M2 than M3. This will make the ind voltage go lower than midp. MN4/MP3 and MN5/MP4 act as cross-coupled inverters. When the ind goes low, MN4 sees a higher VGS driving outn to zero, which drives outp to supply.

Table 1. Phase distribution

Phases	***# of Comparators***	***Reference Used***
Phase 16	1	vref
Phase 32	1	vref – 1*lsb
Phases 8 and 24	2(1 for each phase)	vref – 2*lsb
Phases 4, 12, 20, and 28	4(1 for each phase)	vref – 4*lsb
Phases 2, 6, 10, 14, 18, 22, 26 and 30	8(1 for each phase)	vref – 8*lsb
All odd phases (1, 3, 5, …, 31)	16(1 for each phase)	Vref – 16*lsb

Since the cross-coupled back-to-back inverters act as a positive feedback loop, a reset for the comparator is needed every clock cycle, which happens when the CLK is low enabling MP1 and MP2, which pulls outp and outn to the supply. An SR latch ensures that the comparator maintains its output value without being reset.

3 Results

System simulation was done using Spectre and used a 32-phase 200 MHz clock. Figure 6(a) shows the transient response of the system due to a fast load change from 0 to 24 mA in 100ps. The results show that the system exhibits a very good response with a change of not more than 4% of the output. Figure 6(b) shows ripples across different loads highlighting that the output sees only 40 mV of voltage ripples across different loads.

There is the classic efficiency vs frequency vs ripples trade-off. As we increase the frequency of operation, the efficiency will decrease but the ripples and system performance will increase. Figure 7 shows the efficiency of the converter using different frequencies and ripples vs load across different frequencies. The system achieves 47.5% peak efficiency (at a maximum load of 24 mA) using a 200 MHz clock with maximum ripples across different loads of 39 mv. The efficiency is improved to 60.7% when using 100MHz but at the expense of increased voltage ripples. Voltage ripples reach a maximum of 89 mV across different loads when using 100MHz.

A new Figure-of-Merits (FOM) was developed in [10], that compares the transient response of SC regulators. The FOM is shown in the equation below:

$$FOM = \left(\frac{Tr * C * \Delta Vout}{Imax * npeak}\right) * 1E^{15} \quad (2)$$

Where Tr is the response time, C is C_{FLY} + C_{OUT}, ΔVout is the change in output due to the load change, ηpeak the peak efficiency, and Imax is the specified max current for the regulator. The scaling factor, 1E15, is to make the number easily readable. In this FOM, the smaller the number, the better. Table 2 compares the performance of the proposed SC boost regulator with the state-of-the-art literature.

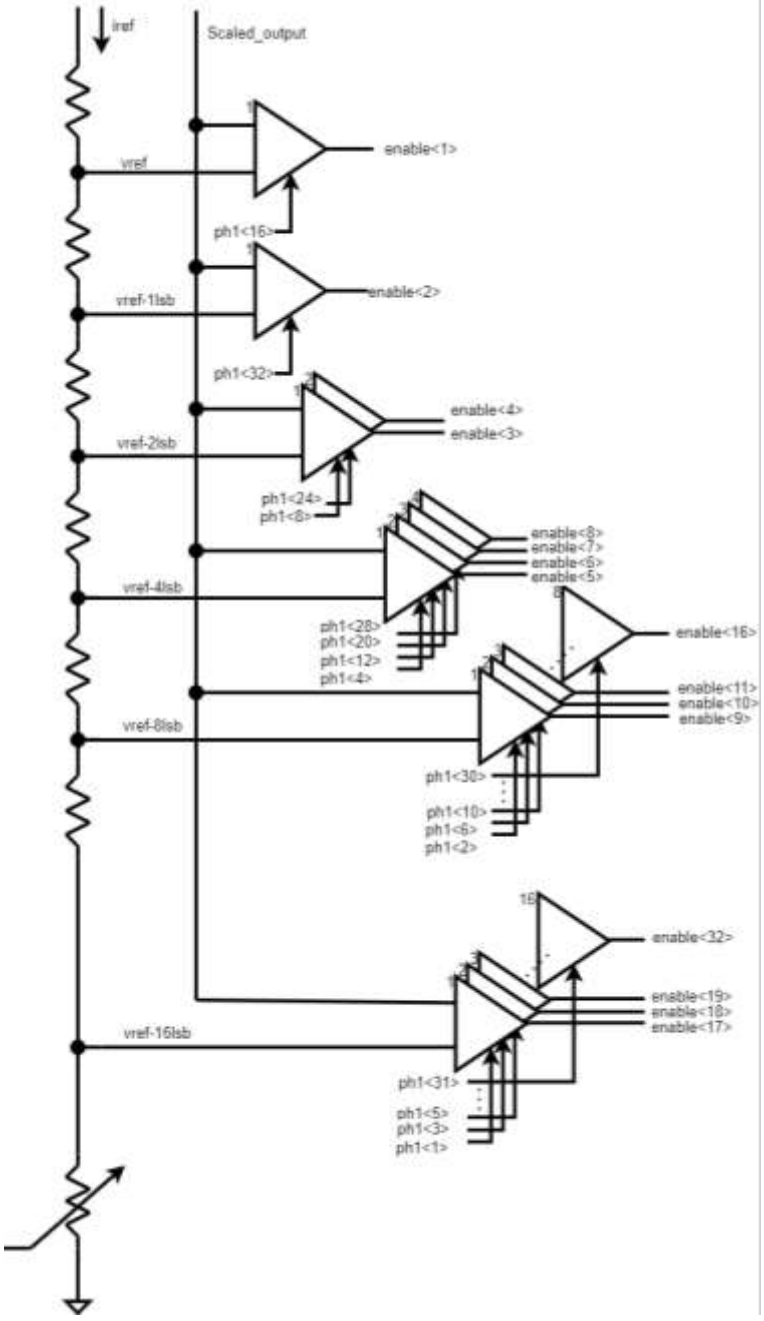


Fig. 4. Pseudo-ADC schematic

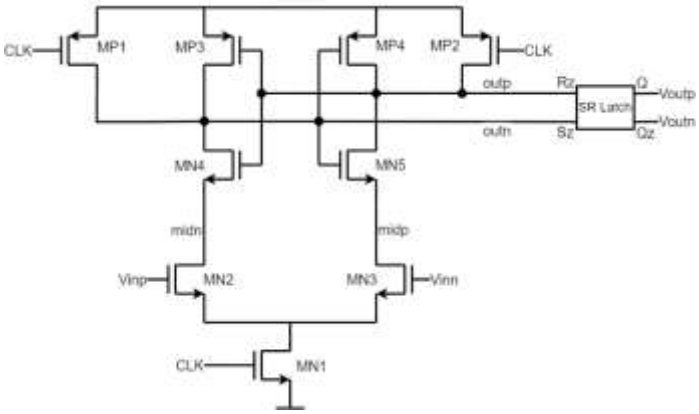
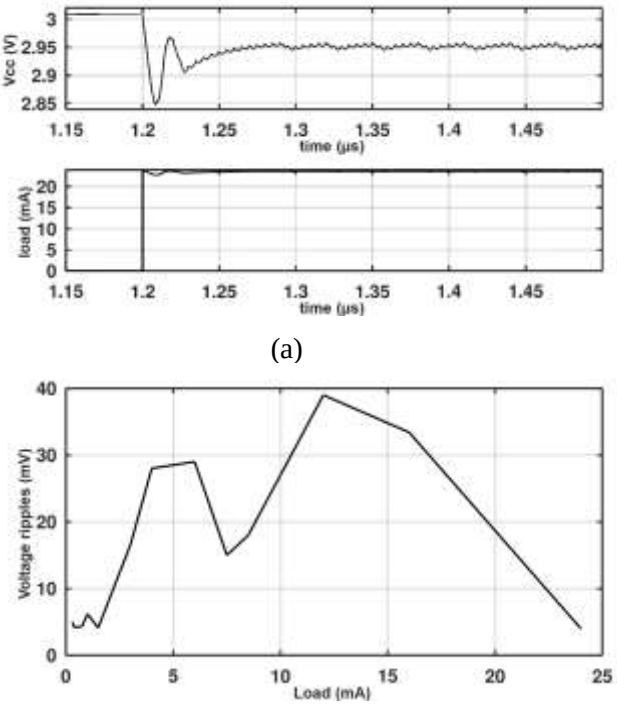


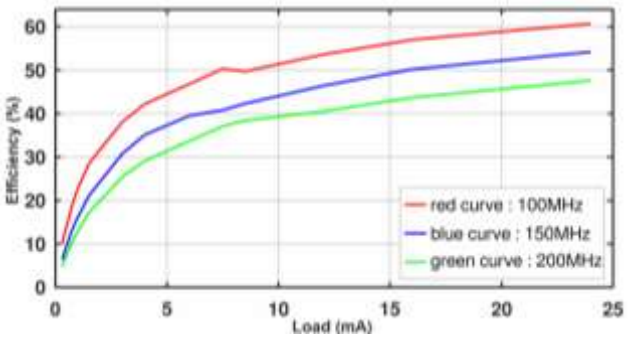
Fig. 5. Comparator schematic



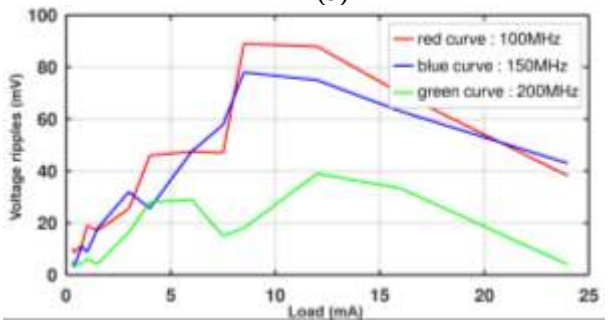
(a)

(b)

Fig. 6. (a) System's transient response to a load change from 0 to 24 mA in 100 ps, (b) Voltage ripples Vs. load



(a)



(b)

Fig. 7. (a) System's efficiency across different loads using different frequencies, (b) Voltage ripples across different loads using different frequencies

Table 2. Comparison between this work and SC converters in literature

	[12]	[13]	[14]	[15]	[16]	[17]	This work
Input Voltage (V)	2.5	0.35 – 0.6	1	1.8 - 5	0.25-1	1-4	1.8
Output Voltage (V)	1	0.86 – 1.8	1.2 – 2.4	3.3	1	1,1.8	3
Type	Buck + LDO	2 stage Boost	Reconfigurable Step-up	Reconfigurable Buck-Boost	Reconfigurable Boost	Reconfigurable Buck-Boost	1:2 charge pump
Number of phases	18	1	4	1	2	2	32
Maximum Load current (mA)	31	0.35	1	10	20.1	10	24
Switching frequency (MHz)	90	0.4 (2)	50-250	0.1	40 (8)	1	200
Flying capacitor size(nF)	0.54	- (3)	N/R (4)	1000	~3	3000	0.942
Output capacitor size(nF)	0.26	4.05(3)	N/R (4)	1000	N/R (4), off-chip	1000	1
Technology(nm)	65	180	28 FDSOI	350	65	180	45
Results	measured	measured	measured	measured	measured	measured	simulated
Output ripple (%) ($\Delta V_{ripple}/V_{out}$)(1)	2	1	N/R (4)	1.5	7.6	>0.1	>0.4
Undershoot (%) ($\Delta V/V_{out}$)(5)	19.5	N/R (4)	N/R (4)	6	N/R (4)	N/R (4)	4
Peak efficiency (%)	76.2	75.8	88	70	72 (9)	77.4	46(200MHz) / 60.6(100MH)
FOM	3.12	N/A (7)	N/A (7)	10E6 (6)	N/A (7)	N/A (7)	2.27

(1) ΔV_{ripple} is the output ripples magnitude, and V_{out} is the output voltage of the charge pump.
(2) Estimated from Figures.
(3) Total capacitance (C_{FLY} + C_{OUT}) reported.
(4) N/R: not reported
(5) ΔV is the output undershoot magnitude, and V_{out} is the output voltage of the charge pump.
(6) The number is huge as it uses two external 1uF capacitors
(7) Can not be calculated due to un-reported parameters

4 Conclusion

A fast transient, 24 mA fully integrated boost converter is presented. The use of the pseudo-ADC and the 32-phase high-frequency clock operation makes the converter able to respond to very fast transients up to 24 mA in100ps with only 4% change in the output voltage as well as a maximum of 40 mV voltage ripples across different loads.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

The authors have no conflict of interest to declare