Design of Monolithic RF CMOS Sub-mW Self-Oscillating-Mixers

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Abstract: —In this paper, different topologies of RF self-oscillating mixers (SOM), stacking the voltage controlled oscillator (VCO) and the mixer on top of each other, are assessed. Their design considerations to address sub-mW operation suitable to ultra-low power applications are presented. Two configurations of SOM circuits are implemented in 130nm CMOS technology. The obtained results are presented and performances in terms of gain, noise, linearity, area, power consumption and stability over process and mismatch are compared and discussed.

Keywords: - RF; SOM; LC-VCO; mixer; CMOS.

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1. Introduction

The emergence of the Internet of Things (IoT) leads to stringent requirements on the power consumption of devices. The energy budget is restricted because of the limited battery lifetime and the unstable output power of energy harvesters. This rapidly became a key issue driving the implementation of ultra-low power (ULP) radiofrequency (RF) integrated circuits (IC). To reduce power consumption, several techniques are used in RF design: lowering either the supply voltage or the current. First, low voltage operation can be achieved when RF front-ends in transceivers use folded topologies. The stacked circuit is converted to a cascaded one and then voltage and power consumption are reduced [1]. Besides, lowering the current can be achieved with current-reuse technique in the RF front-end. The overall power consumption is reduced since the bias current is shared between multiple blocks stacked one on top of the other. Many examples of current reuse configurations are proposed in literature. [2] presents a voltage controlled oscillator (VCO) using NMOS and PMOS pairs that share the available current and leads to an equivalent transconductance as standard cross-coupled topology but consuming half of the power.

Another efficient approach is to combine different functions of the RF front-end in a single circuit sharing the current [3]. Merging the low-noise amplifier (LNA) and the VCO has been proposed in [4] and depicts ultra-low power consumption for wireless sensor network applications. Also, the LNA and the mixer have been combined in one circuit achieving a good conversion gain and low power consumption despite of high noise factor [5], [6]. Another combination is between the VCO and the mixer called self-oscillating mixer (SOM) (Fig. 1) [7], [8].

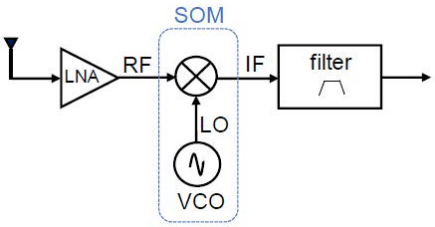


Fig. 1. Block diagram of RF front-end receiver using a SOM

In some configurations, low noise amplification is added to the SOM resulting in LMV (LNA-Mixer-VCO) circuit [9], [10]. The SOM based topologies are good candidate for ULP and low-cost applications. But, great design considerations should be taken into account since dynamics and performances of the combined building blocks have mutual dependencies [11].

In this paper, different topologies of self-oscillating mixers have been implemented and compared. Hence, depending on the design constraint, this work can help designers to choose the suitable architecture of the circuit. Section II depicts both configurations of SOM circuits and their operating principle. The proposed designs are presented in section III, while the obtained results are discussed in section IV. Conclusions are given in section V.

2. Self-oscillating mixer topologies

The principle of SOMs is based on merging the mixer and the local oscillator (LO) on one circuit. Thus, the dc bias current is reused which decreases their power consumption compared to the conventional cascaded mixer and oscillator circuits. The first designer's constraint is to choose the most appropriate topology for the SOM. That is led by the type and the disposition of the used blocks.

Concerning the oscillator, LC-VCO is recommended since it consumes less power for a given phase noise requirement. The LC-tank determines the frequency while the active cross-coupled pair allows the LC-tank loss cancellation to sustain the oscillations [12]. Concerning the mixer, Gilbert active cells are usually used in SOM circuits. They consist of a transconductor stage, ensuring the voltage-to-current conversion, and an on/off

switching core resulting in an intermediate frequency (IF) signal. Despite their low noise figure (NF), they have high linearity, high voltage conversion gain (VCG) and large frequency response [13], [14], [15], [16]. Their NF can be improved by adding some design noise reduction techniques [17].

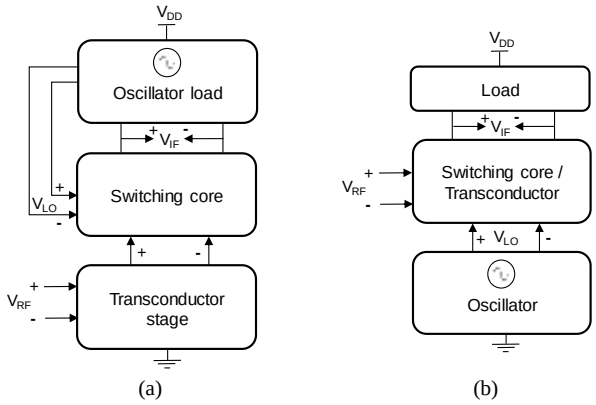
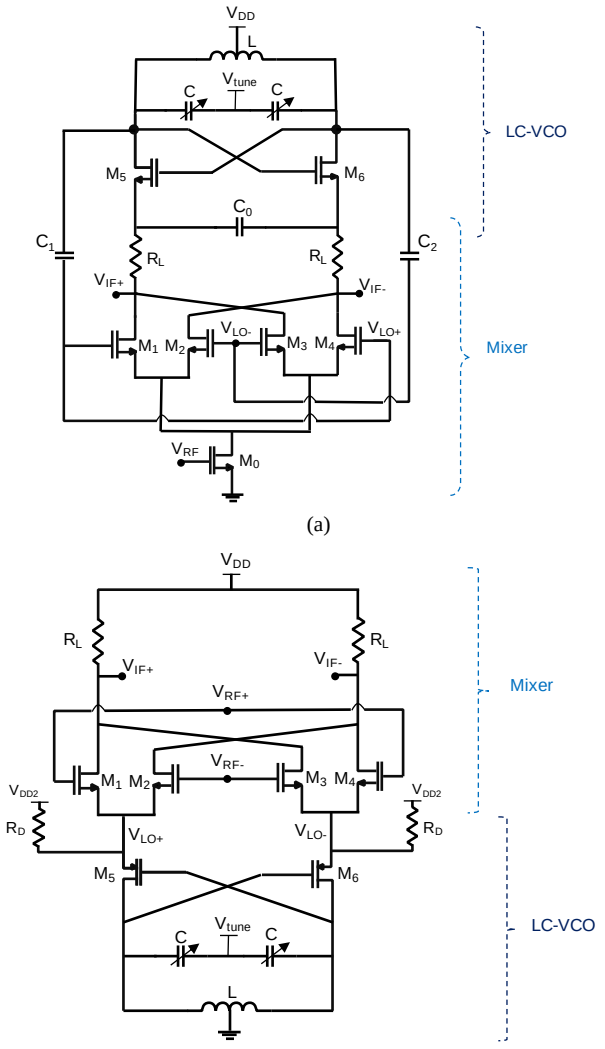


Fig. 2. SOM topologies : (a) Config1 : the oscillator is stacked above the mixer and (b) Config2: the oscillator is below the RF input stage

Most SOM topologies in literature are based on the configurations shown in Fig.2, that we will denote Config1 and Config2. In Config1 based SOMs, the oscillator is stacked above the mixer which is led by an RF transconductor stage, as depicted in Fig. 2(a). The RF input signal (V_{RF}) is applied into the transconductor stage of the Gilbert mixer. The resulting signal is multiplied with the LO signal (V_{LO}) applied to the switching core, and then the obtained IF current is converted through the load to an IF voltage (V_{IF}) [10], [18], [19].
In Config2 based SOMs, the oscillator is below the mixer, as shown in Fig. 2(b). The LO and RF inputs are injected into the switching core. In this case, the more appropriate mixing topology is the commuting mixer in which one stage of transistors can be used simultaneously as transconductance and as switches [20], [21].

3. Self-oscillating mixer designs

Two SOM circuits based on the configurations discussed above have been implemented in 130nm CMOS technology to compare their performances and to discuss the suitable choices according to a given design specification. Fig. 3 shows the schematics of the proposed self-oscillating mixers. Those SOM circuits have been designed to work at 2.4GHz, a frequency band suitable to many wireless communication standards such as Wi-Fi, Bluetooth, ZigBee, etc.
In Config1 SOM, shown in Fig. 3(a), the LC-VCO, that generates the oscillations, is stacked above a double-balanced mixer. The NMOS cross-coupled pair M_5-M_6 are used for the oscillator, while M_1-M_4 constitute the switching core for the mixer. Capacitor C_0 gives a path for LO signal which drives M_1-M_4 via capacitors C_1 and C_2 to achieve the current switching function. In the 1st half LO period, M_1, M_4 and M_5 are ON, thus output RF current of M_0 flows into them through the load R_L and C_0, while M_2, M_3 and M_6 are OFF, resulting in an IF current. In the 2nd half period, M_2, M_3 and M_6 are ON and the current flows through them, achieving a complementary operation with a resulting IF current. The differential current is converted by the resistive loads into an output IF voltage. Therefore, the cross-coupled pair of the VCO, M_5-M_6, contributes to the switching function without perturbing the natural operation of the mixer. Transistor M_0 acts as a transconductance (gm) and as a tail current to adjust the dc bias in the circuit.
In the proposed Config2 SOM, shown in Fig. 3(b), the LC-VCO uses a PMOS cross-coupled pair (M_5-M_6) for tank loss compensation instead of NMOS pairs as usually used in literature [20]. In fact, since the mixer (M_1-M_4) is stacked above the VCO, the mixer bloc appears as an external load for the VCO. Here, the output LO signals are chosen to be at the sources of the PMOS cross-coupled pair, instead of their drains in the NMOS version, in order to isolate the resonator from any load effect. Thus, the loading problem can be avoided which improves the quality factor and the phase noise (PN) performances [22]. The RF signal is applied to the gates of the transconductors (M_1-M_4) that are switched ON/OFF by the LO signal fed into their sources. A further supply voltage V_{dd2} is added to the LC-VCO section, via resistors R_D, in order to provide more dc current and to reduce the dependence between both SOM blocks improving the circuit performance.



(b)

Fig. 3. Proposed (a) Config1 and (b) Config2 self-oscillating mixer schematics

The voltage conversion gain of the circuit depends essentially on the transconductance value. It can be expressed as

$$VCG \approx \frac{1}{2} g_m R \quad (1)$$

where gm is equal to g_{m0} (transconductance of transistor M_0) and to $g_{m1\text{-}4}$ (transconductance of transistors M_1-M_4) in Config1 and Config2 SOMs, respectively. Concerning R, it is equal to R_x //R_L and to R_L in Config1 and Config2 SOMs, respectively. R_x is the resistance seen at the sources of M_5 and M_6. It highly depends on the equivalent resistance of the LC tank and its quality factor. Since this resistance tends to be small, it causes the decrease of the conversion gain, which is one of the limitations of this structure. Also, the load charge R_L cannot be highly increased because of the limited voltage headroom given by the supply voltage, given in (2). Only a certain dc voltage V_{Rmax} across it is allowed, corresponding to a maximum resistance value R_{Lmax}.

$$V_{DD} \approx V_{od_0} + V_{od_{1,2}} + V_{GS_{3,4}} + V_{Rmax} \quad (2)$$

where V_{od_i} denote the overdrive voltage $(V_{GSi} - V_{thi})$ of the transistor M_i, and $V_{Rmax} = I_{D0} R_{Lmax}$.

One of SOM circuit design challenges is to judiciously size the transconductance g_m in the mixer section since it has a direct impact on the voltage conversion gain. In Config1 SOM, the conversion gain depends on the dc current I_{d0} across g_{m0} which is limited for a fixed power budget, constraining the choice of g_{m0}. That can be expressed as

$$g_{m0} = \mu_n C_{ox} \frac{W_0}{L_0} (V_{GS0} - V_{th}) \quad (3)$$

where W_0, L_0 and V_{GS0} are the width, length, gate-to-source voltage of transistor M_0, respectively. V_{th} is the threshold voltage.

In Config2 SOM, the transconductance depends on the LO signal injected to their sources. Transistors M_1-M_4 are switched ON/OFF according to V_{LO} variation. Considering V_{LO_dc} as the dc voltage and V_{LO_OFF} as the minimum value of V_{LO} turning OFF the transistors M_1-M_4, the operating principle of the proposed SOM is shown in Fig. 4. When V_{LO}<V_{LO_dc}, transistors are ON providing a certain value of g_m. While V_{LO} increases, g_m decreases until it is OFF for $V_{LO} \geq V_{LO\_OFF}$. This latter can be expressed as

$$V_{LO\_OFF} = V_{G1-4} - V_{th} \quad (4)$$

where $V_{G1\text{-}4}$ is the gate voltage of transistors M_1-M_4.

The switched transconductance of M_1-M_4 has the following expression

$$g_{m1-4} = \mu_n C_{ox} \left(\frac{W}{L}\right)_{1-4} (V_{LO\_OFF} - V_m)$$

$$= \mu_n C_{ox} \left(\frac{W}{L}\right)_{1-4} (V_{GS1-4} - V_{LO\_dc} - V_{th} - V_m) \quad (5)$$

where $V_{GS1\text{-}4}$ and V_m are the gate-to-source voltage and the magnitude of V_{LO}, respectively. $W_{1\text{-}4}$ and $L_{1\text{-}4}$ are the width and length of transistors M_1-M_4, respectively.

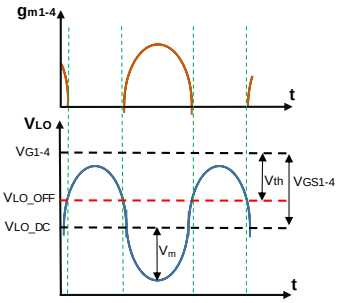


Fig. 4. LO voltage and transconductance of M_1-M_4 waveforms in Config2 SOM

As a result, the voltage conversion gains of both SOM structures can be expressed as

$$VCG_{Config1} \approx \frac{1}{2} \mu_n C_{ox} \frac{W_0}{L_0} (R_x // R_L)(V_{GS0} - V_{th}) \quad (6)$$

$$VCG_{Config2} \approx \frac{1}{2} \mu_n C_{ox} \frac{W_{1-4}}{L_{1-4}} R_L \left(V_{GS1-4} - V_{LO_{dc}} - V_{th} - V_m\right) \quad (7)$$

In order to increase the conversion gain, it is necessary to increase either the resistor or the transconductance values. Nevertheless, they are limited by the voltage headroom, that can also affect the power consumption and the noise contribution in the mixer [23]. Thus a design tradeoff between these performances should be taken into account. Furthermore, the noise at the IF output can be considered as the addition of the single noise contributions of the different sections of the self-oscillating mixer. In order to improve the noise performance of the SOM, the switching transistors need to be biased at a low dc current which decreases the 1/f noise portion. In Config1 SOM, since both stages formed by M_0 and (M_1-M_4) share the same DC current, the linearity of the transconductance stage is affected. Hence, another design tradeoff between noise and linearity in SOM circuits should be taken into account, while maintaining the same oscillation frequency.

4. Self-oscillating mixer results

Both SOM configurations, shown in Fig. 3, are implemented in 130nm CMOS technology to limit the cost of the RF front-end. Their oscillation frequency is calibrated to be on the 2.4GHz ISM band and can be tuned by changing the voltage V_{tune}. Transistors are sized to work with a regular voltage threshold, and supply voltage is 1.2V (V_{DD2} is equal to 0.6V). Both self-oscillating mixers allow reaching sub-mW operation. Their power consumptions are 800µW and 600µW for Config1 and Config2 SOMs, respectively.

Knowing that inductor is the biggest component in RF devices, and since only one inductor is used on both proposed SOM circuits, the occupied areas of Config1 and Config2 are similar and equal to 0.24mm².

The obtained conversion gains are shown in Fig. 5. The LO signal has been tuned through V_{tune} in order to get the performances at different IF frequencies. It can be seen that Config1 SOM performs a higher conversion gain than Config2 SOM. It is around 18dB for Config1 versus 9dB for Config2.

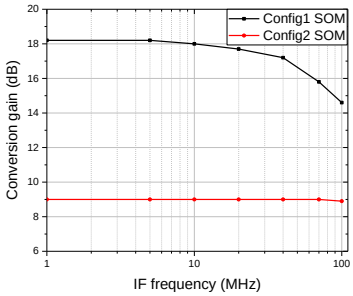


Fig. 5. Conversion gain of both SOM configurations

Moreover, Fig. 6 shows the obtained phase noise profiles of both circuits. It can be noticed that a phase noise of -113dBc/Hz and -110dBc/Hz at 1MHz offset frequency for Config1 and Config2 SOMs, respectively. This result is as expected from the previous section. While maintaining a comparable current to sustain oscillations and then a comparable power consumption between both structures, the VCG is better in the first configuration.

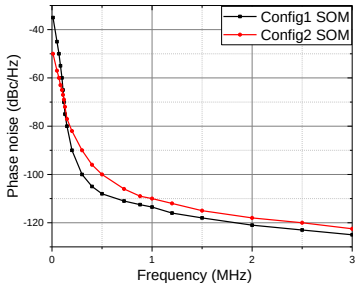


Fig. 6. Phase noise of both SOM configurations

Noise and gain performances of the Config1 are better than Config2 because of the transconductance g_{m0} that addresses a part of low noise amplification function too.

Generally, the linearity is poor in SOM circuits, since the mixer is biased at a low dc current. For example, in Config1 topology, the 3rd order intercept point (IIP3) can be approximated as [24]

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_{m0}}{K3_{gm0}}\right| f_1 f_2 C_{gs0}} \quad (8)$$

where C_{gs0} is the parasitic gate to source capacitance of transistor M_0 and $K3_{gm0}$ is the second derivative of the small signal transconductance with respect to an input voltage with input frequencies f_1 and f_2 in a 2-tone test. Hence, by reducing the dc current, g_{m0} decreases which results in a low linearity. In the proposed Config1 SOM, the obtained IIIP3 is -4dBm. The main source of distortion in Config2 SOM is the non-linearity of transistors M_1-M_4. The larger these transistors are, the higher is their IIP3. Also, increasing the overdrive voltage of M_1-M_4 can improve the linearity of the mixer at the cost of a higher power consumption. The obtained IIP3 is -12dBm for Config2 SOM.

Besides, the device and process mismatch analysis for the proposed self-oscillating mixers has been carried out by Monte Carlo simulations. The performed 600 runs include random variations of process and device mismatch. The illustrated histograms on Fig. 7 give the obtained conversion gain at an IF frequency of 10 MHz from an RF frequency of 2.45GHz. It can be noticed that both configurations have very narrow spread showing the gain stability of these SOMs versus process and mismatch uncertainties. Their standard deviations are equal to 0.003 and 0.002 with σ of 0.07 and 0.04 through mean values of 18dB and 9dB for Config1 and Config2, respectively.

A performance summary and comparison of the proposed SOM circuits with other published works is shown in Table 1.

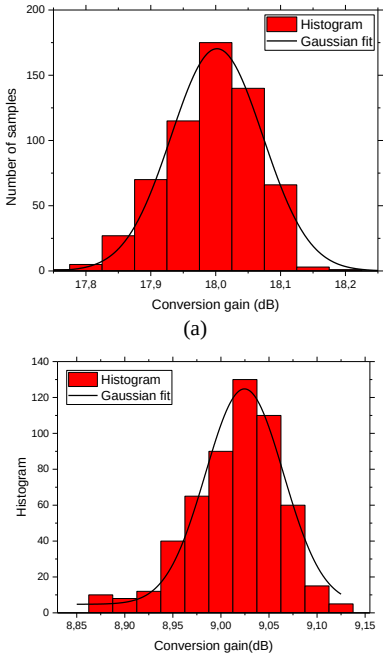


Fig. 7. Monte Carlo analysis of the conversion gain for (a) Config1 and (b) Config2 SOMs

	This work		[18]	[20]	[25]
	Config1	Config2	Config1	Config2	Config1
CMOS process (nm)	130	130	130	180	65
RF frequency (GHz)	2.45	2.45	7.8-8.8	4.2	2.5
IF frequency (MHz)	10	10	300	55	7
Supply voltage (V)	1.2	1.2	1.5	1	1
Conversion gain (dB)	18	9	11.6	10.9	10
PN @1MHz (dBc/Hz)	-113	-110	-102	-113.1	-107.4
Power P_{dc} (mW)	0.8	0.6	12	3.14	0.6
IIP3 (dBm)	-4	-12	-8.3	-11.8	-
Area (mm²)	0.24	0.24	0.47	0.96 *	1.2 *

*with pads

5. Conclusion

Two configurations of monolithic self-oscillating mixers have been presented and designed in this paper in CMOS process. A comparative study of their performances has also been carried out. By adopting a SOM approach, stacking the mixer and the VCO on top of each other, it is shown that the area and the power consumption are reduced. The circuits reach sub-mW operation which is suitable for ultra-low power applications.

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Conflicts of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.