Comparative analysis of Vertical Nanotube Field Effect Transistor (NTFET) based on channel materials for low power applications

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Abstract: - 3D Vertical Nanotube Field Effect Transistors (NTFETs) with various channel materials are analysed for 5nm gate length (L_G) in this research work. The DC and RF studies are performed on NTFET devices with Silicon, Gallium Nitride (GaN), and SiliconGermanium (SiGe) as channel materials. The impact of variation of channel length, channel thickness, and temperature analysis on these devices have been studied. The I_{ON}/I_{OFF} ratio of Si-NTFET, GaN-NTFET and SiGe-NTFET are found to be 2.7×10^8, 1.08×10^9, 1.69×10^8 respectively. GaN channel NTFET exhibits the lowest subthreshold swing (SS) of 33.1mV/dec with the highest cut-off frequency of 190 GHz. From the analysis, it is found that NTFET with GaN channel device outperforms the other two devices.

Key-Words: - Si-NTFET, GaN-NTFET, SiGe-NTFET, I_{ON}/I_{OFF} ratio, subthreshold swing (SS), transconductance (g_m), and cut-off frequency (f_t).

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1 Introduction

The nanoscale device experiences short channel effects (SCEs)[1] such as Drain-Induced Barrier Lowering (DIBL) and Gate-Induced Drain Leakage (GIDL) [2]. The multigate devices and Gate-all-around (GAA) devices such as Nanowire[3]–[5], Nanotubes[6]–[10], Tunnel FET[11]–[14], FinFET[15]–[17] were proposed in the literature to reduce the SCEs [17]–[22]. Because these devices retain high driving capabilities and produce immune to SCEs due to their strong carrier confinement and channel control [23]–[26]. Nanotube Field Effect Transistor (NTFET) is one of the promising devices for low-power applications. Its hollow cylindrical shape contributes eventual electrostatic controllability to the gates [27]–[29]. NTFET is an improved version of nanowire FET[10]. Silicon-based FET displays better drivability with good performance. GaN channel FETs have qualities such as high mobility, high saturation velocity, low electron mass and a large bandgap. [30]–[32]. GaN FET with high-κ dielectric produces a low leakage current with a high drive current of the device [33]–[35].

In this research work, DC and RF analysis of the n-type NTFET with different channel materials such as Silicon, Gallium Nitride (GaN), SiliconGermanium (SiGe) are analysed. The performance analysis is done by using the Sentaurus TCAD tool. For Si-NTFET, GaN-NTFET, and SiGe-NTFET devices, input and output characteristics, transconductance (gm), and cut-off frequency (f_t) are analysed. The study was performed on SiGe-NTFETs with various mole fractions. The DC characteristics are analysed for Si-NTFET, GaN-NTFET, and SiGe-NTFET devices with various gate length (L_G).

2 Device Structure

NTFET device architecture is designed and material analysis is done by using the Sentaurus TCAD tool. The NTFET device structure and cross-sectional view are given in Fig.1. Inner and outer gate architecture is significant in NTFET because it helps to reduce the impact of SCEs. The inner gate is surrounded by HfO_2 high-κ dielectric which could resolve the poor reliability issue caused by thin gate oxide [36], [37]. The thin gate oxide layer is surrounded by source/drain, source/drain extension, and channel. The channel is enveloped by the GAA

outer gate and outer gate oxide layer. Different channel materials such as Silicon, Gallium Nitride (GaN), SiliconGermanium (SiGe) are used.

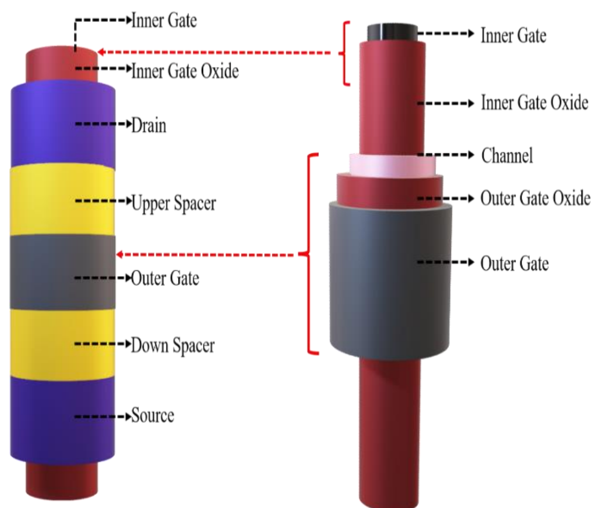

Fig.1. 3D vertical NTFET device and cross-sectional view

The parameters used in this work are given in Table 1. Sentaurus Structure Editor is used to develop the devices, doping, and to generate meshes for Si-NTFET, GaN-NTFET, and SiGe-NTFET. Sentaurus Workbench is used for performance analysis. Field and doping-dependent mobility degradations, as well as Shockley-Read-Hall (SRH), are utilized to simulate the NTFET device. Hurkx model provides a better evaluation of the Trap Assisted Tunneling current contribution to junction leakage current.

Table 1. Device Specification of NTFET

Parameter	NTFET
Inner Gate Length (L_{IG})	130 nm
Outer Gate Length (L_{OG})	5-70 nm
Channel Thickness (t_{CH})	1.8-5 nm
Inner Gate Diameter (D_{IG})	20 nm
Outer Gate Diameter (D_{OG})	32 nm
Source/Drain Length (L_S /L_D)	15 nm
Source/Drain Extension Length (L_{Sxtn} /L_{Dxtn})	33 nm
Oxide Thickness (T_{OX})	0.5 nm
Doping Concentration in Source/Drain Region	2×10^{20} cm^{-3} (N^+)
Doping Concentration in Source/Drain Extension	1×10^{20} cm^{-3} (N^+)

3 Results and Discussion

The transfer characteristics of Si-NTFET, SiGe-NTFET, GaN-NTFET are plotted in Fig.2. NTFET with GaN as a channel material shows a better I_{ON}/I_{OFF} ratio (1.08×10^9) compared to Silicon (2.7×10^8) and SiGe (1.69×10^8) due to its high bandgap energy. Wide bandgap semiconductor materials improve efficiency and power density.

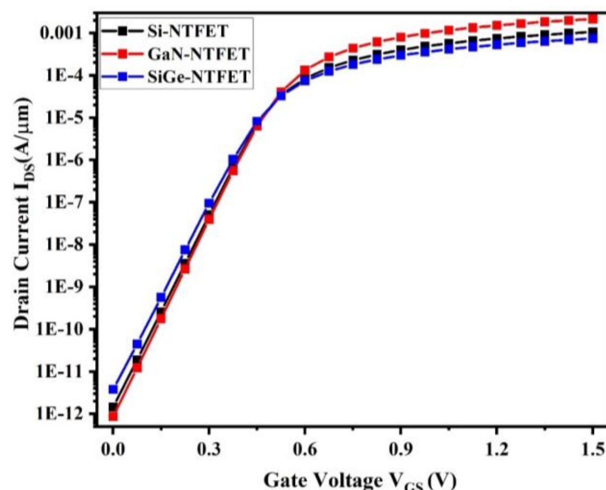

Fig.2. DC analysis of NTFET with various channel materials

3.1 The effect of Gate Length (L_G)

The study has been performed for Si-NTFET, SiGe-NTFET, GaN-NTFET for different outer gate lengths, between 5 nm and 70 nm (Fig.3 (a, b, c)).

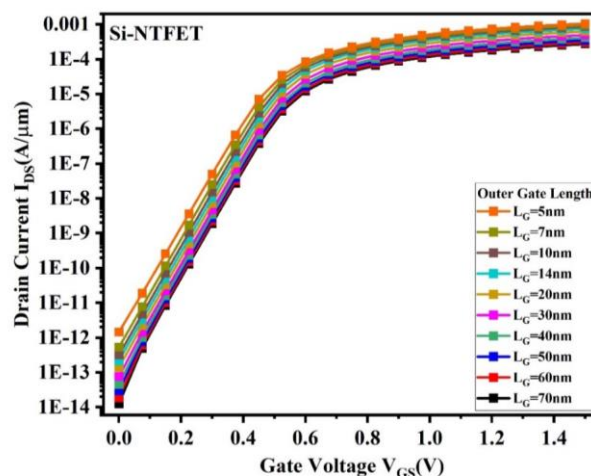

Fig.3(a). DC analysis of Si-NTFET with various gate length

Based on this investigation, it is discovered that Si-NTFET, GaN-NTFET, and SiGe-NTFET have higher drive current even for reduced gate length, which is attributed to the NTFET device's excellent drain velocity at the drain side. Scaled-down NTFET

device shows better device drivability [38]. The leakage current of the NTFET decreases as the gate length increases.

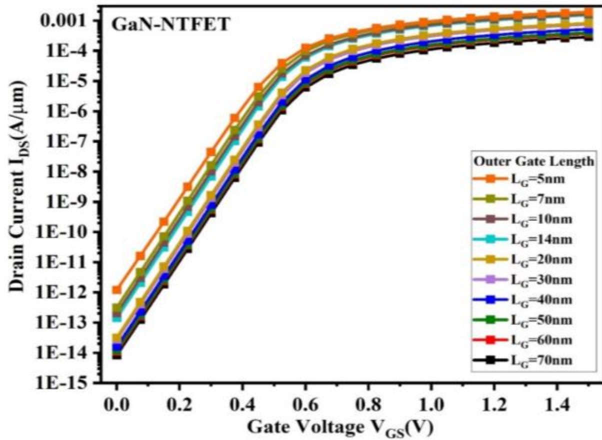

Fig.3(b). DC analysis of GaN-NTFET with various gate length

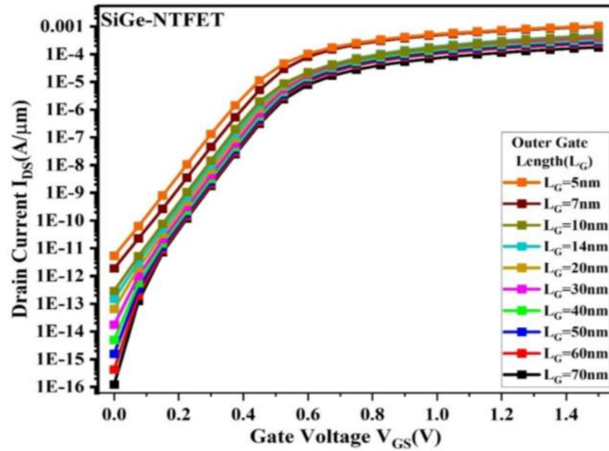

Fig.3(c). DC analysis of SiGe-NTFET with various gate length

3.2 The effect of Channel Thickness (t_{CH})

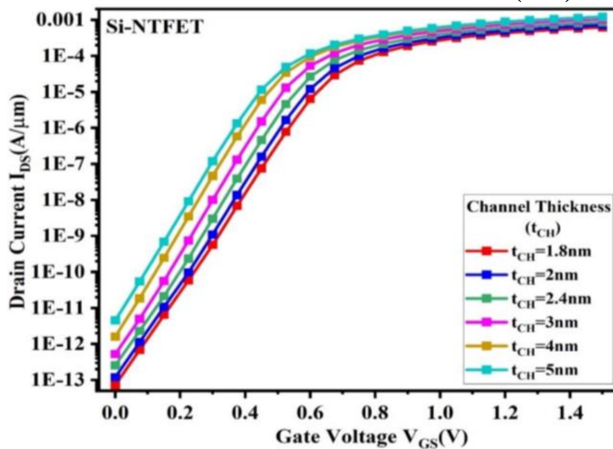

Fig.4(a). DC analysis of Si-NTFET with various Channel Thickness (t_{CH})

Fig. 4(a), 4(b), and 4(c) show the DC characteristics of Silicon, GaN, SiGe-NTFET for different channel thicknesses for a gate length of 5nm. As the channel thickness (t_{CH}) increases, the I_{ON}/I_{OFF} ratio decreases with an increased value of SS. The thin t_{CH} reduces the leakage current. This indicates that the smaller t_{CH} value has higher electrostatic control of the inner and outer gate over the channel. Compared to Silicon and SiGe channel devices, GaN-NTFET shows a better I_{ON}/I_{OFF} ratio because of its higher electron mobility.

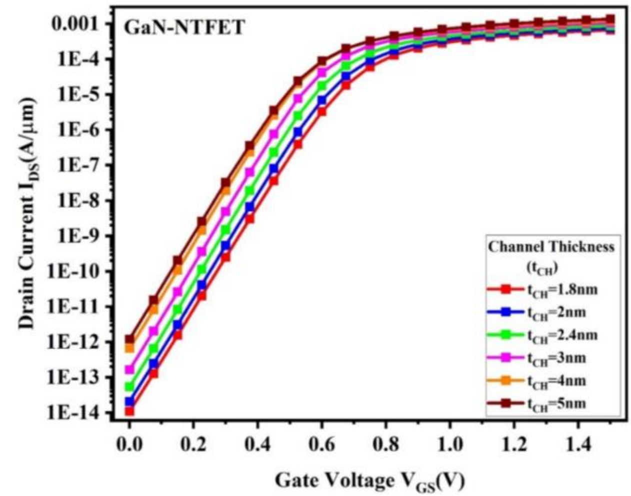

Fig.4(b). DC analysis of GaN-NTFET with various Channel Thickness (t_{CH})

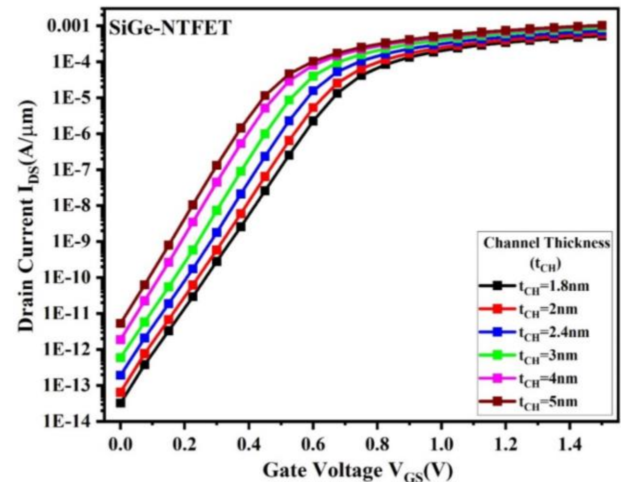

Fig.4(c). DC analysis of SiGe-NTFET with various Channel Thickness (t_{CH})

Fig.5 shows the effect of t_{CH} on the leakage current, drive current, and SS of Si, GaN, SiGe-NTFET devices. For reduced channel thickness the gate control is good which reduces the lateral field effects from the drain end. The threshold voltage of Si, GaN, and SiGe devices increases as the t_{CH} decreases (Fig.5(a)). The subthreshold swing is gently reduced with thin t_{CH} (fig 5(b)). Fig.5(c) compares the I_{ON}/I_{OFF}

ratio of Si-NTFET, GaN-NTFET, SiGe-NTFET with different channel thicknesses. I_{ON}/I_{OFF} ratio of GaN-NTFET is higher than Si and SiGe-NTFET. As shown in Fig.5(d) the OFF-state current (I_{OFF}) of GaN-NTFET is the lowest among the three devices. From these analyses, it is found that GaN-NTFET outperforms the other devices due to its high electron mobility.

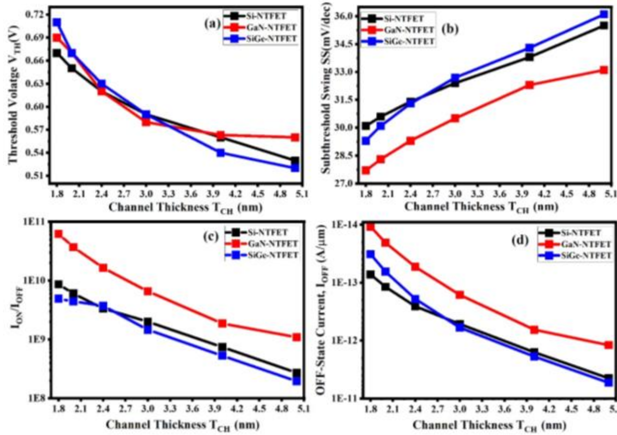

Fig.5 (a) Threshold Voltage (V_{TH}) (b) Subthreshold swing (c) I_{ON}/I_{OFF} ratio (d) OFF-state current of Si, GaN, SiGe-NTFET at different thickness Channel (t_{CH})

3.3 The effect of $Si_{(1-x)}$ Ge_x mole fraction

Fig.6 represents the drain current of $Si_{(1-x)}$ Ge_x-NTFET for various mole fractions.

Table 2. I_{ON}, I_{OFF}, V_{TH}, SS values of $Si_{1-x}Ge_x$-NTFET for various mole fraction

$Si_{1-x}Ge_x$	I_{ON} (A/μm)	I_{OFF} (A/μm)	V_{TH} (V)	SS (mV/dec)
$Si_{0.1}Ge_{0.9}$	1.22×10^{-3}	2.78×10^{-11}	0.47	39.2
$Si_{0.2}Ge_{0.8}$	1.17×10^{-3}	1.97×10^{-11}	0.48	38.5
$Si_{0.3}Ge_{0.7}$	1.10×10^{-3}	8.52×10^{-12}	0.511	37
$Si_{0.4}Ge_{0.6}$	1.06×10^{-3}	6.26×10^{-12}	0.52	36.4
$Si_{0.5}Ge_{0.5}$	1.03×10^{-3}	5.30×10^{-12}	0.524	36.1
$Si_{0.6}Ge_{0.4}$	8.56×10^{-4}	1.06×10^{-12}	0.57	33.6
$Si_{0.7}Ge_{0.3}$	8.44×10^{-4}	1.73×10^{-13}	0.62	30.9
$Si_{0.8}Ge_{0.2}$	7.61×10^{-4}	1.52×10^{-14}	0.67	28
$Si_{0.9}Ge_{0.1}$	7.26×10^{-4}	8.60×10^{-15}	0.69	27.4

It is found that as the mole fraction of Ge in $Si_{(1-x)}Ge_{(x)}$ increases, the band gap shrinks, and carrier mobility increases, which leads to a higher drive current. In Table 2 I_{ON}, I_{OFF}, V_{TH}, SS values of $Si_{(1-x)}$ $Ge_{(x)}$ for various mole fraction are given.

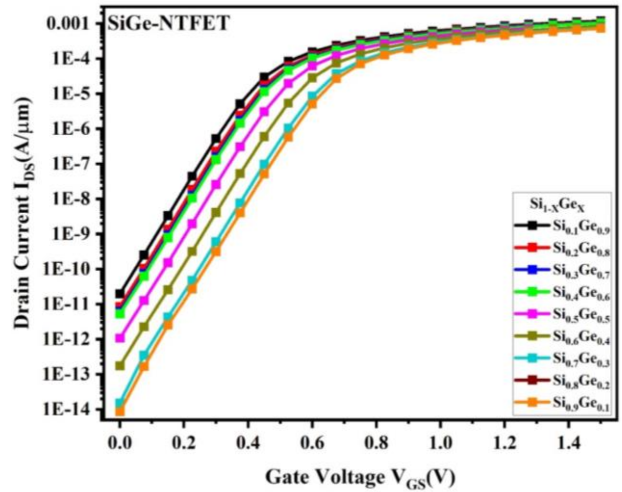

Fig.6 DC analysis of SiGe-NTFET with various mole fraction

3.4 Temperature Analysis

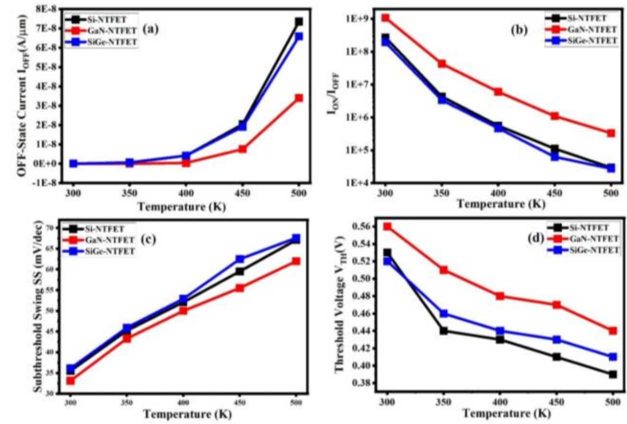

Fig.7(a) OFF-state current (I_{OFF}) (b) I_{ON}/I_{OFF} ratio (c) Subthreshold swing (SS) (d) Threshold Voltage (V_{TH}) of Si, GaN, SiGe-NTFET at different temperature

The temperature analysis of Si, GaN, SiGe-NTFET is plotted in fig.7. Fig 7(a) shows the leakage current vs temperature. The leakage current (I_{OFF}), threshold voltage (V_{TH}) and SS of GaN are greatly reduced and good I_{ON}/I_{OFF} ratio is maintained even for high temperature which is shown in fig7(b), (c) and (d) due to high band gap of GaN.

3.5 Output Characteristics

Further analysis has been performed for L_G of 5nm and channel thickness (t_{CH}) of 5nm. The output characteristics of the Si-NTFET, GaN-NTFET, SiGe-NTFET plotted for gate voltage (V_{GS}) are swept from 0.3V to 1.5V (Fig.8). The ON-state current (I_{ON}) is low for a V_{GS} of 0.3V due to the wider barrier width. The ON-state current increases as V_{GS} is increased from 0.3V to 1.5V.

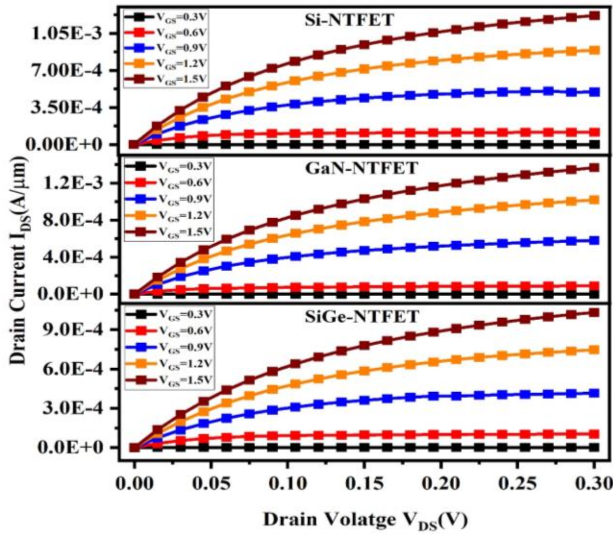

Fig.8. Drain current Vs Drain voltage of NTFET with different materials

3.6 Transconductance and cut off frequency

In Fig.9 the transconductance characteristics of Si-NTFET, GaN-NTFET, SiGe-NTFET are plotted for V_{DS}=0.3V. From Fig.9, it is noted that the value of transconductance steadily increases as V_{GS} extends from 0V to 1.5V. The trans-conductance increases as the control over the gate is enhanced. The transconductance is greatly high for GaN-NTFET than for Si-NTFET and SiGe-NTFET. The transconductance is impacted by the drain current (1):

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad (1)$$

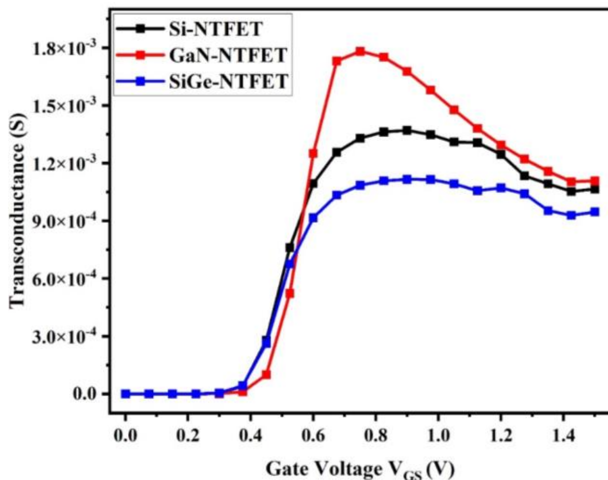

Fig.9. Transconductance characteristics of Si-NTFET, GaN-NTFET, SiGe-NTFET

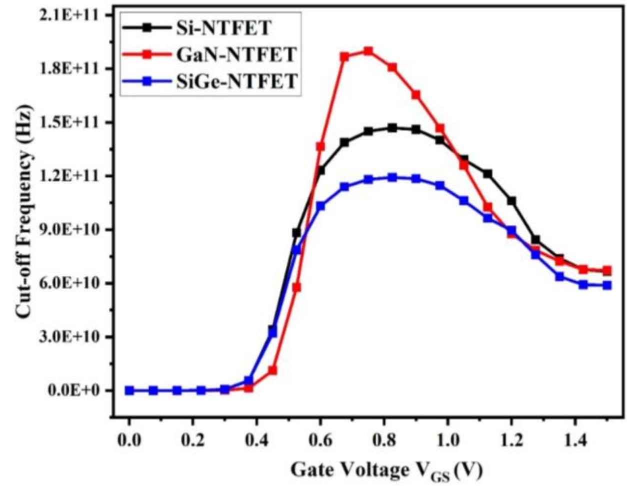

Fig.10. Cut off Frequency for Si-NTFET, GaN-NTFET, SiGe-NTFET

The frequency at which the current gain equals unity is denoted as the cut-off frequency (f_t) and can be represented mathematically (2)

$$f_t = \frac{g_m}{2\pi C_{GG}} \quad (2)$$

The leakage current of GaN-NTFET is improved by 17.37% compared to Si-NTFET and by 77.54% compared to SiGe-NTFET. The transconductance of GaN-NTFET is improved by 29.92% compared to Si-NTFET and by 60.36% compared to SiGe-NTFET. The cut-off frequency of GaN-NTFET is improved by 29.25% compared to Si-NTFET and by 59.66% compared to SiGe-NTFET. In terms of Subthreshold Swing (SS), GaN-NTFET is decreased by 6.76% and 8.31% compared to Si-NTFET and SiGe-NTFET respectively. The comparison of Si-NTFET, GaN-NTFET, and SiGe-NTFET for the various parameters such as I_{ON}, I_{OFF}, I_{ON}/I_{OFF}, V_{TH}, SS, gm, f_T is shown in Table 3.

Table 3. Comparison of Si-NTFET, GaN-NTFET, SiGe-NTFET for L_G=5nm, t_{CH}=5nm

Material	Silicon	GaN	SiGe
I_{ON} (A/µm)	1.06×10^{-3}	1.94×10^{-3}	1.06×10^{-3}
I_{OFF} (A/µm)	1.44710^{-12}	1.19×10^{-12}	6.26×10^{-12}
I_{ON}/I_{OFF}	2.70×10^{8}	1.08×10^{9}	1.69×10^{8}
V_{TH} (V)	0.53	0.56	0.52
SS(mV/dec)	35.5	33.1	36.4
gm (S)	1.37×10^{-3}	1.78×10^{-3}	1.11×10^{-3}
f_t (GHz)	147	190	119

The performance comparison of GaN channel NTFET and SiGe channel NTFET are compared with reported NTFET and NWFET devices as given in

Table 4. The proposed novel GAA GaN channel NTFET shows a 55% improvement in SS and the I_{ON}/I_{OFF} ratio is improved by 4 magnitudes compared to the work reported in [7]. Compared to GaN-NWFET [39], the SS is improved by 57% and the I_{ON}/I_{OFF} ratio is improved by 4 magnitudes.

Table 4. Performance comparison of GaN, SiGe-NTFET and GaN, SiGe-NWFET at same gate length (L_G) and channel thickness (t_{CH})

Ref	**Material**	**Device**	**L_G (nm)**	**t_{CH} (nm)**	**SS (mV/dec)**
This Work	GaN	NTFET	5	1.8	28
[7]	GaN	NTFET	5	1.8	~63
This Work	GaN	NTFET	5	1.6	27.1
[7]	GaN	NTFET	5	1.6	63.8
[39]	GaN	NWFET	5	1.6	65.7
This Work	SiGe	NTFET	7.5	5	34.38
[40]	SiGe	NW-FinFET	7.5	5	-

4 Conclusion

Silicon, GaN, SiGe based NTFET have been simulated. The results of important metrics like ON-state current (I_{ON}), OFF-state current (I_{OFF}), subthreshold swing (SS), transconductance (g_m), and cut-off frequency (f_t) have been compared for Si-NTFET, GaN-NTFET, and SiGe-NTFET. From this study, GAA double gate GaN-NTFET results in the lowest leakage current. This shows that GaN-NTFET has good control over the channel due to its high electric field strength and electron mobility. GaN NTFET outperforms in terms of I_{ON}/I_{OFF} ratio, transconductance, and cut-off frequency.

Statements & Declarations

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References:

[1] D. E. Nikonov and I. A. Young, Benchmarking of Beyond-CMOS Exploratory Devices for Logic Integrated Circuits, *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits*, vol. 1, no. c, pp. 3–11, 2015, doi: 10.1109/JXCDC.2015.2418033.

[2] H. Valinajad, R. Hosseini, M. E. Akbari, A. Branch, and K. Branch, Electrical Characteristics of Strained Double Gate, *International Journal of Recent Research and Applied Studies*, vol. 13, no. November, pp. 436–442, 2012.

[3] B. H. Lee *et al.*, Vertically Integrated Multiple Nanowire Field Effect Transistor, *Nano Letters*, vol. 15, no. 12, pp. 8056–8061, 2015, doi: 10.1021/acs.nanolett.5b03460.

[4] Y. Zhai *et al.*, High-performance vertical gate-all-around silicon nanowire FET with high-κ/metal gate, *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3896–3900, 2014, doi: 10.1109/TED.2014.2353658.

[5] X. Chen, S. Chen, Q. Hu, S. L. Zhang, P. Solomon, and Z. Zhang, Device noise reduction for silicon nanowire field-effect-Transistor based sensors by using a schottky junction gate, *ACS Sensors*, vol. 4, no. 2, pp. 427–433, 2019, doi: 10.1021/acssensors.8b01394.

[6] A. Singh, S. Chaudhury, C. K. Pandey, S. M. Sharma, and C. K. Sarkar, Design and analysis of high k silicon nanotube tunnel FET device, *IET Circuits, Devices and Systems*, vol. 13, no. 8, pp. 1305–1310, 2019, doi: 10.1049/iet-cds.2019.0230.

[7] K. Han, J. Li, Z. Deng, Y. Zhang, and S. Long, GaN Nanotube FET with Embedded Gate for High Performance, Low Power Applications, *IEEE Journal of the Electron Devices Society*, vol. 8, no. June, pp. 925–929, 2020, doi: 10.1109/JEDS.2020.3012687.

[8] H. M. Fahad and M. M. Hussain, Are nanotube architectures more advantageous than nanowire architectures for field effect transistors?, *Scientific Reports*, vol. 2, pp. 2–8, 2012, doi: 10.1038/srep00475.

[9] S. P. Scarlet, N. Vinodhkumar, and R. Srinivasan, Performance enhancement of

junctionless silicon nanotube FETs using gate and dielectric engineering, *Journal of Computational Electronics*, no. 0123456789, 2020, doi: 10.1007/s10825-020-01611-5.

[10] H. M. Fahad and M. M. Hussain, High-performance silicon nanotube tunneling FET for ultralow-power logic applications, *IEEE Transactions on Electron Devices*, vol. 60, no. 3, pp. 1034–1039, 2013, doi: 10.1109/TED.2013.2243151.

[11] D. Gracia and D. Nirmal, Performance Analysis of Dual Metal Double Gate Tunnel-FETs for Ultralow Power Applications, *Lecture Notes in Electrical Engineering*, vol. 466, pp. 11–18, 2018, doi: 10.1007/978-981-10-7191-1_2.

[12] D. Gracia, D. Nirmal, and D. J. Moni, Impact of leakage current in germanium channel based DMDG TFET using drain-gate underlap technique, *AEU - International Journal of Electronics and Communications*, vol. 96, pp. 164–169, 2018, doi: 10.1016/j.aeue.2018.09.024.

[13] D. Gracia, D. Nirmal, and A. Nisha Justeena, Investigation of Ge based double gate dual metal tunnel FET novel architecture using various hetero dielectric materials, *Superlattices and Microstructures*, vol. 109, pp. 154–160, 2017, doi: 10.1016/j.spmi.2017.04.045.

[14] D. J. Moni, A. J. Anucia, D. Gracia, and D. Nirmal, Performance Analysis of GaSb/InAs Tunnel FET for Low Power Applications, *Proceedings of the 4th International Conference on Devices, Circuits and Systems, ICDCS 2018*, pp. 335–338, 2019, doi: 10.1109/ICDCSyst.2018.8605119.

[15] A. Nandi, A. K. Saxena, and S. Dasgupta, Design and analysis of analog performance of dual-k spacer underlap N/P-FinFET at 12 nm gate length, *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1529–1535, 2013, doi: 10.1109/TED.2013.2250975.

[16] S. S. Zaman, P. Kumar, M. P. Sarma, A. Ray, and G. Trivedi, Design and simulation of SF-FinFET and SD-FinFET and their performance in analog, RF and digital applications, *Proceedings - 2017 IEEE International Symposium on Nanoelectronic and Information Systems, iNIS 2017*, vol. 2018-Febru, no. December, pp. 200–205, 2018, doi: 10.1109/iNIS.2017.49.

[17] A. Kranti and G. A. Armstrong, Source/drain extension region engineering in FinFETs for low-voltage analog applications, *IEEE Electron Device Letters*, vol. 28, no. 2, pp. 139–141, 2007, doi: 10.1109/LED.2006.889239.

[18] A. Kranti and G. A. Armstrong, Design and optimization of FinFETs for ultra-low-voltage analog applications, *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3308–3316, 2007, doi: 10.1109/TED.2007.908596.

[19] A. Nandi, A. K. Saxena, and S. Dasgupta, Design and analysis of analog performance of dual-k spacer underlap N/P-FinFET at 12 nm gate length, *IEEE Transactions on Electron Devices*, vol. 60, no. 5, pp. 1529–1535, 2013, doi: 10.1109/TED.2013.2250975.

[20] R. Wang *et al.*, Analog/RF performance of Si nanowire MOSFETs and the impact of process variation, *IEEE Transactions on Electron Devices*, vol. 54, no. 6, pp. 1288–1294, 2007, doi: 10.1109/TED.2007.896598.

[21] K. D. Buddharaju *et al.*, Gate-all-around Si-nanowire CMOS inverter logic fabricated using top-down approach, *ESSDERC 2007 - Proceedings of the 37th European Solid-State Device Research Conference*, vol. 2007, no. October, pp. 303–306, 2007, doi: 10.1109/ESSDERC.2007.4430938.

[22] T. J. King, FinFETs for nanoscale CMOS digital integrated circuits, *IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, ICCAD*, vol. 2005, pp. 207–210, 2005, doi: 10.1109/ICCAD.2005.1560065.

[23] J. Song, B. Yu, Y. Yuan, and Y. Taur, A review on compact modeling of multiple-gate MOSFETs, *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 8, pp. 1858–1869, 2009, doi: 10.1109/TCSI.2009.2028416.

[24] F. G. Pikus, K. K. Likharev, F. G. Pikus, and K. K. Likharev, Nanoscale field-effect transistors : An ultimate size analysis Nanoscale field-effect transistors : An ultimate size analysis, *Applied Physics Letters,* vol. 3661, pp. 1–4, 1997, doi: 10.1063/1.120473.

[25] Z. Ren, R. Venugopal, S. Datta, M. Lundstrom, D. Jovanovic, and L. Alamos, The Ballistic Nanotransistor: A Simulation Study, *IEEE,* vol. 87545, pp. 4–7.

[26] G. Baccarani and S. Reggiani, A Compact Double-Gate MOSFET Model Comprising Quantum-Mechanical and Nonstatic Effects, *IEEE Transactions on Electron Devices,* vol. 46, no. 8, pp. 1656–1666, 1999.

[27] J. Hur *et al.*, Comprehensive Analysis of Gate-Induced Drain Leakage in Vertically Stacked Nanowire FETs: Inversion-Mode Versus Junctionless Mode, *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 541–544, 2016, doi: 10.1109/LED.2016.2540645.

[28] R. Ambika and R. Srinivasan, Analysis of independent gate operation in Si nano tube FET and threshold prediction model using 3D numerical simulation, *Journal of Computational Electronics*, vol. 15, no. 3, pp. 778–786, 2016, doi: 10.1007/s10825-016-0822-5.

[29] H. M. Fahad, C. E. Smith, J. P. Rojas, and M. M. Hussain, Silicon nanotube field effect transistor with core-shell gate stacks for enhanced high-performance operation and area scaling benefits, *Nano Letters*, vol. 11, no. 10, pp. 4393–4399, 2011, doi: 10.1021/nl202563s.

[30] M. S. Islam, N. K. Alam, and R. Islam, Effect of Gate Length on the ballistic performance of nanoscale InGaSb double gate MOSFET, 2014 *International Conference on Informatics, Electronics & Vision (ICIEV),* pp. 8–11, 2014.

[31] I. Bin, K. Arnub, and M. T. Ali, Design and Analysis of Logic Gates using GaN based Double Gate MOSFET (DG-MOS), *AIUB Journal Of Science and Engineering,* Vol. 06, no. 01, 2018.

[32] G. Length, R. Kim, U. E. Avci, and I. A. Young, Comprehensive Performance Benchmarking of III-V and OFF -Current, *IEEE Transactions on Electron Devices,* vol. 62, no. 3, pp. 713–721, 2018.

[33] M. Kanamura, T. Ohki, T. Kikkawa, and K. Imanishi, Enhancement-Mode GaN MIS-HEMTs With High- k Gate Dielectrics, *IEEE Electron Devices Letters*, vol. 31, no. 3, pp. 189–191, 2010.

[34] H.- Laalo *et al.*, High-Performance GaN MOSFET With High-κ $LaAlO_3/SiO_2$ Gate Dielectric, *IEEE Electron Devices Letters*, vol. 33, no. 1, pp. 2011–2013, 2012.

[35] K. Lee, C. Huang, J. Gong, and C. Lee, High-Performance 1- µ m GaN n-MOSFET With MgO / MgO – TiO 2 Stacked Gate Dielectrics, *IEEE Electron Devices Letters*, vol. 32, no. 3, pp. 306–308, 2011.

[36] R. K. Baruah and R. P. Paily, A dual-material gate junctionless transistor with high-k spacer for enhanced analog performance, *IEEE Transactions on Electron Devices*, vol. 61, no. 1, pp. 123–128, 2014, doi: 10.1109/TED.2013.2292852.

[37] K. Koley, A. Dutta, S. K. Saha, and C. K. Sarkar, Analysis of high-κ spacer asymmetric underlap DG-MOSFET for SOC application, *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1733–1738, 2015, doi: 10.1109/TED.2015.2397699.

[38] A. Singh, C. K. Pandey, S. Chaudhury, and C. K. Sarkar, Effect of strain in silicon nanotube FET devices for low power applications, *EPJ Applied Physics*, vol. 85, no. 1, pp. 1–7, 2019, doi: 10.1051/epjap/2018180236.

[39] Y. Chu *et al.*, Superior Performance of 5-nm Gate Length GaN Nanowire nFET for Digital Logic Applications, *IEEE Electron Device Letters*, vol. 40, no. 6, pp. 874–877, 2019, doi: 10.1109/LED.2019.2894416.

[40] M. S. Mobarakeh, S. Omrani, M. Vali, A. Bayani, and N. Omrani, Theoretical logic performance estimation of Silicon, Germanium and SiGe nanowire Fin-Field Effect Transistor, *Superlattices and Microstructures*, vol. 120, pp. 578–587, 2018, doi: 10.1016/j.spmi.2018.06.022.

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All authors contributed to the study conception and design. Device modelling and analysis were performed by Josephine Anucia. A, Jackuline Moni. D. The first draft of the manuscript was written by Josephine Anucia.A. All authors read and approved the final manuscript.

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