Implementation of a Low Power Boost Converter in-line with a Rectifier for RF Energy Harvesting Application

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Abstract—With the growing requirement of RF coverage, harvesting and management of the associated power along with the conversion of energy into appropriate form is essential. It makes the design of relevant rectifier systems an important aspect. Attainment of a high percentage conversion efficiency (PCE) at lower input power, may not be enough if it is not supported by a DC-DC converter. A boost converter plays a significant role for managing the harvested energy for further utilization. This paper presents a simple, low power, high frequency boost converter for specific target storages or applications. It achieves a peak efficiency of 93% at a very low input power of -12dBm with the use of only two MOSFETs and for smaller value of inductance making the design feasible. Moreover it achieves a very good transient settling time of 5.5µs .

Keywords—*Energy Harvesting, PCE, Boost Converter*
Received: December 13, 2020. Revised: July 15, 2021. Accepted: July 31, 2021. Published: August 10, 2021.

1. Introduction

Self-sustainable architectures are gaining interest and acceptability in many facets of technology. Researchers are attempting to develop highly efficient structures for different target applications while considering the feasibility and cost effectiveness. A good power management strategy is always important after efficiently converting the RF energy to DC with the use of a high frequency rectifier. The output power or the voltage of the rectifier is generally not suitable for the target device or for charging a battery. To facilitate this, the power or the voltage needs to be either boosted or bucked depending on the application. Hence, design and implementation of a DC-DC converter is important while considering proper efficiency, lower power, less area and implementation feasibility as important elements.

Many designs are reported in which indicate a series of works that have been undertaken in this domain. Single-switch inverting buck-boost^2 converter (SIBB2C) design is presented in [1] which emphasises on using less number of switches and wide conversion ratio. This design is experimented in both step-down and step-up modes with maximum of 90% efficiency while maintaining feasibility and maneuverability. A low-voltage stress buck-boost converter with a high voltage conversion gain based is proposed in [2] which is based on a coat circuit where the problem of parasitic parameters of the device is dealt with to get higher conversion ratio. The higher and wider conversion gain is achieved with the use of a single switch only. A very high gain and low power Graphene Nano Ribbon Field Effect Transistors (GNRFET) based Buck and Boost converter is reported in [3]. This is a switch capacitor based 4-ribbon GNRFET design which achieves 97% efficiency at higher load and 85% at lower load and frequency. A dual input buck-boost converter is reported in [4] as part of an energy harvesting power management system which is claimed to achieve upto 95.1% efficiency with reduction in indictor dependence. A 3-mode charge pump based single input multi output buck-boost converter is designed in [5] which modifies the power stage topology and achieves higher gain and faster transient response. It facilitates smooth transition between modes with 94.61% peak efficiency and 9.9 µs response time.

This paper presents a very simple DC-DC converter in line with the previously designed TG based RF rectifier [14]. The proposed design demonstrates a peak efficiency of 93% at -12dBm. The output voltage is 4.9V which is sufficient to charge a battery and also can be used for powering up any other systems. The inductance used is very low. Further it achieves a proper settling time of 5.5µs at 28µW which is significant. The basic strength of the design is its simple structure while maintaining all other parameters at par with any other contemporary works.

The remaining of the paper is organised as follows. Section II deals with the proposed design with explanation of the functionality, Section III deals with simulation results and discussion and Section IV includes the concluding remark.

2. The Proposed Design

In this work, we have proposed a simple and modular single stage DC-DC boost converter to achieve desired voltage level to charge a battery. This design is flexible to be operated in multiple ranges of sources from nW to microwatt with a single shared inductor. The proposed power stage has two major features. First, the switching frequency is high because of the adoption of 45nm technology node. Second, the ripples associated with the inductor current is reduced by more than 80%. The discontinuous mode of operation is performed without having any current sensing mechanism. The schematic of the design is illustrated in Fig.1.

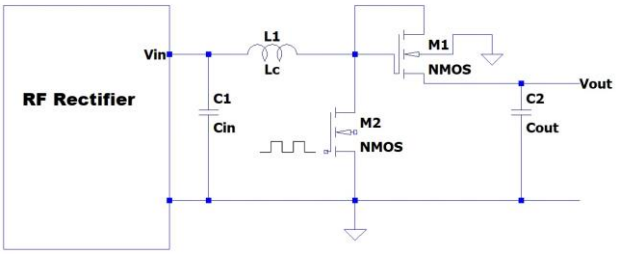

Figure 1: The proposed design

Figure 1 shows the basic configuration of a boost converter in line with a RF rectifier where the switch integrated is a MOSFET. In our case, the diode has been replaced by a second MOS switch that is essentially used in most of the lower power converters. The major parameters that we have considered for the designing of the power stage are minimum input voltage $V_{IN(min)}$, nominal output voltage V_{OUT} and maximum output current $I_{OUT(max)}$.

The first step of the design is to determine the maximum switching current which is invariably depends on the duty cycle (D) at $V_{IN(min)}$. We have also added the efficiency of the converter (η) for more realistic duty cycle as presented in Eq.1

$$D = 1 - \frac{V_{IN(\min)}}{V_{OUT}}\eta \tag{1}$$

In the next step we have to determine the maximum switching current which is a direct function of the inductor ripple current. Eq.2 and Eq.3 shows the expressions for inductor ripple current and maximum switching current.

$$\Delta L = \frac{V_{IN(\min)}}{f_{sw}L} D \tag{2}$$

$$I_{OUT(\max)} = \left(I_{L(\min)} - \frac{\Delta L}{2}\eta \right)(1-D) \tag{3}$$

Here I_{Lmin} is the minimum current of the switch and f_{sw} switching frequency. In this case for a reasonable approximation, we have considered inductor ripple current as 20%. Accordingly we have calculated the inductor value using Eq.4.

$$L = \frac{V_{IN(\min)} \times (V_{OUT} - V_{IN})}{f_{sw} \times \Delta L \times V_{OUT}} \tag{4}$$

It can be observed that, higher the inductor value, the higher is the maximum output current because of the reduced ripple current. With this analysis we have developed the converter stage and then select the value of output capacitor C_{OUT} using Eq.5.

$$C_{OUT} = \frac{I_{OUT(\max)}}{f_{sw}\Delta V_{OUT}} D \tag{5}$$

Here, ΔV_{OUT} is the desired output voltage ripple which we have considered as 5% of the output voltage.

By considering these equations we have chosen the following parameters for a target output voltage of 5V as for most of the applications including charging of a battery, 5V is a standard value. The chosen values are presented in table 1.

Table 1: Chosen values of parameters

Parameters	Values
Inductor	10μH
C_{in}	100pF
C_{out}	1pF
Switching Frequency	100MHz
Duty cycle	90%
Input Voltage	800mV

We have plotted inductance across the switching frequency in figure 2, which shows that they maintain an inverse exponential relationship and at 100MHz we can get a very low value of inductor, which is acceptable from the feasibility of fabrication point of view. We may increase the frequency further to reduce the inductance but that may complicate the generating circuitry. So this can be considered as optimization of switching frequency and the inductance.

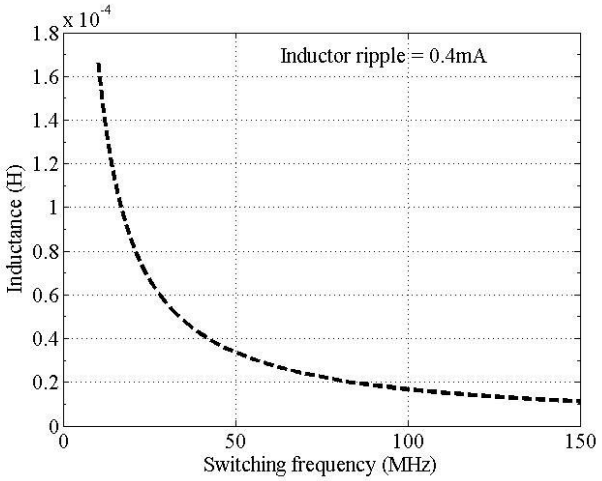

Figure 2: Inductance versus switching frequency

The output voltage is plotted across the inductance in figure 3. This confirms our chosen value for the target output voltage.

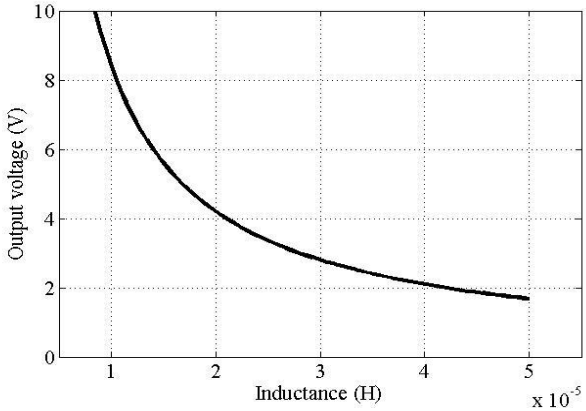

Figure 3: Output voltage versus inductance

The output capacitance is plotted across the ripple voltage and shown in figure 4, which also depicts an inverse exponential relationship of these parameters. The significance our chosen value of output parameter is reflected in this plot.

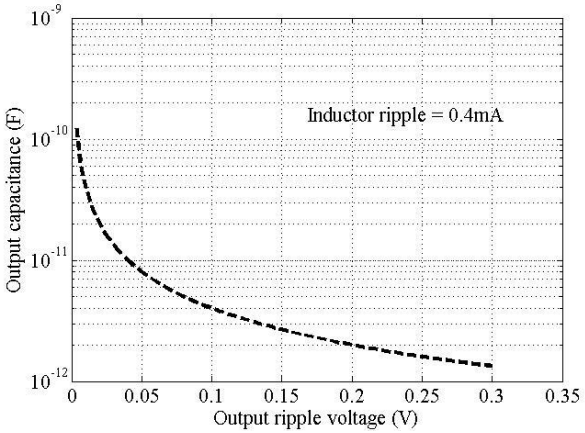

Figure 4: Output capacitance versus output ripple voltage

The circuit is simulated using GPDK 45nm and analyzed different aspects of its performance. The transient response is shown in figure. 5.

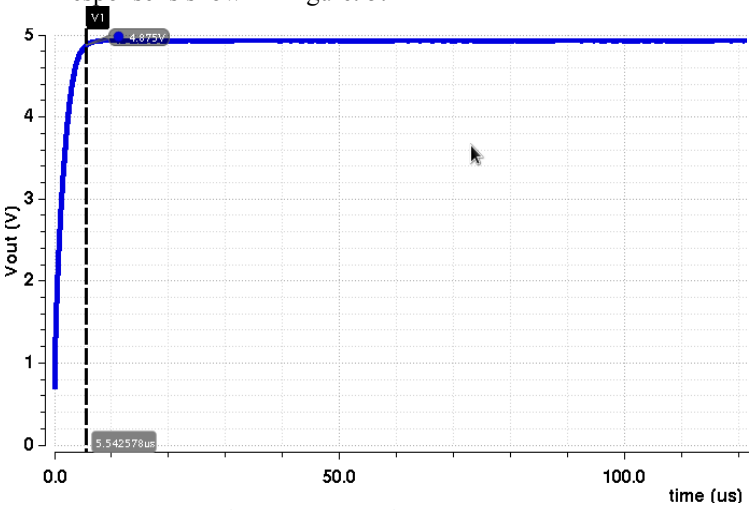

Figure 5: Transient response

Figure 6 clearly shows the output voltage of 4.9V which is very close to the targeted value. Also from the fitted marker it is seen that the transient is settling at 5.5µs. Also the transient is plotted for different value of input voltages starting from 100mV to the maximum of 1V and is shown in figure 6. It is evident that the output voltage increases with the increase of the input voltage. Also it is giving better settling time as the input voltage increases. This direct relationship of V_{out} and V_{in} is further clearly depicted in figure 7.

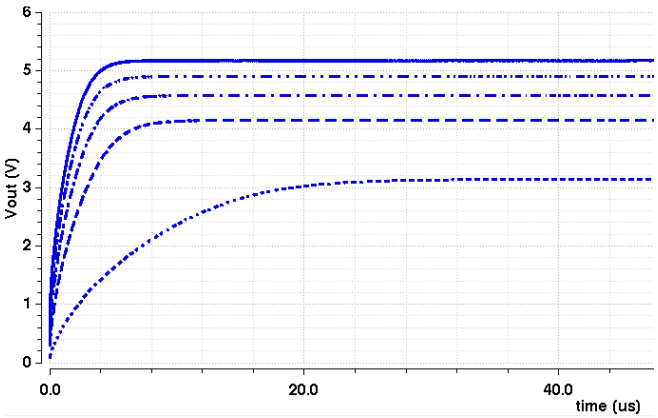

Figure 6: Transient for different input voltages

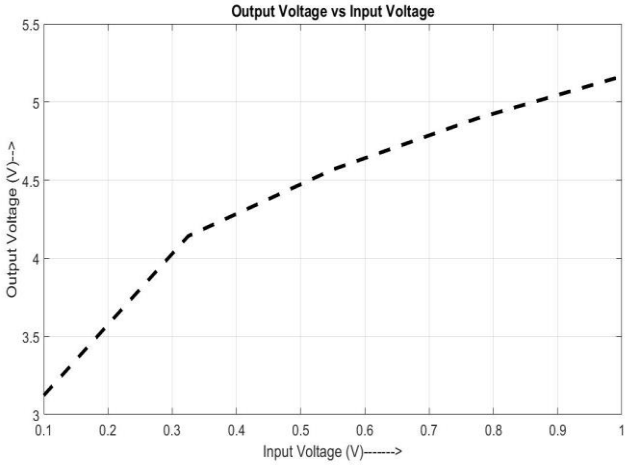

Figure 7: Output Voltage versus Input Voltage

The conversion efficiency is plotted across input power. The peak efficiency is observed at -12dBm and is shown in figure 8. This shows a maximum efficiency of 93% which is at par with any other complex realization.

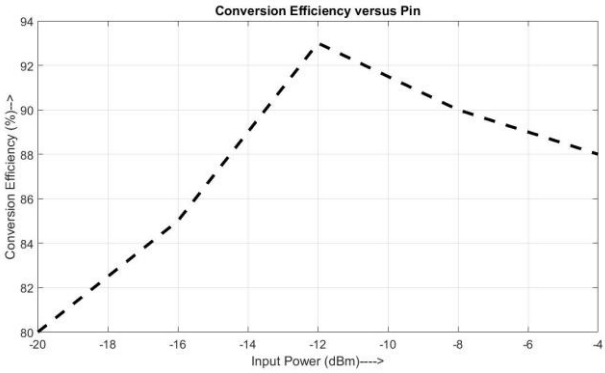

Figure 8: Conversion Efficiency versus Input Power

Table 2: Comparative Analysis with recent works

	[1]	[2]	[5]	[6]	[7]	[8]	[9]	**This Work**
Technology Node	--	--	0.18µm BCD	.25µm CMOS	0.35µm CMOS	0.18µm CMOS	0.35µm CMOS	**45nm**
Input Voltage(V)	24	48	2.7-4.2	2.5-5	2.1-3.3	1.8	2.5	**0.8**
Output Voltage(V)	-118	400	1.8, 3.3, 5	1.8, 5	1.8, 2.5, 3 3. 3	0.9, 1.2, 1.5, 1.8	1.8, 2.5, 3, 3.	**4.9**
Switching frequency	25kHz	100kHz	1M Hz	2MH z	0.5MHz	2M Hz	0.75-1MHz	**100MHz**
Inductor	470 µH	950 µH	4.7 µH	2.2µ H	4.7 µH	N/A	4.7 µH	**10µH**
Capacitor	30µF	4µF	4.7 µF	22µF	10µF	N/A	10uF	**1pF**
No. of Transistors	4/6	5	6	5	7	6	6	**2**
Passive Components	5/7	8	8	7	8	7	8	**3**
Peak efficiency	90%	94.3%	94.61%	90%	91%	83.7%	89.5%	**93%**
Load transient response	--	--	9.9µs@ 1.5W	70µs @0.5 W	80µs@0 .5W	192µs@ 0.11W	40µs@1 .02W	**5.5µs@28µ W**

We have compared our proposed design with different contemporary reported works. This is summarized in table 2. The tabulated values clearly shows that the performance of the system is satisfactory with the use lesser number of components and smaller values of inductance. This confirms that circuit will be helpful for realization in a small area and thereby yield a cost effective structure. The settling time of the transient is also provides better performance.

3. Conclusion

The simple DC-DC boost converter is implemented in line with a previously designed high frequency rectifier. The basic design emphasis was to utilise the energy harvesting system for charging of a battery or directly powering up some applications and hence 5V was chosen as the target output voltage. Though there happens to be several such boost converters reported but most of them are implemented with complex circuitry and thereby increases the implementation cost. Also many of the structures deal with high power only. So we have tried to design a very simple structure with optimum number of components at low input power. Making a boost converter at power is significant so as to use it as part of a realistic energy harvesting system. We have tried to reduce the inductance value as that is crucial for maintain low chip area. This implantation is capable to achieve 93% peak conversion efficiency at -12dBm while optimising the inductance value to be 10µH. Capacitances are also very small. Thus the realization was done with 2 MOSFETs and 3 passive components, which can be stated to be a significant achievement at low power. The settling time of the transient is also quite low which indicates its capability for high frequency applications. The structure can be extended further with a proper and well-designed high frequency pulse generating scheme.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.