Investigation on Power, Delay and Area optimization of XOR Gate

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Abstract: Nowadays a mobile computing and m$_{ul}$timedia applications are need for high-performance reduced size and low-power devices. The multiplication is major operation in any signal processing applications. In any multiplier architecture, adder is one of the major processing elements. In which XOR is the basic block of an adder and multiplier. In this paper, a various design styles of XOR Gate have been surveyed and simulated using Microwind tool. In that XOR gate was analyzed the power using the different styles. They are conventional XOR gate, Pass transistor logic based EX-OR gate, Static inverter based EX-OR gate, Transmission Gate based EX-OR Gate, EX-OR Gate based on 8 & 6 Transistor & and Modified version of EX-OR Gate The CMOS circuit layout was created and simulated in Microwind software. In that the proposed XOR-based circuit has 40.17% of power consumption has improved &14.28 % of area in-terms of number of transistor improved as compare to modified version of EX-OR Gate design.

Keywords: Multiplier, Adder, XOR, VLSI, Microwind.

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1. Introduction

In the present scenario in wireless communication, portable and mobile devices have consistently demanding the designer to design low power consumption and fastest data path computations with low cost device [1][8][9]. Power loss and time delay becomes a major parameter in the integrated circuits, which plays a very crucial role in digital signal processing and communication operations. In any communication and signal processing applications, the adder is a basic building block [2][5]. In that adder consists of AND gate, OR gate and NOT gate. Most of the designers are used XOR only for generating the sum and carry bits. Also XOR gate is fundamental component of many digital circuits. This paper was presented about the various design styles of XOR gates like pass transistor logic, static inverter logic, Transmission Gate logic, XOR gate using 8, 6 and 4 transistors. Analyzed and compared the area, power and speed of XOR gate using above mentioned technique [3][4]. The best one is selected for the full adder design.

2. Design styles of XOR Gate:

2.1. Conventional XOR gate

The exclusive OR Gate is obtained by the combination of standard logic gate (AND, OR and NOT Gate). It is used as building block of an arithmetic logic circuits, computation logic and error detection and correction circuits. The two input XOR gate is performed to modulo two addition of inputs. The output is high, whenever the inputs are not equal and whenever the inputs are equal the output is low[6]. The truth table of XOR gate is shown in Table No.1. The

symbol of XOR gate is shown in Fig No.1 and transistor level implementation is shown in Fig No.2.

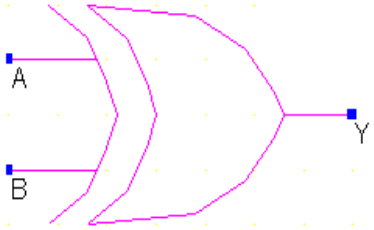

Fig No.1: Symbol of XOR Gate

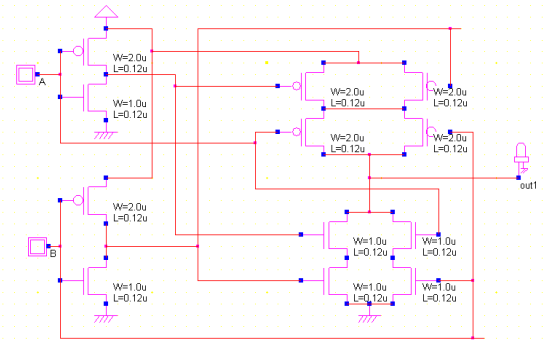

Fig.No.2 Conventional XOR Gate

Table No.1: Truth table of XOR gate

Inputs		Output
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

2.2. Pass transistor logic based EX-OR gate

The pass transistor logic based XOR gate is shown in Fig No.3.This design consumes very little amount of power supply[4]. But does not produced full rail (rail to rail) output of particular input condition. The reason for this poor output is only nMos transistor used in the design. This nMos transistor was produced only good zero, but produces the poor one output.

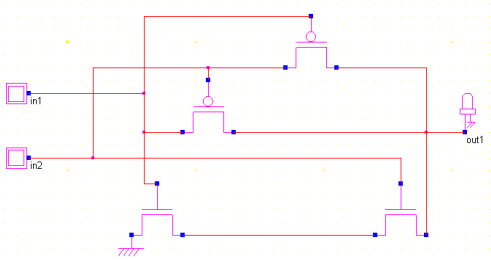

Fig.No.3 Pass transistor logic based EX-OR gate

2.3. Static inverter based EX-OR gate:

The static inverter based XOR gate is shown in Fig.No.4.This design have strong driving capability of input signal. But some of input combinations like 01 is produced poor output voltage level and 00 input combination, the output was produced but need more time (more delay introduced). This delay is the drawback of in this design [4].

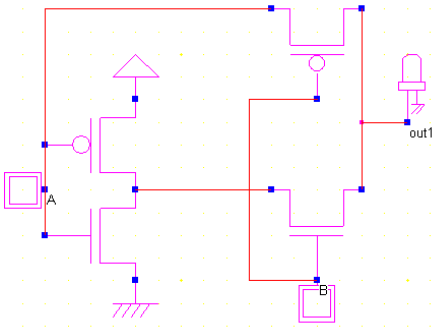

Fig.No.4 Static inverter based EX-OR gate

2.4. Transmission Gate based EX-OR Gate

The Transmission Gate based XOR gate is shown in Fig.No.5. The advantages of transmission gate is produced the full rail output (Strong 0 and strong 1) for the application of input. Because in this design utilized both nMOS and pMOS transistors [4][6].

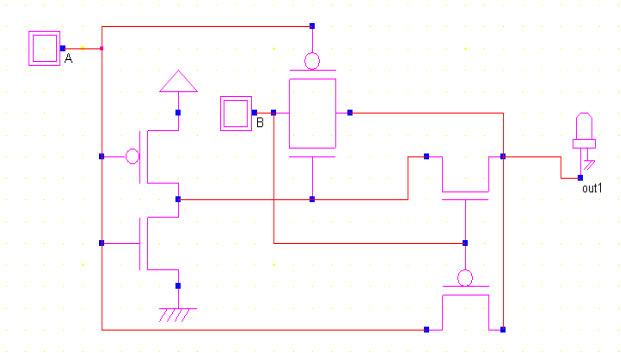

Fig.No.5 Transmission Gate based EX-OR Gate

This design speed is improved in terms of delay and power consumption as compared to above mention techniques. But, due to existence of the static inverter, it occupies more area as compare to above design style.

2.5. Transistor based EX-OR Gate

The 8 Transistor based XOR gate is shown in Fig.No.6.This design was produced the full rail (rail to rail) for the application lower supply voltages[4][7].

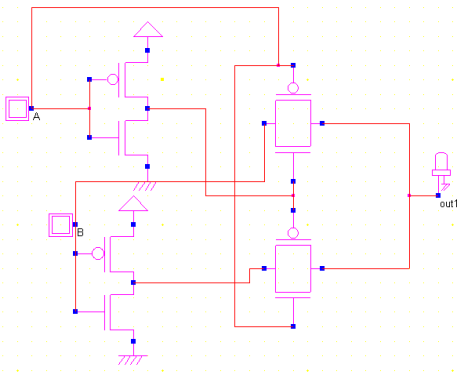

Fig.No.6. 8 transistor based EX-OR

Even though, the output voltage is dropped at high supply voltages. But also it consumed more power as compare to above design, because due to presents of two static inverter.

2.6. Transistor EX-OR Gate based

The 6 Transistor based XOR gate is shown in Fig No.7. This design has good driving capability of output. But it consumes more power and less delay at low supply voltages more specifically [4][10].

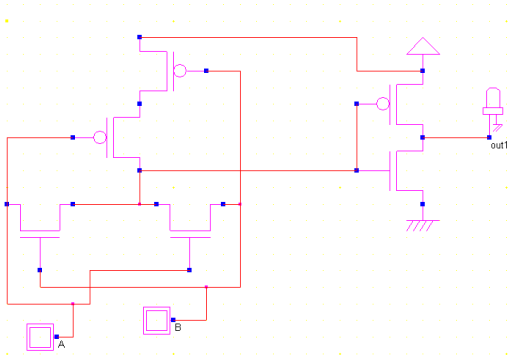

Fig.No.7 6 Transistor based EX-OR Gate

2.7. EX-OR Gate based on 4 Transistor

The 4 Transistor based XOR gate is shown in Fig.No.8.In this design 4 transistor(2 nMos and 2 pMOS) are used for design of XOR gate. This design is efficient in terms of power consumption as compared to all the above technique. But it has low speed of operation in terms of delay characteristics[4][6][7].

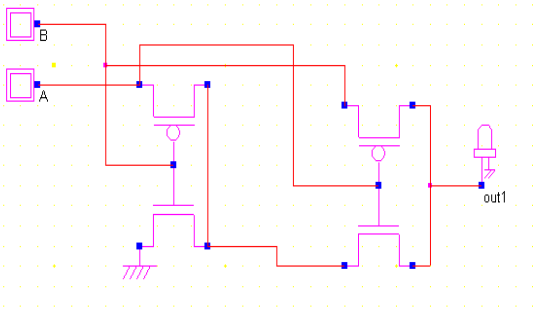

Fig.No.8 EX-OR Gate based on 4 Transistor

2.8. Modified version of EX-OR Gate:

The modified version of XOR gate is shown in Fig.no.9 In this design style only 4 transistors (2-nMOS & 2-pMOS transistor) are used and also introduced static keeper circuit to improve the output level[4][6][7]. It has further improved the consumption of power as compare to above existing styles.

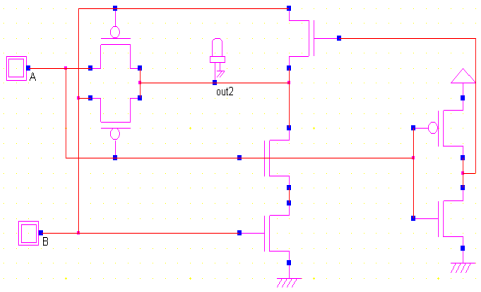

Fig.No.9 Modified version of EX-OR Gate

2.9. Proposed EX-OR Gate:

The proposed XOR gate is shown in Fig.No.10. This design is modification of normal static logic. In this design style only 4 transistors (2-nMOS & 2-pMOS transistor) plus normal static inverter are used. It is further improved the power consumption and area wise as compare to above design technique.

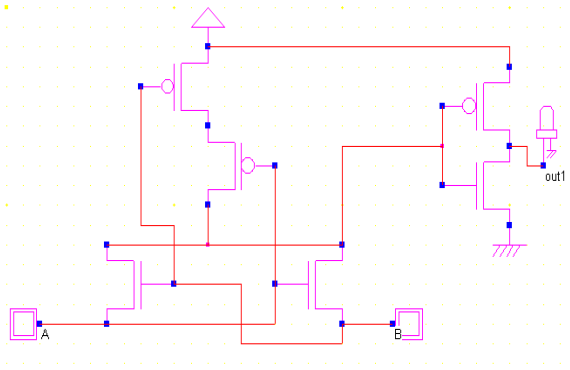

Fig.No.10 Proposed EX-OR Gate

3. Simulation Result

The proposed XOR gate is designed using Microwind DSCH simulator and synthesized using Standard CMOS circuit 90nm technology. And also the layout was generated using Microwind software from the Verilog file which is generated by DSCH Microwind software. The power, speed in-terms of rise and fall time delay and area in-terms of number of transistor is measured and analyzed for different styles of XOR Gate. The Table No.2 shows that consumption of power, area utilization and delay for various styles of XOR gate design. The Fig.No.11 & 12 Shows that layout and simulation result of proposed XOR gate. In that the proposed XOR-based circuit has 33.6% of power consumption has improved & 22.7 % of area in-terms of number of transistor improved as compare to Modified version of EX-OR Gate design styles. The graphical analysis for Power, Area and Delay of XOR gate is shown in Fig.No.13, 14 and 15 respectively. The Fig.No.16 shows that tradeoff between area, power and delay of XOR gate.

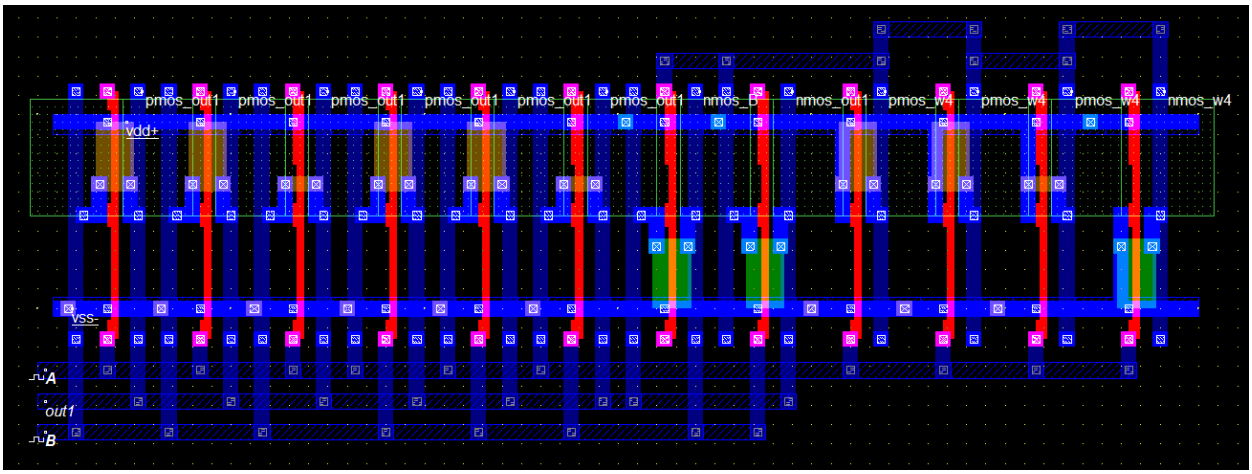

Fig.No.11 Layout of proposed XOR Gate

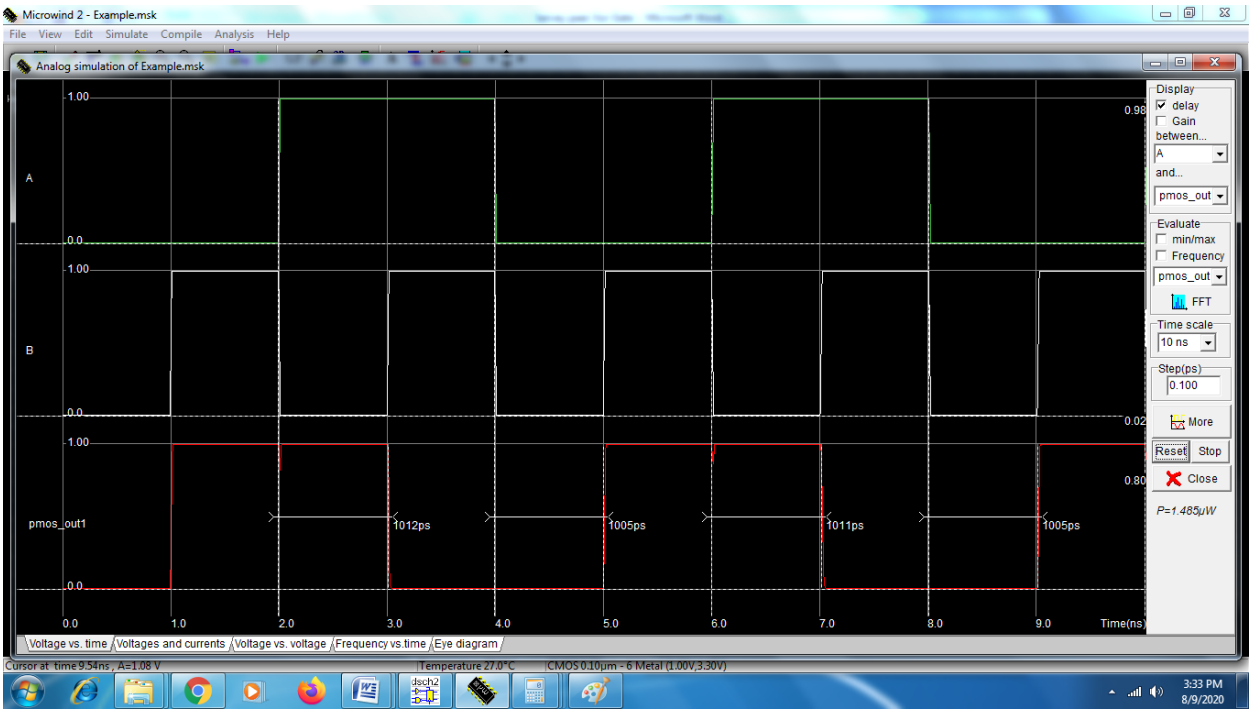

Fig.No.12 Simulation Results of proposed XOR gate.

Table No.1: Comparison Results of Various design Styles

Design Style	Power Consumption (uW)	Area (No. of Transistor)	Fall time delay (ps)	Rise time delay (ps)	Total Delay (ps)
XOR gate conventional	3.24	12	58	38	48.00
Pass transistor logic based XOR	-	4	7	12	9.50
Static inverter based EX-OR gate	1.80	4	7	58	32.50
Transmission Gate based XOR	2.62	6	9	22	15.50
EX-OR Gate based on 8 Transistor	7.97	8	16	12	14.00
EX-OR Gate based on 6 Transistor	9.48	6	55	21	38.00
Modified version of EX-OR Gate	2.23	7	10	12	11.00
Proposed EX-OR Gate	1.48	6	5	12	8.50

4. Conclusion

In this paper a new XOR gate was proposed, designed and compared with the various circuit design styles in terms of power consumption, delay, and area in-terms of number of transistor. The transistor level XOR gates is designed and simulated in DSCH micro wind software using CMOS 90nm technology. The CMOS circuit layout is created and simulated in Microwind software.

In that the proposed XOR-based circuit has 40.17% of power consumption has improved &14.28 % of area in-terms of number of transistor improved as compare to Modified version of EX-OR Gate design style. Further, this design can be extended to test the different adders, multiplier, and filters and signal processing module. Also it is possible to optimize the performance of ALU, DSP processors and data path modules using proposed design.

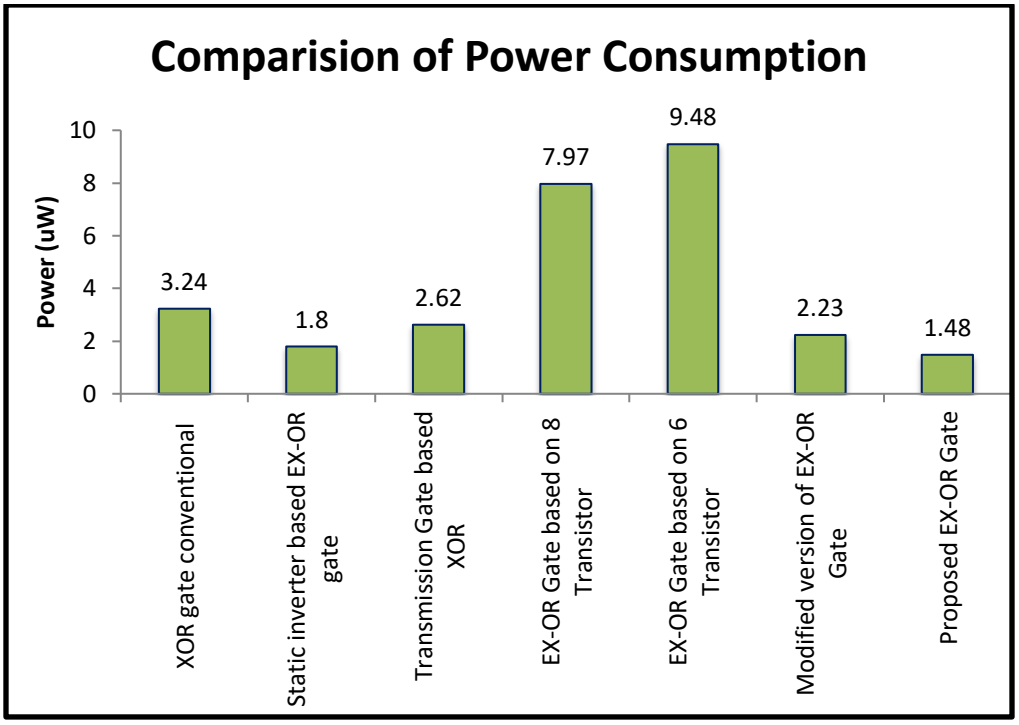

Fig.No.13 Comparison chart for Power Consumption of XOR Gate

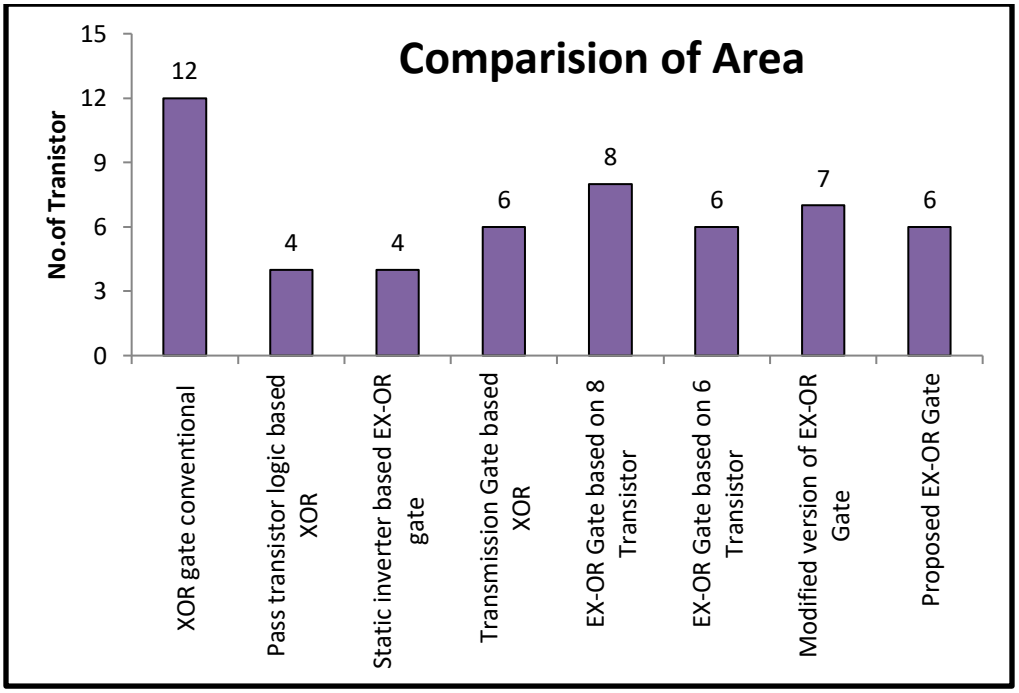

Fig.No.14 Comparison Chart for Area Utilization of XOR Gate

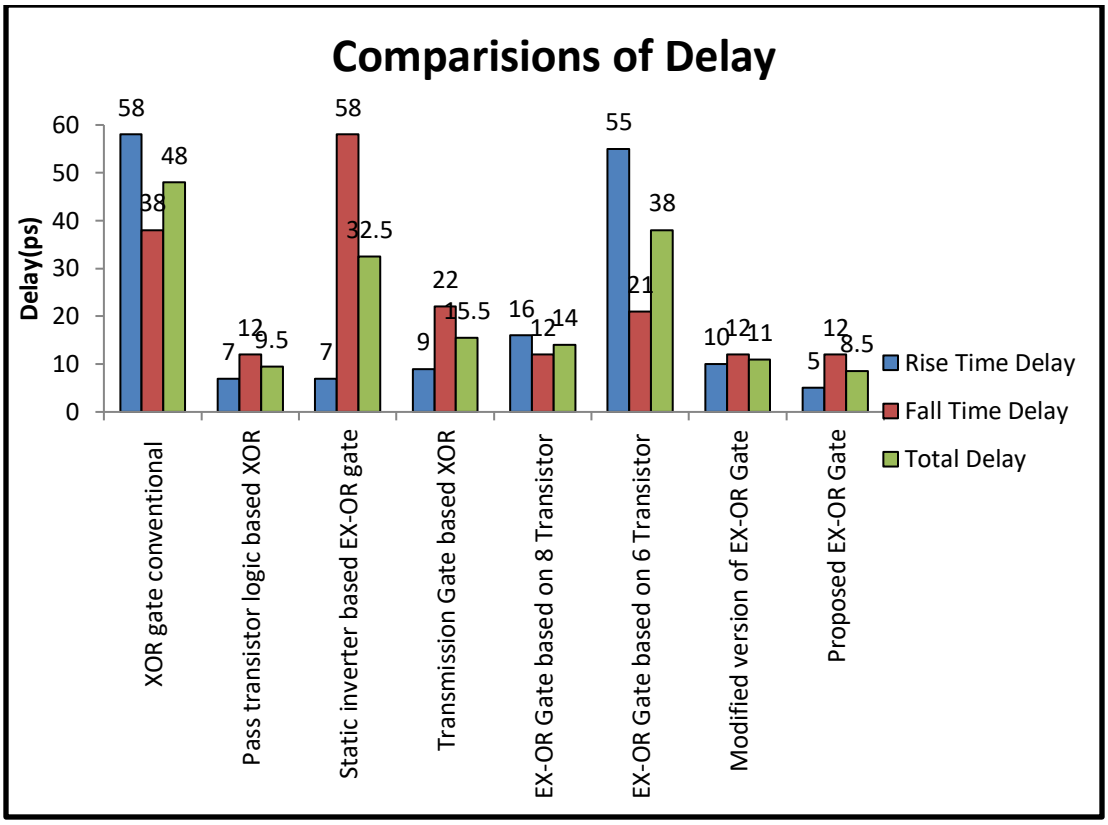

Fig.No.15 Comparison Chart for delay of XOR Gate

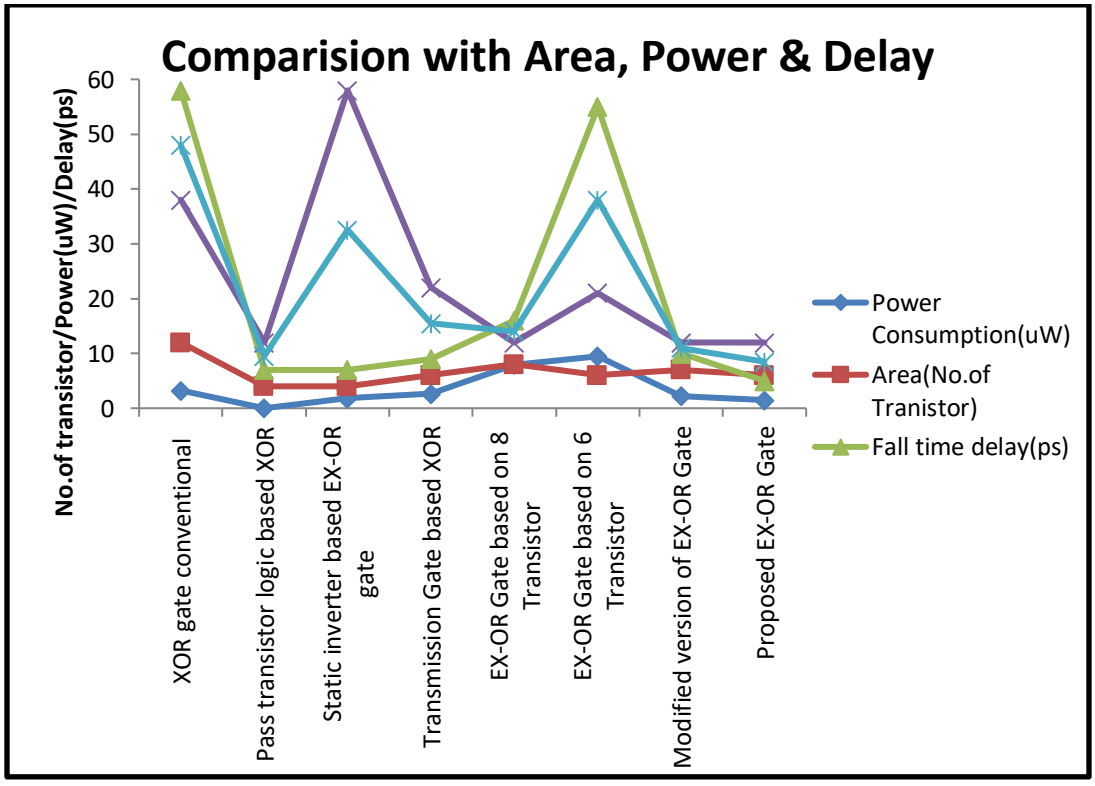

Fig.No.16 Tradeoff between Area, Power and delay of XOR Gate

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