

# Measurement Method for the Dynamic On-State Resistance of GaN Semiconductors

MICHAL ŠÍR

Faculty of Electrical Engineering and Communication  
Brno University of Technology  
Technická 3058/10, 61600 Brno  
Czech Republic  
michal.sir@psbel.com  
<http://www.vutbr.cz>

IVAN FEŇO

Research and Development  
Bel Power solutions GmbH  
Ackerstrasse 56, 8610 Uster  
Switzerland  
ivan.feno@psbel.com  
<https://www.belfuse.com/power-solutions>

*Abstract:* - Defects in material structure effects the ON-state resistance of GaN devices, which can't be considered constant in power loss evaluation when considering high operating frequency. The aim of this article is to propose a novel method to measure the dynamic RDSon. The method resolves a typical disadvantage of former methods e.g. an unclear clamping diode voltage drop in former approaches. Test results obtained with the new method are presented for 3 samples provided by different suppliers. Results shows that each sample exhibits a different dynamic RDSon characteristics what indicates a different process technology used to manufacture the device.

*Key-Words:* - GaN semiconductor, Novel RDSon Measurement method, Dynamic On state resistance, Dynamic RDSon

## 1 Introduction

In the last few years amount of available GaN switching devices for power electronic applications significantly increased. A number of emerging devices with a different internal structure shows a growing tendency. Devices are offered not only by small/startup companies but also by well-known manufacturers of semiconductors. The higher bandgap of Gallium Nitride (3.4eV) material offers potentially higher operating temperatures, fast switching capability and therefore generate less power loss than widely used silicon or SiC devices.

General requirements on power conversion systems are moving to smaller, higher dense solutions (60-100W/inch<sup>3</sup>) to reduce the overall size of the system and cost of the power supply. The power loss in a semiconductor switch can be in general divided in two parts: switching and conduction power loss:

$$\Delta P = \Delta P_{Sw.} + \Delta P_{Cond.} \quad (1)$$

The switching power loss  $\Delta P_{Sw.}$  is defined by energy dissipated during switching event multiplied by switching frequency. The conduction loss  $\Delta P_{Cond.}$  is defined as a product of squared effective current and resistance in conductive state of semiconductor device. It is assumed the switching loss is linearly increased with switching frequency and conduction

loss is in many cases considered to stay constant – as the on-state resistance and effective device current remains the same over the frequency. As shown further in the article, due to defects in the semiconductor structure, the on-state resistance of a device is not constant and should be considered nonlinear at higher switching frequencies.

## 2 Theory of Measurement

In order to obtain a plot of the dynamic on-state resistance during a device operation cycle in a power electronic circuit, the Ohm law is applied:

$$v_{DS(t)} / i_{DS(t)} = r_{DSon(t)} \quad (2)$$

The current through the device  $i_{DS(t)}$  and the voltage over the drain source terminals  $v_{DS(t)}$  are measured during the device switching operation. Let's consider following conditions for further analysis:

- a typical CCM operation
- the  $v_{DS(t)}$  high voltage transition has settled before the  $r_{DSon(t)}$  is measured
- inductor with a low inter-winding capacitance is used to connect the device switching node with the rest of the circuit

In this case we can consider the current through the device constant in a short time scale and the bandwidth of the current probe not critical. Therefore, a 50MHz BW current probe used in the inductor path is sufficient to emulate the device current. This allows to avoid the current sensor in the switching loop what is essential for a representative emulation of the normal device operation.

Sensing of the  $v_{DS(t)}$  voltage is however a critical point. During device off time, the  $v_{DS(t)}$  voltage reach a level of hundreds of volts while after a switch-on transient the  $v_{DS(t)}$  quickly drops to few millivolts. Therefore it is essential to use a  $v_{DS(t)}$  sensing with a high dynamic range. Taking account the speed requirements, the task is getting quite challenging.

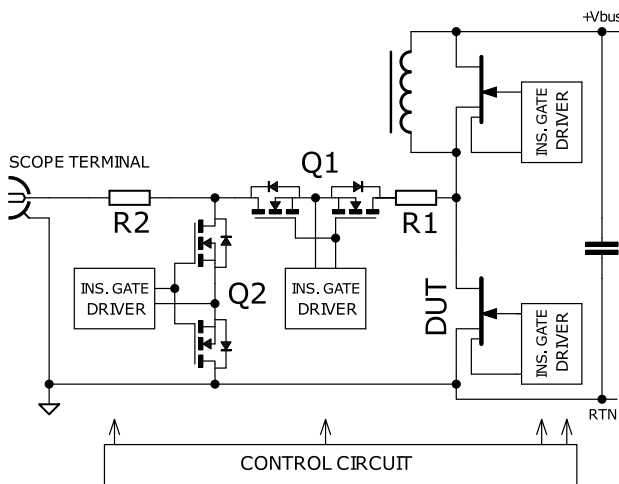


Fig. 1. Block diagram of dynamic  $R_{DS(on)}$  measurement setup

An alternative option is to use a clamping circuit which protects the  $v_{DS(t)}$  sensing device to saturate in off-state and enables the transfer of a signal in mV range to the sensing device in on-state conditions. Typically, a HV signal diode is used to clamp the  $v_{DS(t)}$  voltage as shown in [3][4][5]. The common issue of this solution is the diode drop voltage which is not easy to characterize / calibrate taking account the very fast transient conditions the diode is exposed to. To avoid issues mentioned above a novel clamping circuit was developed.

The circuit features following advantages:

- Very low impedance clamping capability to block the high voltage propagation into the sensing device
- Effectively zero-voltage drop between the DUT and the  $v_{DS(t)}$  sensor resulting in precise  $R_{DS(on)}$  evaluation
- A capability to measure  $r_{DS(on)}$  down to 70-100ns after the DUT switch on
- A high  $r_{DS(on)}$  sensing BW

### 3 Description of Test Setup

The proposed  $r_{DS(on)}$  tester (Fig.1) consists of two parts – the power circuit and the measurement circuit.

#### A. Power circuit

To get test conditions which are relevant and as close as possible to the end application of the semiconductor device, the power circuit of the tester consists of a half-bridge, which is common for power topologies (totem pole PFC, DCDC converters, inverters, etc). For the gate control a fast gate driving circuits are used. Both HS and LS switch drivers are equipped with isolated power supplies to avoid parasitic noise coupling into the control and signal sensing circuits.

#### B. Measurement circuit

The measurement block of the tester consists of two low capacitance switches (Fig.1): A clamping device Q2 which protects the scope input from saturation during DUT off-state and a coupling switch Q1 which connects the  $v_{DS(t)}$  to the scope input during DUT on-state.

The Q1 is rated to withstand the bulk voltage +Vbus which supplies the HB circuit of the tester. The switch is turned off during DUT off time. It is important to select a device with a very low Qoss capacitance to minimize the capacitive current flowing through the clamping switch Q2 during switching transients. Two 500V rated silicon FETs in anti-series configuration are used to meet requirements.

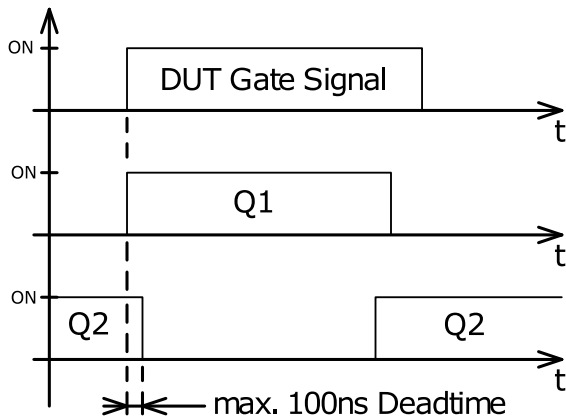


Fig. 2. Switching diagram of Q1 and Q2 vs. DUT timing

Two low voltage EPC GaN transistors (Q2) are used to clamp the  $r_{DSon(t)}$  voltage during DUT off-state. Low Qoss of these GaN devices is essential to keep parasitic capacitance in the measurement signal path low, because the Qoss together with series resistors (R1, R2) operates as a low pass filter in the signal path.

Referring to Fig.2 the operation of the tester is explained by control waveforms which ensure the scope input is protected from the HV overload and can detect  $v_{DS(t)}$  at 20mV/div setting. The series resistors in the signal path are designed to provide required SWR and therefore a relatively flat transfer function. The 50Ohm scope termination together with series resistors in the measurement signal path creates however a voltage divider which is taken account in on state resistance calculation.

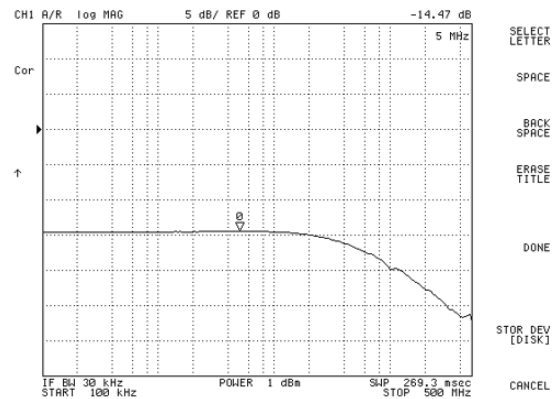


Fig. 3. Transfer function of the measurement signal path

To obtain a maximum measurement precision the  $v_{DS(t)}$  voltage sensing is calibrated in DC mode. Fig.3 shows the transfer function of the signal path between DUT drain-source terminals and the scope input in range of 500MHz, measured by the network analyser Agilent 4395A. Signals for gate drivers are generated by TI Picollo DSP.

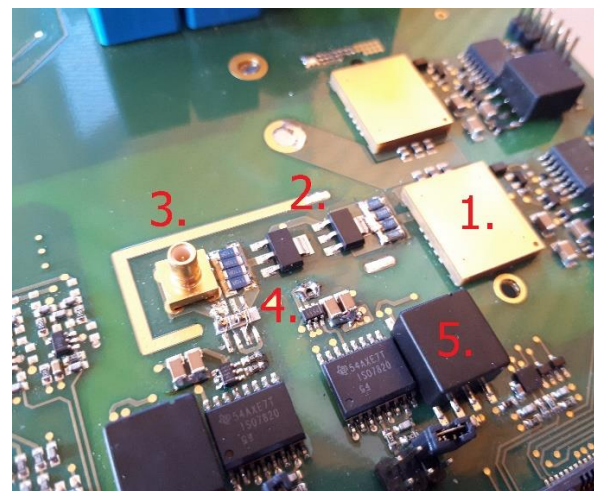


Fig. 4. Detail of the proposed tester (during sample #2 test)

- 1. - Device under test, 2. - Q1, 3. - Scope terminal,
- 4. - Q2, 5. Gate Drivers

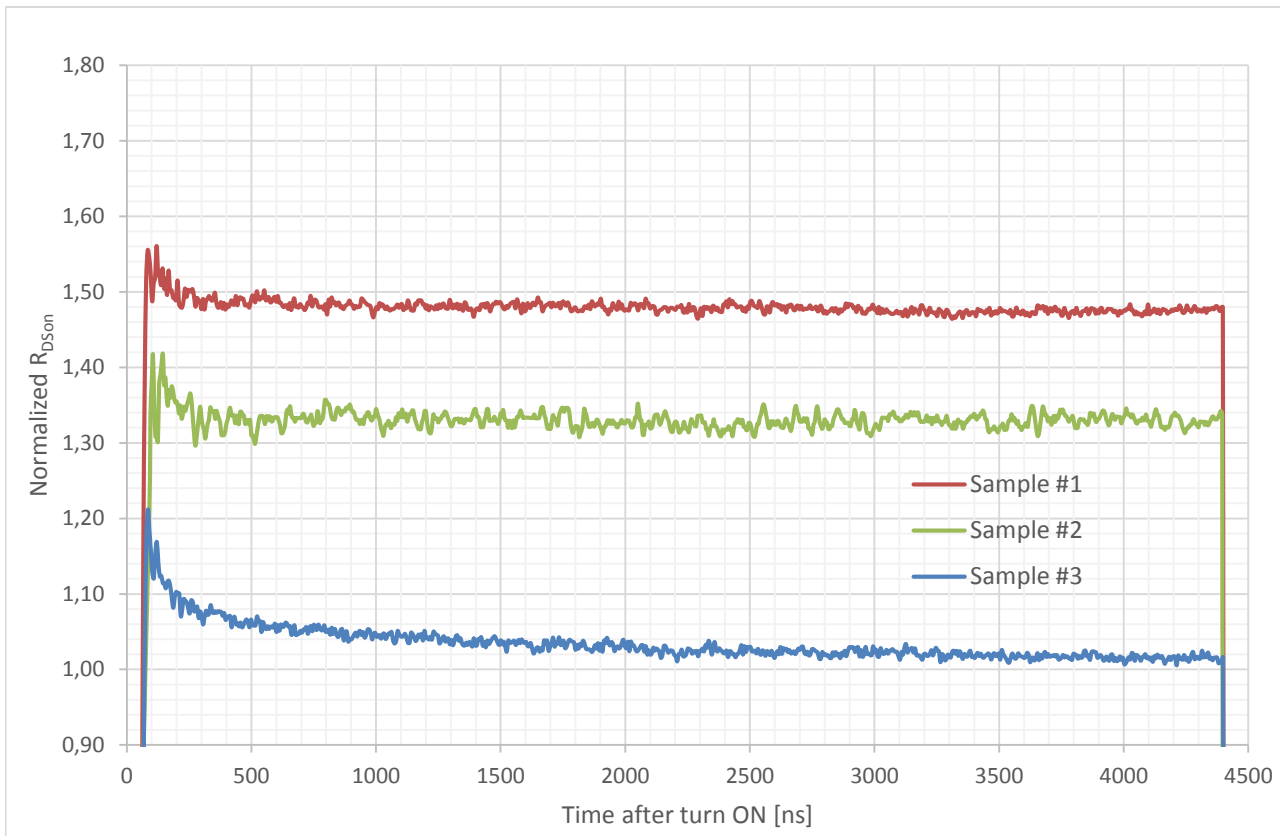


Fig. 5. Plot of  $R_{DS(on)}$  vs. time after turn-on of three tested samples, test voltage 200V

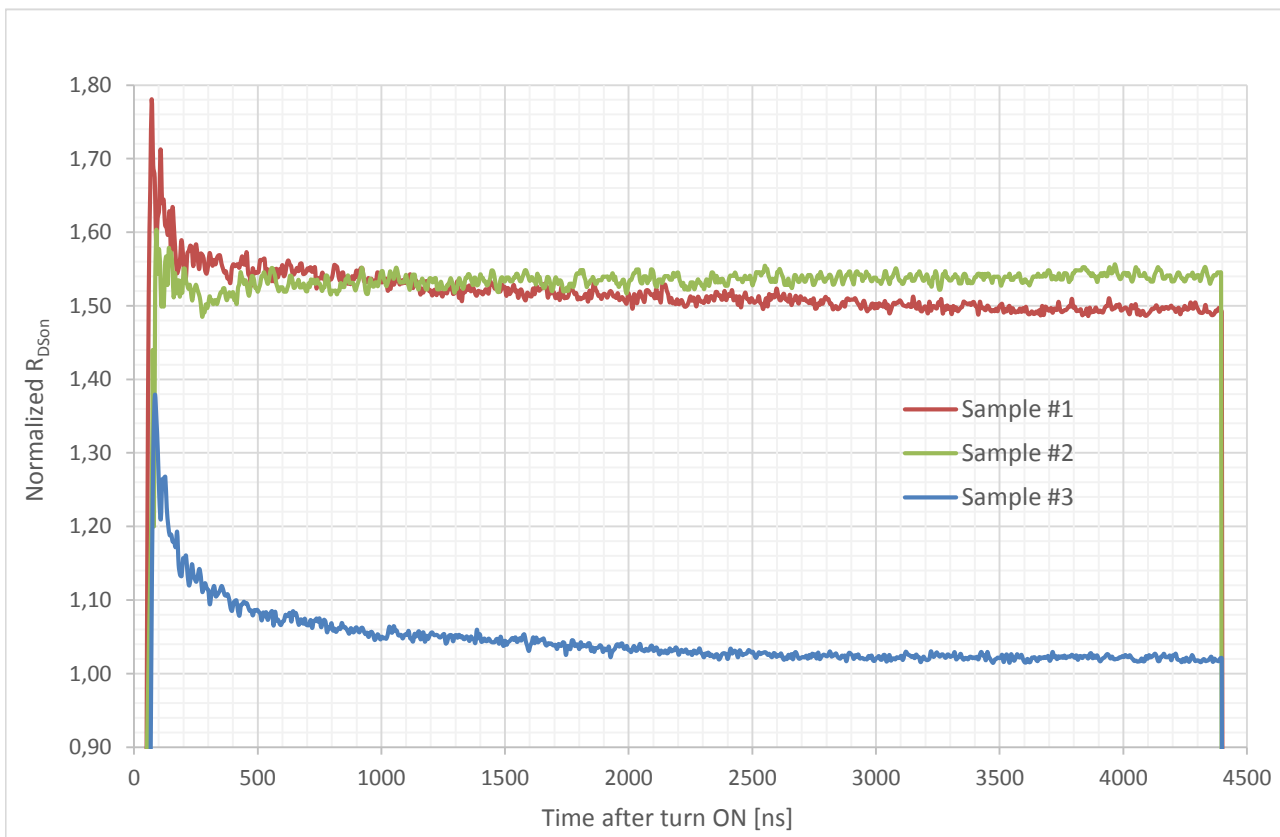


Fig. 6. Plot of  $R_{DS(on)}$  vs. time after turn-on of three tested samples, bulk voltage 400V

## 4 Test Results

Three samples of GaN transistors from three different manufacturers were tested. The test was conducted at 2 different bulk voltage levels. The test sequence consists of three switching cycles to increase the current through the choke to the test level. The voltage and current data acquisition is conducted during the last pulse sequence. The length of the pulse sequence, the peak current and the test voltage is for all samples the same. Consequently the  $r_{DSon(t)}$  plot is constructed starting shortly (70-100ns) after DUT turn-on transient. Because all tested devices have a different static  $R_{DSon}$  figure, the resistance displayed in graphs is normalized to the value in steady state (DC conditions) to emphasize the comparison (Table 1). The  $R_{DSon}$  in steady state is matching the datasheet specification for all samples (note the datasheets are often preliminary and manufacturers continuously updates the data). Fig. 6 summarize  $r_{DSon(t)}$  results while  $v_{DS(t)}$  in off-state is a parameter.

Based on test results the following findings can be formulated.

### A. Short transient increase

A short transient/dynamic on state resistance was detected for samples #1 and #3. This behaviour is affected by the test voltage (e.g. voltage present on a DUT before the turn-on transient). The effect is more pronounced at high test voltage. Sample #2 however does not exhibit the short transient increase.

### B. Long transient increase

A long transient increase is detected on sample #1 and #2, where the on-state resistance drops down to the static value over a long time (time range couple of *ms*). The only sample with no long transient increase is the sample #3.

Because all tested samples have a different internal structure, the mechanism of dynamic  $R_{DSon}$  is likely different. Root cause for the dynamic  $R_{DSon}$  is the electron trapping in crystal defects [1], however test results indicate that each provider of the sample handles the electron trapping in a different way.

The conclusion is all samples will exhibit an increased conduction loss in the application and the effect cannot be predicted from the manufacturer's datasheet.

On the other hand the relative increase will be more significant at higher operating frequencies (>1MHz) in case of sample #3. In case of sample #1 and #2 the increase is permanent during the on state.

Table 1. Part Numbers and Catalogue  $R_{DSon}$  of tested samples

Sample	Part Number	Datasheet $R_{DSon}$	Normalized/DC $R_{DSon}$
#1	GaN Systems GS66506T	67m $\Omega$	61m $\Omega$
#2	VisIC V22N65A	22m $\Omega$	22m $\Omega$
#3	Panasonic PGA26E07	56m $\Omega$	55m $\Omega$

## 4 Acknowledgment

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