RF PAD De-Embedding in CMOS Active Cascode Inductor Design

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Abstract: The rapid advancement of CMOS technology in the last decade has made possible CMOS implementation of radio frequency (RF) integrated circuits. However, the limitation of the passive integrated inductors is still a huge limitation. Integrated inductors take significant chip area, have low inductance values and unsatisfactory quality factors (Q). As a solution, active inductors have been proposed. In this work, the de-embedding technique is applied in the design of an integrated active inductor in CMOS technology for RF systems, in order to analyze and eliminate all external influences to the designed element.

Key–Words: active inductor; RF; integrated circuit; CMOS; de-embedding technique.

1 Introduction

The CMOS electronics applied to analog RF circuits has been highlighted among research topics related to microelectronics. Many technologies have been explored searching for compact circuits with efficient and cost-optimized production.

Several microelectronic topics can still be subject of researching, with a particularly interesting one, the study of inductors. Planar passive inductors take significant area on the chip and do not present satisfactory performance (poor Qs and reduced inductances mainly) [1, 2]. The investigations about the AIs (active inductors), which are, in essence, transistors operating in a feedback mode, have become more intense to overcome these problems. In this way, topologies have been designed for different RF applications, such as amplifiers [3, 4, 5, 6, 7], oscillators [8, 9, 10], filters [11, 12] and quadrature generators [13].

Accurate on-wafer measurements of S-parameters are fundamental in the characterization of RF devices. Therefore, the accurate analysis of these parameters represents an essential role in the design of RF devices and circuits. The measurement of these parameters can only be obtained when it is connected directly to the calibration plan. However, there normally are extra elements for connection between the calibration plane and the DUT (device under test), as a rule, PAD interface ones [14].

Thus, an accurate analysis of the S-parameters of the DUT not only requires a proper calibration of the measuring equipment, but also needs to consider the interface effects introduced by the pads [15] and bias wirebonds. To subtract the interface effects, and thus, obtain only the S-parameters for the DUT, the de-embedding scheme must be applied.

In this context, the focus of this work is the application of the de-embedding scheme at the design level of an integrated CMOS AI to operate in RF systems. This technique is employed to eliminate all external influences in the designed element, and thus, ensure their full analysis and characterization. Normally, the de-embedding scheme is a technique used at prototype level so, in this work, we change this concept bringing this analysis at the design level.

The paper is organized as follows: Besides this introductory section, the de-embedding scheme is shown in section 2, the AI design is presented in section 3, main results are considered in section 4, and finally, section 5 concludes the work.

2 De-embedding scheme

A schematic simulation model can describe the device characteristics in an accuracy way, only if all parameters have been extracted from the analyzed data

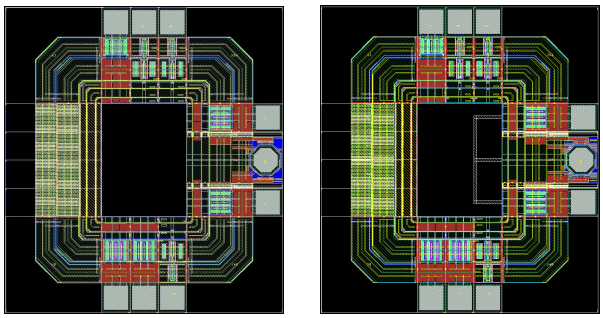
of the system. To extract the parameters of the circuit, results in RF on-chip are performed using specifically designed test structures. Moreover, the de-embedding scheme must be applied to remove the influence of the interface test structures. Thus, from the system raw data, the performance of the DUT is obtained [15, 16, 17].

In essence, the de-embedding scheme is a mathematical process that removes the effects of unwanted parts of the structure built on the collected raw data, subtracting their influences [18]. However, to ensure the accuracy of the analysis, the system calibration must be done before any measurements on the DUT. The calibration system used on wafer measurements can be performed by some calibration methods such as: ISS (impedance standard substrate) SOLT (short-open-load-through) and TRL (through-reflect-line). Besides, the system calibration, the de-embedding scheme for raw data from the DUT needs to be developed based on test structure designed according to the one to be effectively analyzed.

A most popular de-embedding approach is the so-called open de-embedding, which simply removes the effects of the pads from the measurement structure, by subtracting the measured Y parameters of the pad from the measured device. The key assumption is that the pads are connected in parallel to the DUT, which neglects the physical nature of the pads and treats the signal entry/exit points as lumped circuit nodes [19].

The other assumption for in the open de-embedding is that we can indeed measure a true pad open structure by simply open circuiting the pad test structure. In summary, open de-embedding removes the shunt parasitics from the measured device. As the frequency increases, open de-embedding is not sufficient to de-embedding all the parasitics, and a more common approach is the so-called open-short de-embedding. For this, a short structure is also measured.

To obtain accurate results, it is important to remove the additional elements introduced by the complementary test structures. For it is necessary to measure known properties of structures separately and then apply matrix properties to eliminate the influence of interface elements (resistances, capacitances, and inductances) of the RF-PAD. In Figure 1 is shown the layout of the chip in open and short mode to perform the measurements of the S-parameter, and subsequently, be able to apply the de-embedding scheme to remove the RF-PAD interface elements.



(a) (b)

Figure 1: Setup test for S parameter measurements: (a) Open ; (b) Short (980 x 1080 mm).

3 AI design using De-embedding scheme

The designs were developed using the Keysight ADS (Advanced Design System) with simulation models of AMS (Austria MicroSystems) foundry in CMOS 0.35 μm technology [20]. This technology has four metal levels, four polys, and the substrate is P-type, with thickness between 710 and 740μm.

3.1 AI without PAD interface

AIs are based on the operation of a feedback circuit known as gyrator-C. The AI designed in this work is based on the cascode topology. To increase the output resistance of M1 in gyrator is to add a third transistor, M3 , between the drain of M1 and the gate of M2.

In this way, this topology is called Thanachayanont-Payne cascode AI [21] and its input impedance is given by Equation 1, where C_{gs}, g_m, and g_o are the gate-source capacitance, transconductance of transconductor, and output conductance respectively [22]. In Figure 2 is shown the schematic of the designed AI.

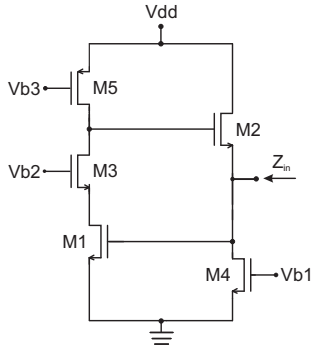


Figure 2: Classical cascode AI.

$$Z \approx \left(\frac{g_{o1}g_{o3}}{C_{gs1}C_{gs2}g_{m3}}\right)\frac{s\left(\frac{C_{gs2}g_{m3}}{g_{o1}g_{o3}}\right)+1}{s^2+s\left(\frac{g_{o1}g_{o3}}{C_{gs2}g_{m3}}+\frac{g_{o1}}{C_{gs1}}\right)+\frac{g_{m1}g_{m2}}{C_{gs1}C_{gs2}}} \quad (1)$$

This topology offer the following attractive characteristics :

- Frequency range expansion by lowering the lower bound of the frequency range;
- Quality factor improvement by lowering the parasitic series resistance R_s and increasing the parasitic parallel resistance R_p;
- No reduction in the upper bound of the frequency range;
- No reduction in the inductance.

The transistors M1, M2, and M3 are the AI core, with the primary function to perform the phase rotation. On the other hand, the transistors M4 and M5 are the bias current sources. The size of the transistors M1, M2, M3 and the current generated by M4 and M5 have been calculated in such a way as to keep the all transistors in the saturation region. The size of all AI transistor gates are fixed W=5μm and L=0.35μm. After the optimization process by ADS tuning interaction, the respective number of gates are: M1=M2=10, M3=M4=5, and M5=4. Completing the design parameters, the bias voltages are: Vb1=0.95V, Vb2=1.80V, Vb3=2.30V and Vdd=3.15V. The power consumption obtained in the simulation for typical values was 3.10mW.

3.2 AI with PAD interface

To simulate the fully cascode active inductor, some elements have been inserted to make the simulation environment more realistic as possible. The complete simulation model is shown in Figure 4. In this case, the use of an accurate RF-PAD model is crucial for a trustful circuit design and several problems can emerge by using a noun precise model for the PADs [23, 24]. Since it is impossible to characterize an isolated PAD, a complete GSG structure must be built, for the extraction of the parameters that will be used in the model. This is necessary, in order to take into account all the RF effects in the structure.

The equivalent circuit for RF-PAD take into account ESD (Electro Static Discharge) protection and the parasitic elements of the structure is shown in Figure 3 [25]. In this work, a 150μm pitch (distance between center of adjacent pads) structure in a GSG configuration was adopted. Also, the model used is not taken into account the microprobe contact resistance, due to the contact resistance of a new microprobe, normally, has a negligible value (supposition at this design level). Its typical value is about $< 0.05\Omega$ on Al [26]. The concentrated parameter values of the equivalent circuit depend on the used technology. In this case, the optimized results using the schematic of Figure 3, as a reference are: CPad=0.53pF, R=4Ω, and C=0.1pF.

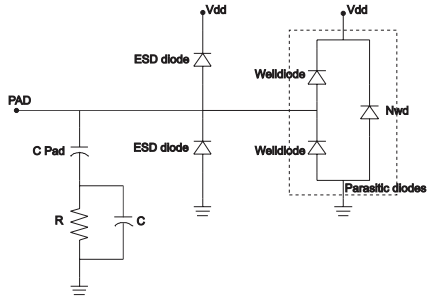


Figure 3: RF-PAD equivalent circuit for GSG structure.

Finally, the RF-PAD model was embedded in the simulation PAD. It is through this pad that the measures of the S-parameter of the active inductor are obtained. The bias pad is modeled by a resistor and a capacitor, shown in Figure 4. The capacitance of the pad appears due the stacking of metals, having value around 1.3 pF. The resistance of the pad should provide and additional impedance to protect the gate of the transistors against the ESD, having the value of 2.1 kΩ.

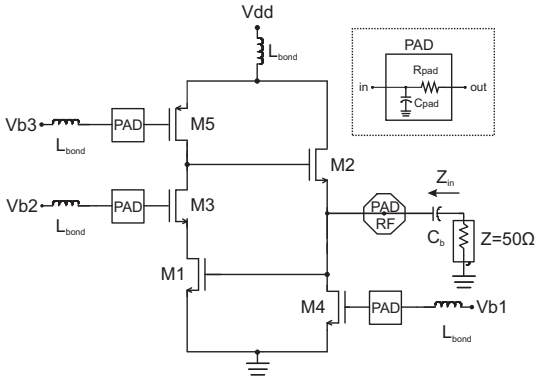
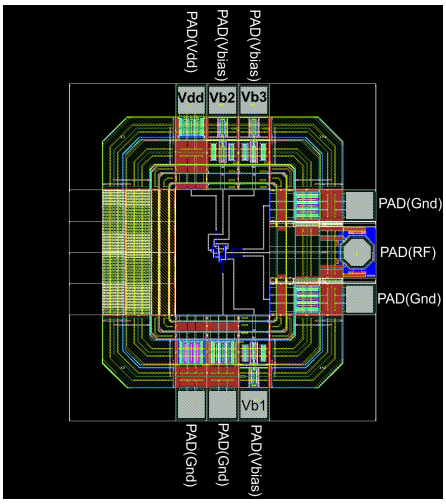


Figure 4: Cascode active inductor - Fully schematic simulation model.

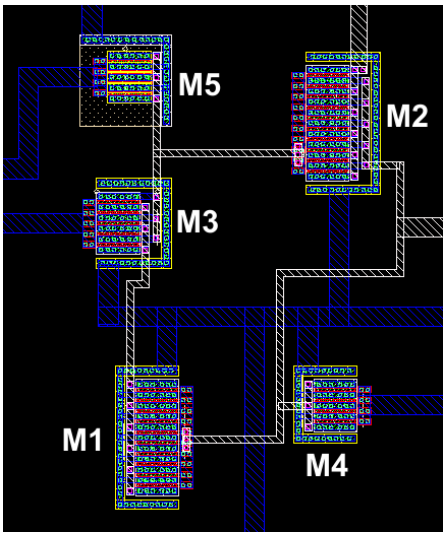
The wirebond also had its effect considered, which typically have an inductance of 0.7nH/mm. In Figure 4, it is represented by L_{bond} and its equivalent value is 1.4nH (2mm).

Thus, the de-embedding scheme can be applied to this entire structure to remove the effects incorporated in the raw data. The final response should be the performance of the active inductor itself (AI without PAD interface).

Once the design of the cascode active inductor was optimized, the layout of the integrated circuit was also performed. The dimensions involved in the layout design must follow rules imposed by the AMS foundry. All of these ones are organized in [27]. The layout of the proposed active inductor is shown in Figure 5, which present the interconnections, as well as, the layout of the IC with protection ring and different types of pads.



(a) Active inductor layout (980 x 1080 μm).



(b) Layout details (72 x 67 μm).

Figure 5: Active inductor layout.

4 Analysis of Results

It is performed three different simulations to present the application of de-embedding scheme at the design level, using for it, the S-parameters of calibration structures and the circuits with and without the interface. Simulation results are presented and compared in Figure 7 for AI without RF-PAD, original element, (shown in Figure 2), AI with RF-PAD (Figure 4), and RF-PAD de-embedded (Figure 6).

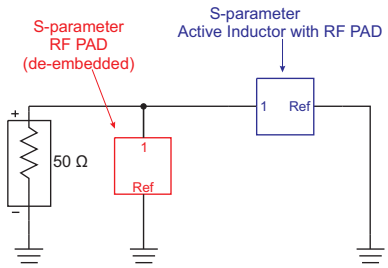


Figure 6: Simulation schematic to apply de-embeeding scheme.

The AI with RF-PAD simulation is crucial for predicting the on-wafer S-parameter measurements. Observe that, on the results of these simulations, the RF-PAD degrades the performance of the device due to its layout specific capacitive and resistive interface. The RF-PAD de-embedded simulation returns the real active inductor performance without its degradation due to the interface. As expected, a significant difference between the data before and after de-embedding has been observed due to the interface. The simulation results of AI without and with RF-PAD (after de-embedding) are in close agreement. The Q parameter is the only one that presents a little variation and this one is foreseen here at the design level. The advantage is that its value can be optimized, if necessary, at the design level.

Table 1 presents a synthesis of the obtained results for the AI cascode. The evaluated variables were: Self Resonant Frequency (SRF), maximum Q (Q_{max}), frequency for which it was obtained the maximum Q (f_{Qmax}), maximum obtained inductance (L_{max}) and frequency for which it was obtained the maximum inductance (f_{Lmax}).

Table 1: AI simulations - Synthesis of results

$Simulation\ Circuit$	$SRF\ (GHz)$	Q_{max}	$f_{Qmax}\ (GHz)$	$L_{max}\ (nH)$	$f_{Lmax}\ (GHz)$
AI with RF PAD	1.68	71	1.06	86.14	1.63
RF PAD de-embedded	2.59	158	1.11	25.56	2.14
AI without RF PAD	2.60	162	1.12	24.78	2.15

From the simulation results shown in Table 1, the AI without RF PAD has an inductive reactance up to

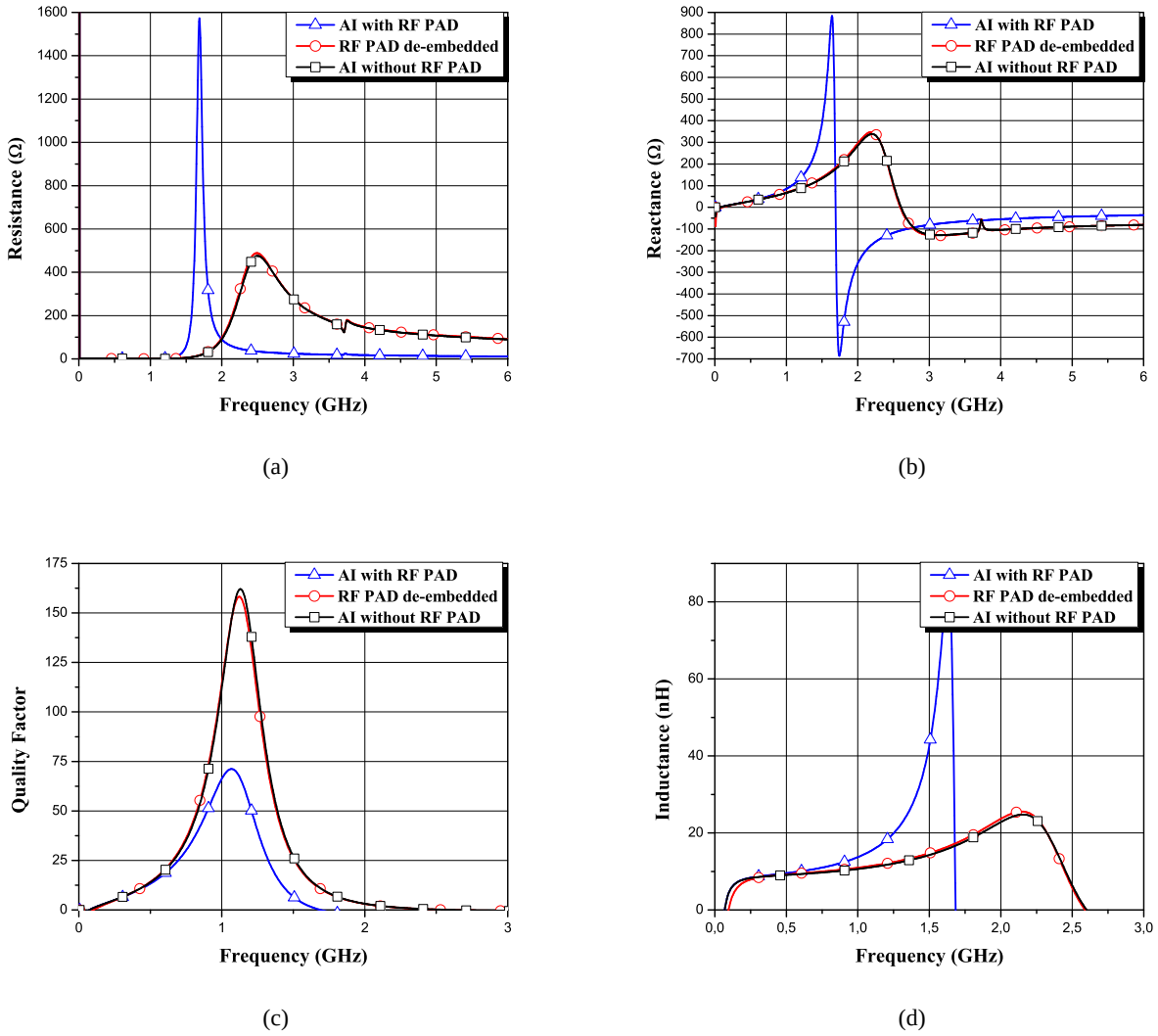


Figure 7: Active inductor results at de-embedding scheme design level.

frequency of 2.60 GHz (SRF). This AI has a high quality factor in a wide frequency range, reaching the maximum value of 162 at 1.12 GHz and a maximum inductance of 24.78 nH at 2.15 GHz. In the AI with RF PAD we can verify that there is a decrease in the self resonant frequency and quality factor, however there is an increase in inductance, in comparison with the AI without RF PAD.

The analysis of these three basic simulation conditions together at the design level is useful for predicting circuit performance with accuracy. This approach is employed to eliminate all external influences in designed element, and thus, ensure their full analysis and characterization. Normally, the de-embedding scheme is a technique used at prototype level so, in this work, we change this concept bringing this analysis at the design level.

This design proposal is interesting to verify if the de-embedding procedure is satisfactory and how it affects the performance of the device. Without this simulation, errors or problems in the de-embedding scheme can result in design problems and, thus, the fabrication of non-operational device. It can result a increase of the design costs and implementation time, due to a necessity of a device redesign at post-fabrication level. In this way, the application of de-embedding scheme at the design level appears as another feature to increase the design process accuracy to facilitate the operability of the prototypes without a necessity of post-fabrication level feedback.

5 Conclusions

This work has presented the application of de-embedding scheme during the design level of a CMOS cascode AI. As expected, it was observed a significant difference between the results before and after the application of de-embedding technique in the simulations. Thus, it is shown the use of the de-embedding scheme at the design level is important to obtain accurate results and eliminate the necessity of post-fabrication feedback for IC devices. Regarding the AI itself, the obtained inductance values and Q justifies that it replaces the passive one, with the advantage of occupying a smaller area of the chip.

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