Design of Power Efficient Digital Systems Using Adiabatic Techniques

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Abstract— This paper presents the design style and analysis of ultra-low power adiabatic 4-bit, 8-bit adder-subtractors and also 3-bit, 5-bit BEC (binary to excess-1 converter) based on ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) logic families which works with the professional four phase power clock. These styles have the profit of energy saving as it reuse the certain amount of the energy by recycling from the load capacitance thus reduces the energy dissipation. MOS level-11 Tanner-spice simulation has been used for the design of Energy saving adiabatic circuits with consideration to particular frequencies with the different load capacitance, and different supply voltages. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compare with conventional CMOS logic for Incrementors and adders. Also comparison of ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) is done. In the analysis it has found that adiabatic is superior for low power applications in Cryptographic hardware for example smart cards, Digital Signal processing system and embedded systems at particular frequency choice.

Keywords- *Adiabatic Techniques, BEC (binary to excess-1 converter), Adder-Subtractor, Positive Feedback Adiabatic Logic (PFAL), Efficient Charge Recovery Logic (ECRL), Power Clock, Low Power System.*

I. Introduction

Adiabatic logic is a new research area and unique low power style. Adiabatic or quasi-adiabatic logics are also called as the energy recovery techniques. Adiabatic logic uses power clock which is used as both power as well as clock for the transistors in the design instead of V_{dd}. This power clock is mainly used for the reuse of energy stored at loads. This adiabatic logic first charges the circuits during the hold phases and then discharges the circuit to recover the supplied charge. [5]

The needs of low power in today's market are towering. However, up to date trends towards ultra-low power has prepared VLSI designers for the search of techniques to recover/reprocess from circuits. The energy recovery techniques are now and then called as adiabatic or quasi-adiabatic computing. The "Adiabatic" is a word of Greek basis that designates thermodynamics. It states to a structure in which a switch occurs without energy being either gone to or gained from the structure. And in progress year many adiabatic many adiabatic logic families have been proposed for the low power systems. [5]

In this investigation, we have design, simulated and analysed the 4-bit, 8-bit adder-subtractors and also 3-bit, 5-bit BEC **(**binary to excess-1 converter**)** using adiabatic logic families namely ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) logic and compared its power utilization with CMOS 4-bit, 8-bit adder-subtractors and also with 3-bit, 5-bit BEC **(**binary to excess-1 converter**)** respectively, ECRL 4-bit, 8-bit adder-subtractors and also 3-bit, 5-bit BEC **(**binary to excess-1 converter**)**, is compared with power utilization of PFAL 4-bit, 8-bit adder-subtractors and also with 3-bit, 5-bit BEC **(**binary to excess-1 converter**)** respectively, and also analysis is done with the wide range of load capacitance and supply voltage.

This paper has five parts. II part describes the adiabatic logic families namely Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL) while III, IV & V consists of proposed design, analysis and conclusion respectively. Here analysis is done at frequency of 50 KHz. The proposed designs are analyzed at different load capacitance at the constant frequency of 50 KHz and constant supply voltage of 2.5V and also the proposed designs are analyzed at different supply voltage at the constant frequency of 50 KHz and constant load capacitance of 200ff.

A. *Design of adiabatic circuits*

In CMOS circuits the amount of energy drawn from power supply ($c_L v_{dd}^2$) is reduced to ($1/2\ c_L v_{dd}^2$) half at the end of the charging process. In discharging process the remaining energy is dissipated, at the completion of cycle the total energy is converted to heat. The amount of energy dissipated in CMOS circuits can be reduced by using a special technique called the adiabatic logics.

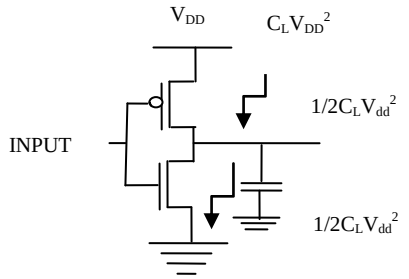

Fig-1: Basic switching analysis in CMOS

Adiabatic circuits designed with two basic rules that rapidly reduces the dissipated power and utilizes the minimal of power requirements to operate the circuit. The rules (i) never turn on a transistor when there is a voltage potential between the source and drain (ii) never turn off a transistor when current is flowing through it. In order to eliminate the wastage of power the circuit uses a power clock instead of a regular DC voltage source. This power clock will provide the active power for the operating circuit and acts as a clock to enable the output. [4]

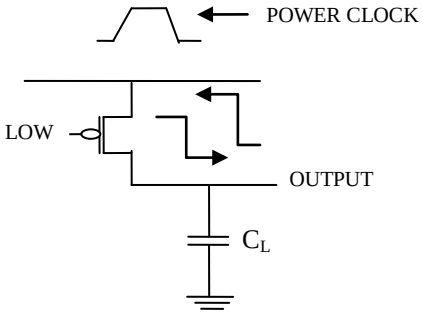

Fig-2: Fundamental charging path and Recovery path in adiabatic sentence gates

B. Power Clock Generation

The generation of power supply/clock for adiabatic techniques is most crucial part in driving the circuit. It can generate using a two block conversion circuit as shown in Fig-3. A DC power supply which acts as a constant voltage source in initial block that drives the next block to generate alternating current/clock waveform which is controlled by external control signals that are used to maintain constant frequency. More than one phase of supply is required such that logic blocks are cascaded in the circuit. The dissipated energy is refilled by the initial block DC power supply by restoring the maximum voltage of the second block to V_{dd} *range* in each cycle. However, there may be some hitch in some existing styles since number of logics charging and discharging alters from period to period during execution process which eliminates the stable load condition. The initial block DC power supply stabilizes the inequality in voltage and frequency of next block AC power supply. [2]

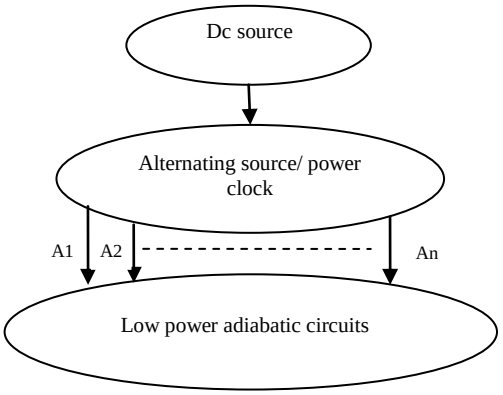

Fig-3: power supply technique for Adiabatic circuits

In the design proposed in this paper, a four phased power clock is used. The phases are (i) ideal, (ii) evaluation, (iii) hold, and (iv) recovery phase. When the clock is at ideal phase, the circuit accepts no inputs. During evaluation phase, the input provided can either is at minimal voltage resembling logic '0' or at maximum voltage resembling logic '1' will be evaluated. At the hold phase, the output of the logic will be enabled and held with respect to the power clock. In recovery phase, the power stored in the load capacitance will be discharged to ground. The power clock operation is given in the Fig-4.

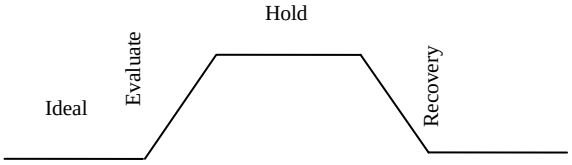

Fig-4: Power clock phases

II. Methodologies of Proposed Designs

There are many adiabatic logic families in the literature we have chosen two adiabatic logic families for our proposed design they are ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) to implement because of its good improvement in the energy dissipation reduction and often used as a reference for new logic families for evaluating power dissipation.

A. Efficient Charge Recovery Logic (ECRL)

In ECRL two PMOS's are Cross-coupled to hold the state. Power-clock is fed to Source nodes of both PMOS's and gates of each transistor are attached to the drain of the other transistor. These nodes form the complementary outputs. Set of NMOS switches are used to implement the logic function. This logic family considers four phase clock. Here the pre-charge and the evaluation will be performed in the same time. It removes the pre-charge diode and dissipates less energy than other adiabatic circuits. [4]

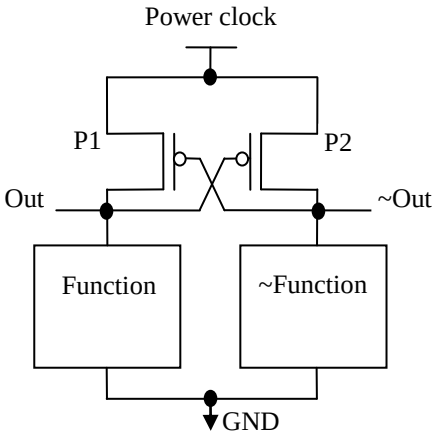

Fig-5: Block Diagram of ECRL

B. Positive Feedback Adiabatic Logic (PFAL)

In PFAL latches are made by two cross coupled inverters and the logic is implemented with the help of set of NMOS transistors. This methodology also has complementary outputs and here logic function is in parallel with the PMOS's so that channel resistance and wire resistance will be small when loads need to be charged. The logic function made of NMOS switch devices is connected between power-clock and the outputs instead of ground and the outputs. During the recovery phase, the NMOS devices between the outputs and the power-clock can provides complete recovery of required outputs. Hence the low-power performance of PFAL can be improved by making it fully reversible. Fig-6 shows the logical structure of PFAL. [5][9]

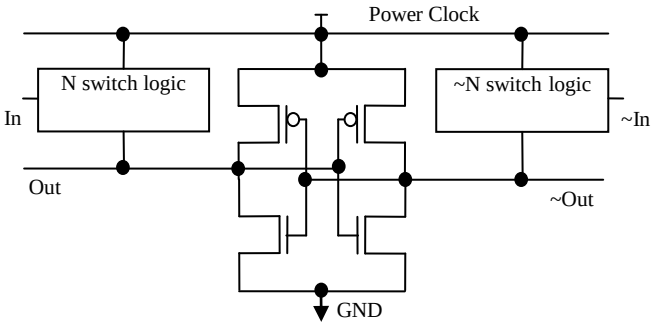

Fig-6: Block Diagram of PFAL

III. Proposed Designs

Adder-subtractors and BEC (binary to excess-1 converter*)* are the primary designs in the microprocessors and Digital Signal Processors and also adders are used in the components like dividers, subtractors, multipliers, and dividers address calculations etc., adders determines the overall performance of system. BEC (binary to excess-1 converter*)* is also known as ones incrementors. The goal of this paper is to design adiabatic BECs (binary to excess-1 converters) and Adder-subtractors based on ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) logic families. A general adder-subtractor circuit is a circuit which acts as both adder circuit and subtractor circuit. N-bit adder-subtractor consists of N-bit ripple carry adder which contains N number of full adders and N xor gates connected to each full-adder. It contains the control line with the help of these control line addition and subtraction operations are controlled, when the control line (M) is 0 adder-subtractor circuit act as adder circuit and when the control line (M) is 1 adder-subtractor circuit act as subtractor circuit. Here each xor gate has two inputs, for all N xor gates one input is control line (M) and other is one of bits of B input. When control line (M) is 0, we have B XOR 0 = B, then full adder gets value of B, the input carry is 0,and the circuit performs A PLUS B operation. When control line (M) is 1, we have B XOR 1 = inversion of B, and input carry is 1 then all the bits of B input is inverted and carry input 1 is added. The circuit performs A-B operation (A+2's complement).

Incrementor circuit is a circuit which increases the value of input by 1(one). The main adiabatic design challenge is to reduce power consumption associated with the static CMOS circuitry.

A. 3-Bit BEC (Binary To Excess -1 Converter) Using Efficient Charge Recovery Logic (ECRL)

The design of Efficient Charge Recovery Logic BEC is made in T-Spice at transistor level uses the model 1102e, where e stands for the electrical model. The block diagram and simulated waveform of ECRL binary to excess-1 converter circuit is shown in Fig-7 and Fig-8 respectively. ECRL family operates at low power, with the computations are more dependent on parameters. This makes the circuit beneficial in terms of utilizing/recovering energy at load capacitance. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. BEC is used to Increment the binary words by one, the design in this paper is three and five bit binary to excess -1 converter. Here we have input and its inverted input signals (I_2, I_1, I_0 and$\sim I_2$, $\sim I_1$, $\sim I_0$) and same way output and its inverted output signal (R_2, R_1, R_0 and$\sim R_0$, $\sim R_1$, $\sim R_2$) as the general structure of ECRL has differential input and output signal. Simulated waveform shown in Fig-8 shows only one kind of outputs (R_2, R_1, and R_0). Two power clocks are used in this circuit as shown in simulated waveforms. The number of power clocks depends on number of output used as input for other component. Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay (R_2 at 10μs). Its overturned outputs and inputs ($\sim R_2$, $\sim R_1$, $\sim R_0$ and $\sim I_2$, $\sim I_1$, $\sim I_0$) are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of ECRL BEC is low compared to CMOS binary to excess -1 converter.

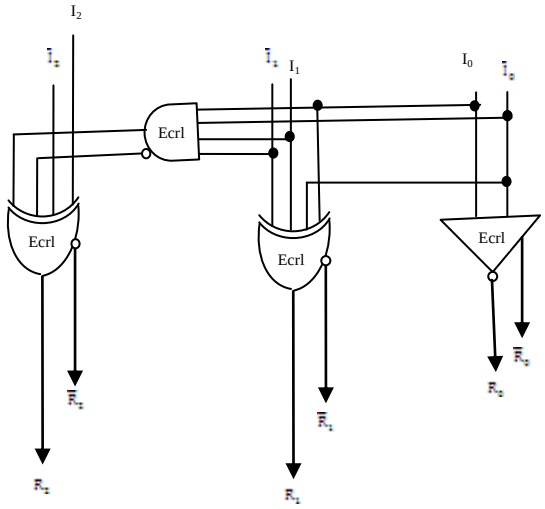

Fig-7: Logic diagram of 3-bit ECRL BEC (Binary to Excess-1 converter)

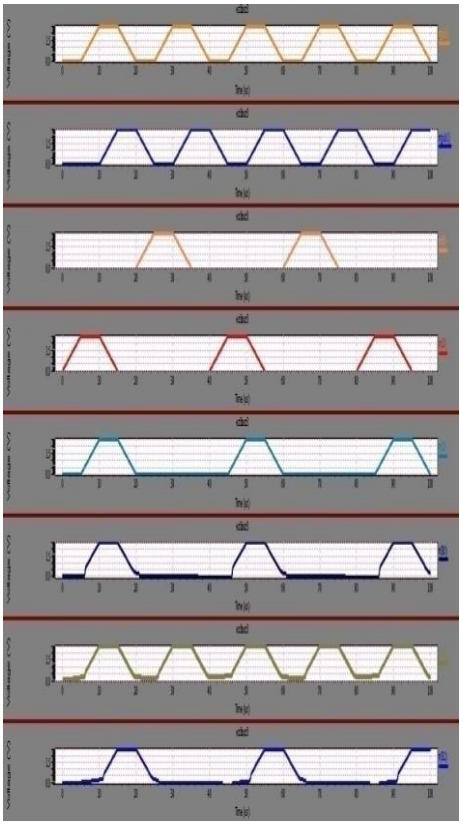

Fig-8: Simulated Waveform of 3-bit ECRL BEC Circuit for in

B. 3-Bit BEC (Binary To Excess-1 Converter) Using Positive Feedback Adiabatic Logic (PFAL)

The positive feedback adiabatic logic (PFAL), which uses two cross coupled inverters that are powered by four phase clock. This design also utilizes model 1102e of transistors for simulation. The PFAL BEC uses more transistors than ECRL design. The simulated waveform and block diagram of PFAL Binary to Excess-1 Converter circuit is shown in Fig-9 and Fig-10 respectively. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. Here we have input and its inverted input signals (I_2, I_1, I_0 and~I_2, ~I_1, ~I_0) and same way output and its inverted output signal (R_2, R_1, R_0 and ~R_0, ~R_1, ~R_2) as the general structure of PFAL has differential input and output signal. The simulated waveform shown in Figure-10 shows only one kind of outputs (R_2, R_1, and R_0). Two power clocks are used in this circuit as shown in simulated waveforms. The number of power clocks depends on number of output used as input for other component. Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay (R_2 at 10µs). Its overturned outputs and inputs (~R_2, ~R_1, ~R_0 and ~I_2, ~I_1, ~I_0) are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of PFAL BEC is low compared to CMOS binary to excess-1 converter.

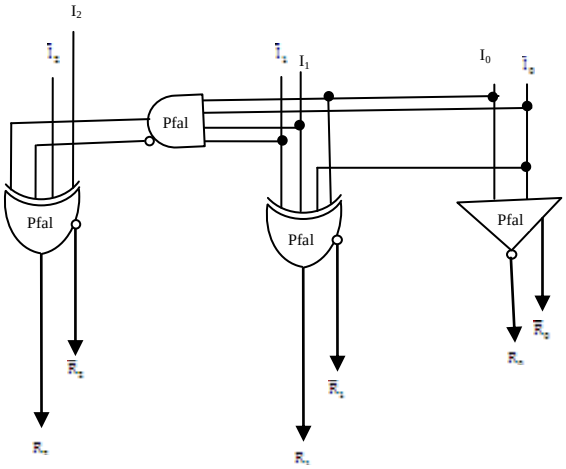

Fig-9: Logic diagram of 3-bit PFAL BEC (Binary to Excess-1 converter)

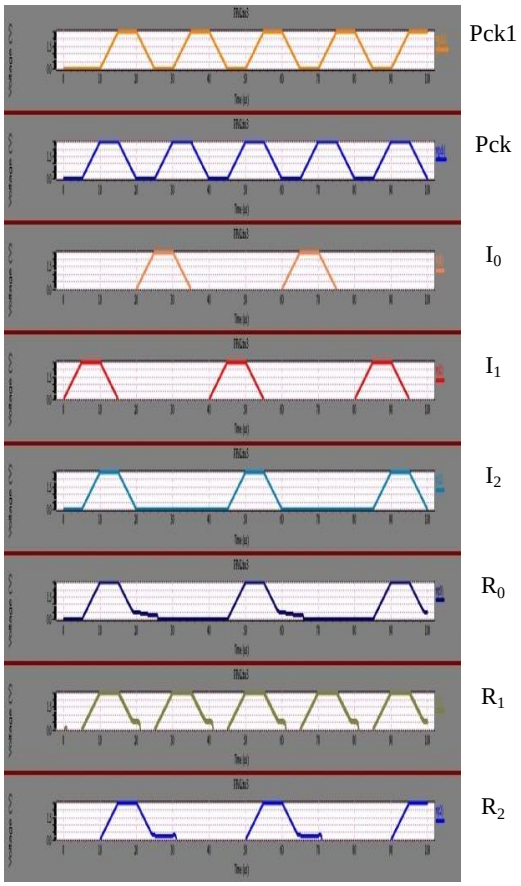

Fig-10: Simulated Waveform of 3-bit PFAL BEC Circuit for input 110

C. 5-Bit BEC (Binary To Excess-1 Converter) Using Efficient Charge Recovery Logic (ECRL)

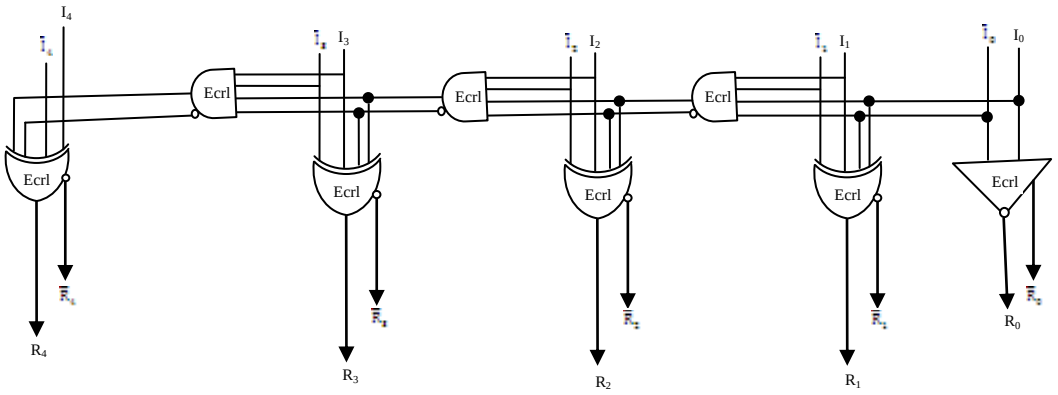

Fig-11: Logic diagram of 5-bit ECRL BEC (Binary to Excess-1 converter)

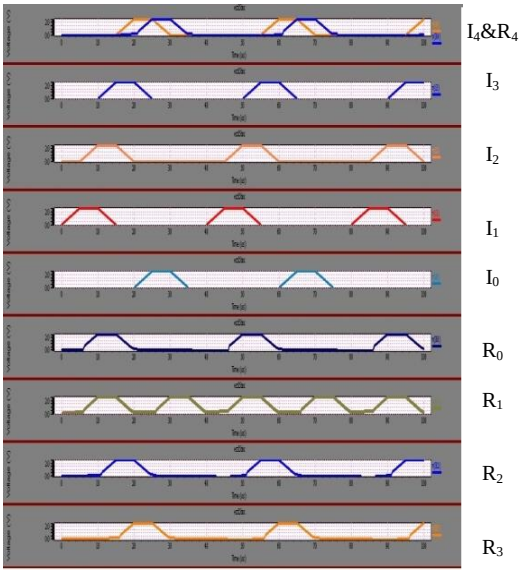

Fig-12: Simulated Waveform of 5-bit ECRL BEC Circuit for input 11110

The design of Efficient Charge Recovery Logic BEC is made in T-Spice at transistor level uses the model 1102e, where e stands for the electrical model. The block diagram and simulated waveform of ECRL binary to excess-1 converter circuit is shown in Fig-11 and Fig.12 respectively. ECRL family operates at low power, with the computations are more dependent on parameters. This makes the circuit beneficial in terms of utilizing/recovering energy at load capacitance. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. Here we used four power clocks. Outputs held according to power clocks. (R_0 at 5µs, R_1 at 5µs, R_2 at 10µs, R_3 at 15µs and R_4 at 20µs). Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay (R_4 at 20µs). BEC is used to Increment the binary words by one, the design in this paper is three and five bit binary to excess -1 converter. Here we have input and its inverted input signals (I_4,I_3,I_2,I_1,I_0 and ~I_4,~I_3, ~I_2, ~I_1, ~I_0) and same way output and its inverted output signal (R_4, R_3,R_2,R_1 R_0 and ~R_4 ~R_3, ~R_2, ~R_1 ,~R_0) as the general structure of ECRL has differential input and output signal. The simulated waveform shown in Fig-12 shows only one kind of outputs (R_4, R_3, R_2, R_1, and R0). Its overturned outputs and inputs (~R_4~R_3, ~R_2, ~R_1, ~R_0 and ~I_4, ~I_3, ~I_2, ~I_1, ~I_0) are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of ECRL BEC is low compared to CMOS binary to excess -1 converter.

D. 5-Bit BEC (Binary To Excess-1 Converter) Using Positive Feedback Adiabatic Logic (PFAL)

The positive feedback adiabatic logic (PFAL), which uses two cross coupled inverters that are powered by four phase clock. This design also utilizes model 1102e of transistors for simulation. The PFAL BEC uses more transistors than ECRL design. The simulated waveform and block diagram of PFAL Binary to Excess -1 Converter circuit is shown in Fig-13 and Fig-14 respectively. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. Here we used four power clocks. Outputs held according to power clocks. (R_0 at 5µs, R_1 at 5µs, R_2 at 10µs, R_3 at 15µs and R_4 at 20µs). Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay (R_4 at 20µs). Here we have input and its inverted input signals (I_4,I_3,I_2,I_1,I_0 and ~I_4,~I_3,~I_2,~I_1, ~I_0) and same way output and its inverted output signal (R_4, R_3,R_2,R_1 R_0 and ~R_4,~R_3,~R_2,~R_1 ,~R_0) as the general structure of PFAL has differential input and output signal. The simulated waveform shown in Fig-14 shows only one kind of outputs (R_4, R_3, R_2, R_1, and R_0).

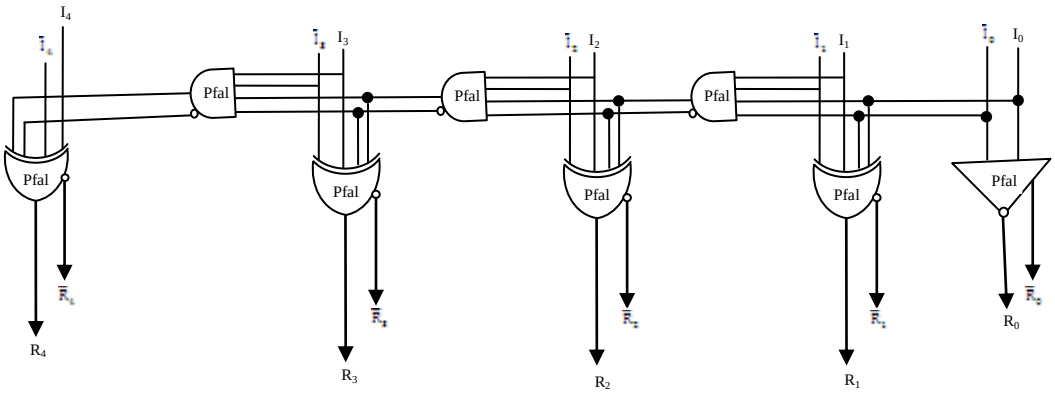

Fig- 13: Logic diagram of 5-bit PFAL BEC (Binary to Excess-1 converter)

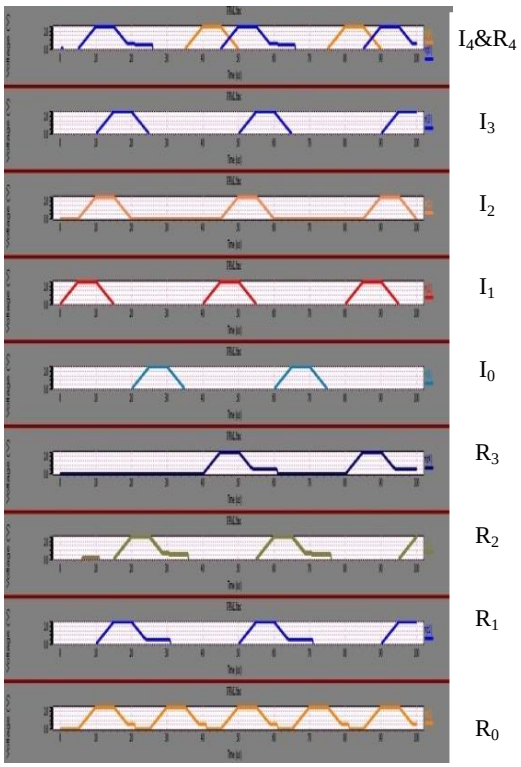

Fig- 14: Simulated Waveform of 5-bit PFAL BEC Circuit for input 01110

E. ECRL 4-Bit Adder-Subtractor

The design of 4-bit ECRL Adder-Subtractor is made in T-Spice at transistor level uses the model 1102e, where e stands for the electrical model. The block diagram and simulated waveform of 4-bit ECRL Adder-Subtractor circuit is shown in Fig-15 and Fig.16. ECRL family operates at low power, with the computations are more dependent on parameters. This makes the circuit beneficial in terms of utilizing/recovering energy at load capacitance. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. Adder-Subtractor is used for addition and also for subtraction. Operations addition and subtraction are controlled with control line which is denoted with M in below diagram, when control line M is one, operation is subtraction and when M is zero, operation is addition. The design in this paper is four and eight bit Adder-Subtractor. Here we have input and its inverted input signals and same way output and its inverted output signal as the general structure of ECRL has differential input and output signal. The simulated waveform shown in Fig-16 shows only one kind of outputs (C_{out}, S_3, S_2, S_1, and S_0). Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay (S_0 at 10µs, S_1 at 20µs, S_2 at 30µs, S_3 at 40µs, C_{out} at 40µs). Various power clocks are used in this circuit, the number of power clocks depends on number of output used as input for other component. Designing these circuits is complex. Its inputs and inverted outputs and power clocks are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of ECRL Adder-Subtractor is low compared to CMOS Adder-Subtractor.

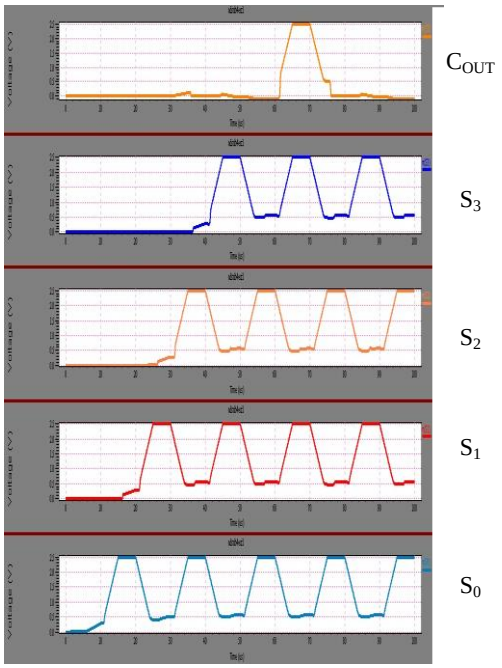

Fig-16: Simulated Waveform of 4-bit ECRL Adder-Subtractor Circuit for input A=0000, B=1111 with the control line set to 0(M=0)

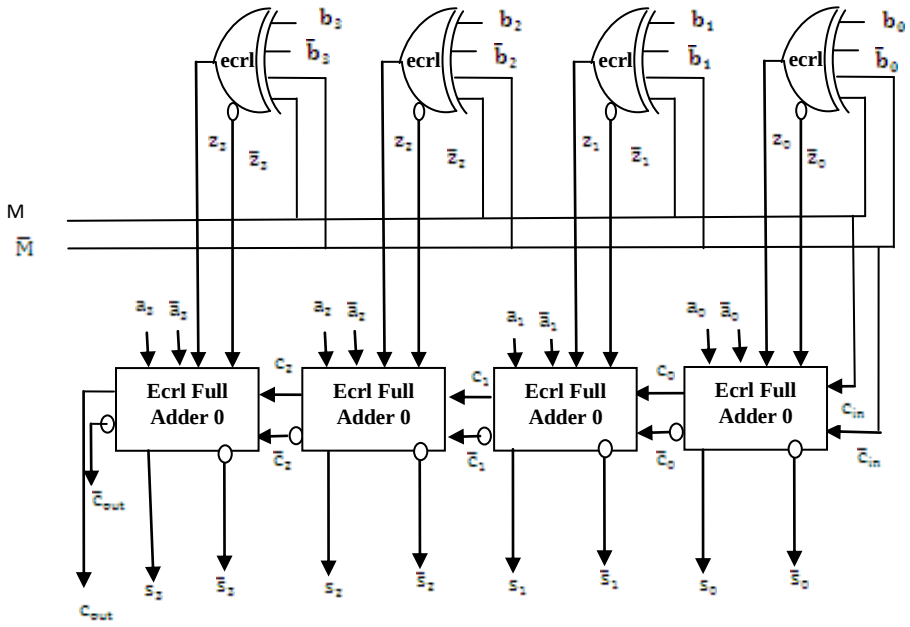

Fig-15: Block diagram of 4-bit ECRL Adder-Subtractor

F. PFAL 4-Bit Adder-Subtractor

The positive feedback adiabatic logic (PFAL), which uses two cross coupled inverters that are powered by four phase clock. This design also utilizes model 1102e of transistors for simulation. The PFAL Adder-Subtractor uses more transistors than ECRL design. The simulated waveform and block diagram of 4-bit PFAL Adder-Subtractor circuit is shown in Fig-17 and Fig.18. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay (S_0 at 10µs, S_1 at 20µs, S_2 at 30µs, S_3 at 40µs, C_{out} at 40µs). Various power clocks are used in this circuit, the number of power clocks depends on number of output used as input for other component. Adder-Subtractor is used for addition and also for subtraction. Operations addition and subtraction are controlled with control line which is denoted with M in below diagram, when control line M is one, operation is subtraction and when M is zero, operation is addition. The design in this paper is four and eight bit Adder-Subtractor. Here we have input and its inverted input signals and same way output and its inverted output signal as the general structure of PFAL has differential input and output signal. The simulated waveform shown in Fig-18 shows only one kind of outputs (C_{OUT}, S_3, S_2, S_1, and S_0). Its inputs and inverted outputs and power clocks are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of PFAL Adder-Subtractor is low compared to CMOS Adder-Subtractor.

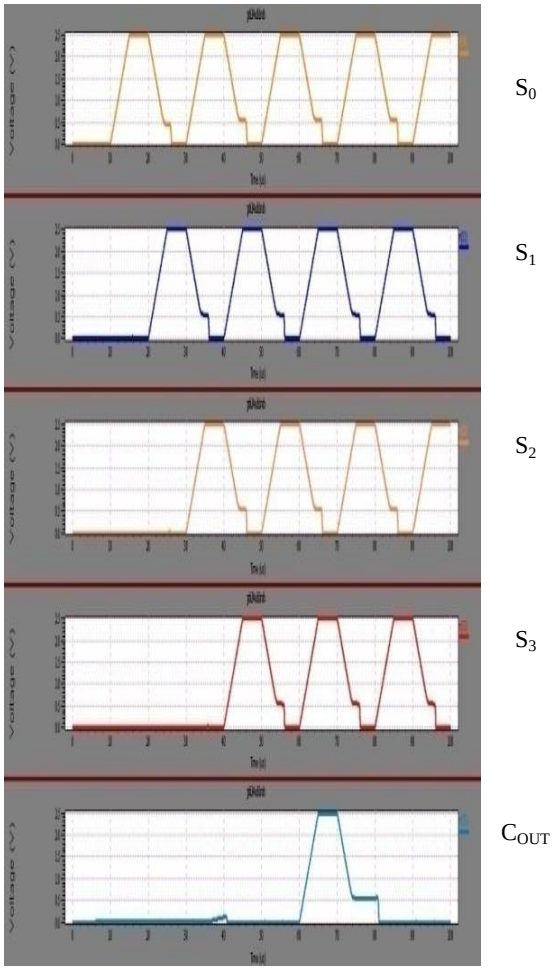

Fig-18: Simulated Waveform of 4-bit PFAL Adder-Subtractor Circuit for input A=0000, B=1111 with the control line set to 0(M=0)

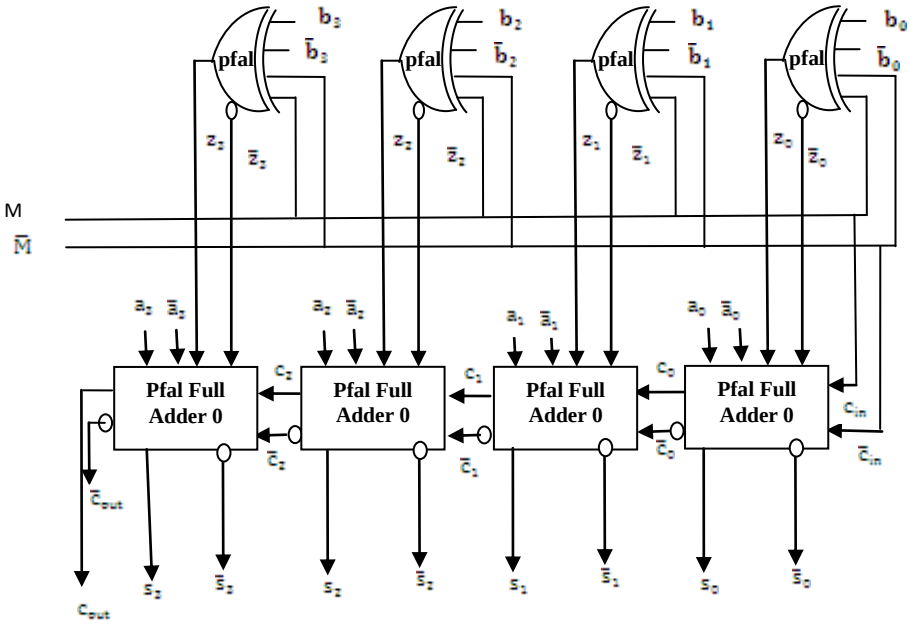

Fig-17: Block diagram of 4-bit PFAL Adder-Subtractor

G. ECRL 8-Bit Adder-Subtractor

The design of 8-bit ECRL Adder-Subtractor is made in T-Spice at transistor level uses the model 1102e, where e stands for the electrical model. The block diagram and simulated waveform of 8-bit ECRL Adder-Subtractor circuit is shown in Fig-19 and Fig-20.ECRL family operates at low power, with the computations are more dependent on parameters. This makes the circuit beneficial in terms of utilizing/recovering energy at load capacitance. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay. (S_0 at 10µs, S_1 at 20µs, S_2 at 30µs, S_3 at 40µs, S_4 at 50µs, S_5 at 60µs, S_6 at 70µs, S_7 at 80µs, C_{out} at 80µs). These delays can be reduced by modifying circuit design. Various power clocks are used in this circuit, the number of power clocks depends on number of output used as input for other component. Adder-Subtractor is used for addition and also for subtraction. Operations addition and subtraction are controlled with control line which is denoted with M in below diagram, when control line M is one, operation is subtraction and when M is zero, operation is addition. The design in this paper is four and eight bit Adder-Subtractor. Here we have input and its inverted input signals and same way output and its inverted output signal as the general structure of ECRL has differential input and output signal. The simulated waveform shown in Fig-20 shows only one kind of outputs (C_{OUT}, S_7, S_6, S_5, S_4, S_3, S_2, S_1, and S_0). Its inputs and inverted outputs and power clocks are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of ECRL Adder-Subtractor is low compared to CMOS Adder-Subtractor. Every component is provided with its own delayed power clocks in order to support their inputs that are delayed from their pervious blocks. Outputs always held according to its power clock.

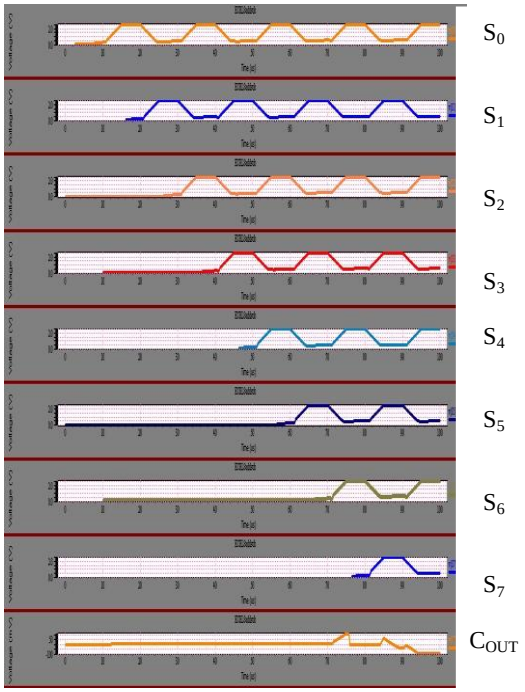

Fig- 20: Simulated Waveform of 8-bit ECRL Adder-Subtractor Circuit for input A=00000000, B=11111111 with the control line set to 0(M=0)

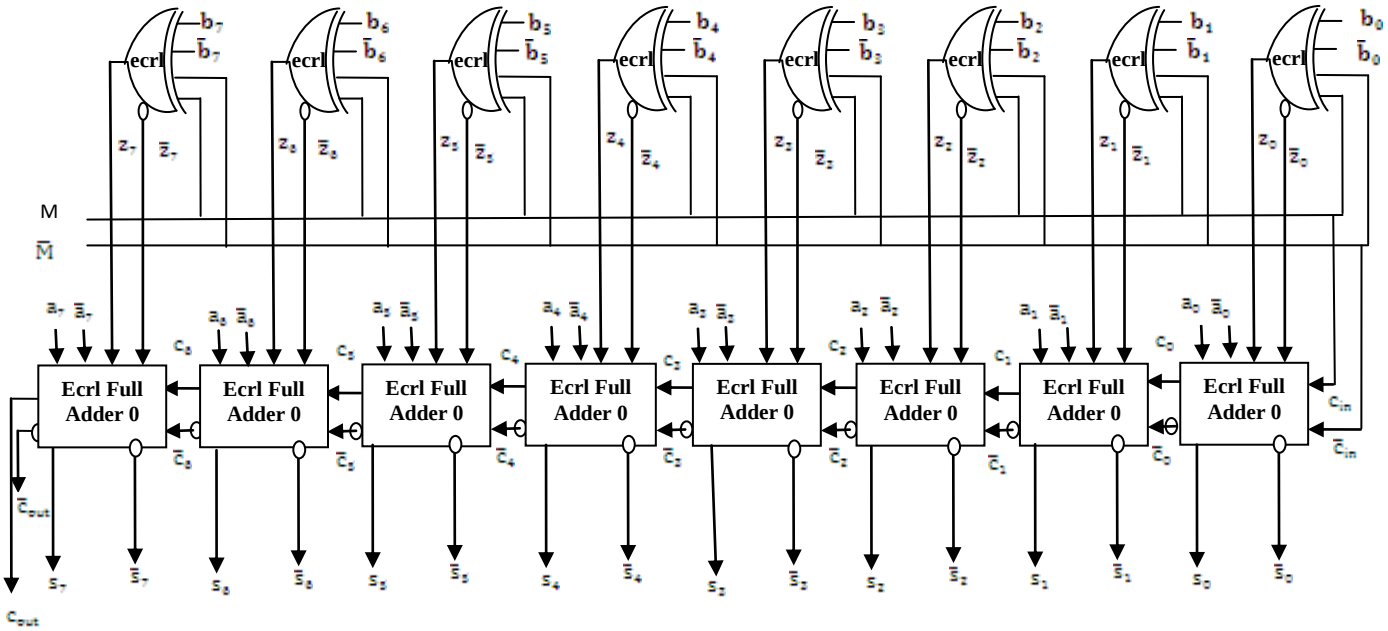

Fig-19: Block diagram of 8-bit ECRL Adder-Subtractor

H. PFAL 8-Bit Adder-Subtractor

The positive feedback adiabatic logic (PFAL), which uses two cross coupled inverters that are powered by four phase clock. This design also utilizes model 1102e of transistors for simulation. The PFAL Adder-Subtractor uses more transistors than ECRL design. The simulated waveform and block diagram of 8-bit PFAL Adder-Subtractor circuit is shown in Fig-21 and Fig-22. An adiabatic logic reduces the power dissipation at the expenses of complexity of circuit. N-bit adder-subtractor has N number of full adders and N number of xor gates. First, inputs A is given to xor gates then output of those xor gates (which is delayed) should be given to full adders and another inputs which is B must be delayed to support the out puts of xors which will act as input to full adders, as output of xor gates are delayed. So each bit of output are generated with delay. Every component provided with a constantly delayed power clock to support the feeding of inputs that are delayed from the previous blocks. So the output of the final component will be at the maximum computation delay. (S_0 at 10µs, S_1 at 20µs, S_2 at 30µs, S_3 at 40µs, S_4 at 50µs, S_5 at 60µs, S_6 at 70µs, S_7 at 80µs, C_{out} at 80µs). Outputs always held according to its power clock. These delays are because of circuit design, so we can reduce these delays by modifying circuit design.

Adder-Subtractor is used for addition and also for subtraction. Operations addition and subtraction are controlled with control line which is denoted with M in below diagram, when control line M is one, operation is subtraction and when M is zero, operation is addition. The design in this paper is four and eight bit Adder-Subtractor. Here we have input and its inverted input signals and same way output and its inverted output signal as the general structure of PFAL has differential input and output signal. The simulated waveform shown in Fig-22 shows only one kind of outputs (C_{OUT}, S_7, S_6, S_5, S_4, S_3, S_2, S_1, and S_0). Its inputs and inverted outputs and power clocks are not shown in simulated waveform. The complimentary outputs facilitate to eradicate the inverters, which might otherwise be used. The switching power dissipation of PFAL Adder-Subtractor is low compared to CMOS Adder-Subtractor.

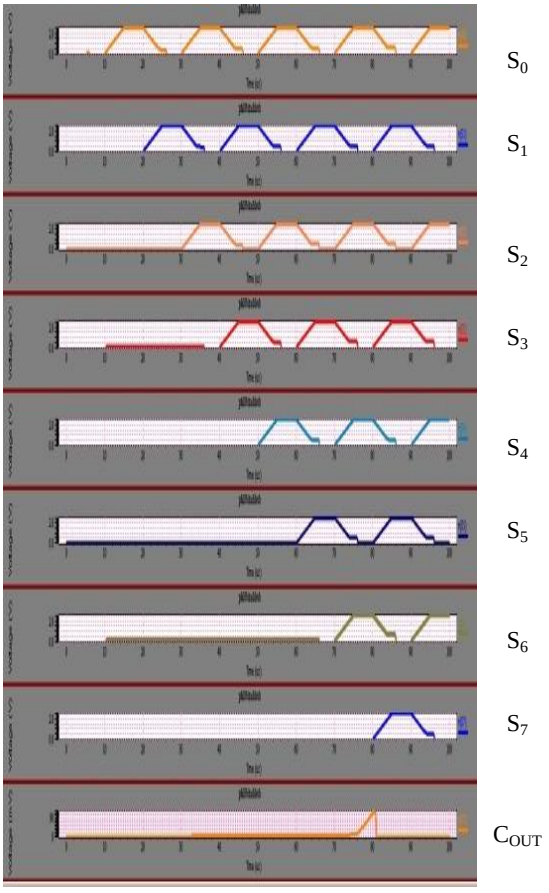

Fig-22: Simulated Waveform of 8-bit PFAL Adder-Subtractor Circuit for input A=00000000, B=11111111 with the control line set to 0 (M=0)

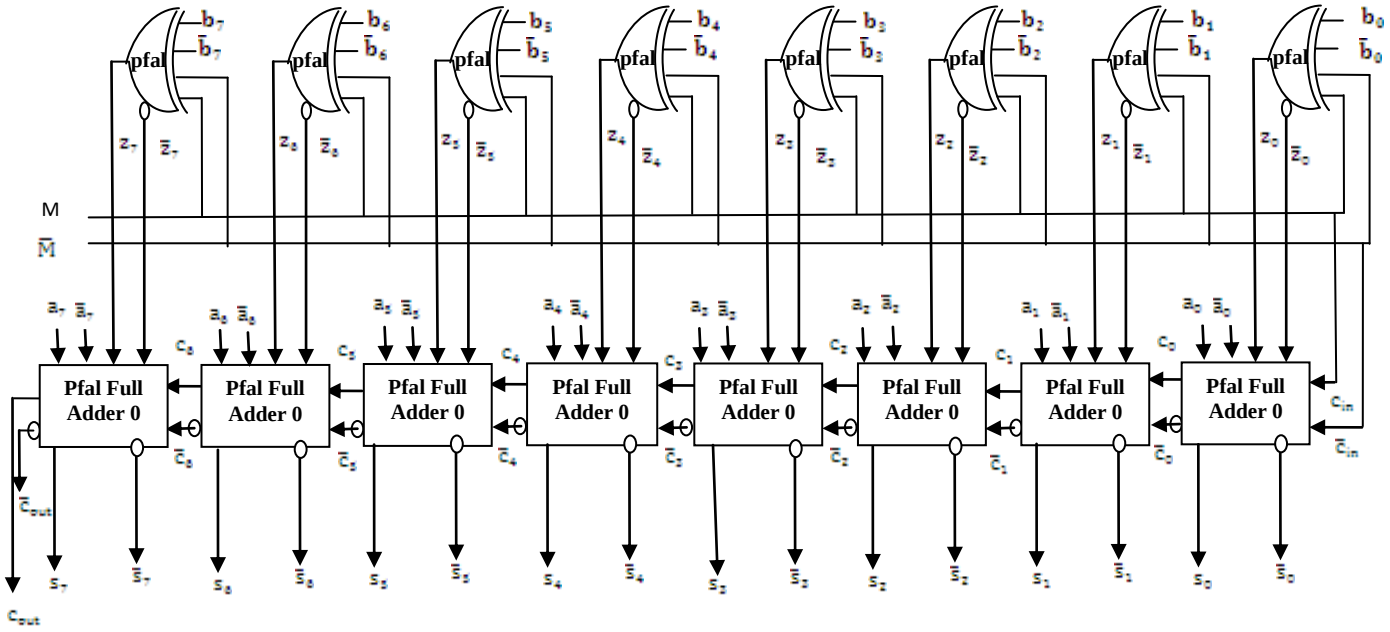

Fig-21: Block diagram of 8-bit PFAL Adder-Subtractor

IV. Study Of Energy Utilization With Varied Parameters

ECRL and PFAL adiabatic logic families are highly dependent on parameters. The study of power utilization for ECRL BECs, PFAL BECs, ECRL Adder-Subtractors and PFAL Adder-Subtractors, is done with admiration of CMOS BECs, CMOS Adder-Subtractors circuit with the help of TSPICE simulation, at MOS Level 11 simulation parameters. The following Tabulations provide vital information about the variation in power consumption to change in parameters.

TABLE.1. Power consumed versus Supply Voltage with load capacitance kept constant at CL= 200fF and Frequency at 50 KHz

3-Bit BEC Circuit Family	No. Of Transistors	Power Analysis	
		Supply Voltage (V)	Power (mW)
CMOS	28	2.5	0.00037348
		3.0	0.00061700
		3.5	0.00099074
ECRL	30	2.5	0.00003048
		3.0	0.00003822
		3.5	0.00004724
PFAL	38	2.5	0.00007918
		3.0	0.00016468
		3.5	0.00030711

TABLE. 2. Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v

3-Bit BEC CIRCUIT FAMILY	NO. Of TRANSISTORS	POWER ANALYISIS	
		Load Capacitance (fF)	Power (mW)
CMOS	28	300fF	0.000464
		400fF	0.000570
		700fF	0.000839
ECRL	30	300fF	0.000040
		400fF	0.000051
		700fF	0.000072
PFAL	38	300fF	0.000067
		400fF	0.000071
		700fF	0.000088

Computing the power factor with respect to other parameter variation shows a considerable difference in consumption. Table.1 shows Power consumed versus Supply Voltage with load capacitance kept constant at CL=200fF and Frequency at 50 KHz for 3-bit CMOS BEC, 3-bit PFAL BEC, and 3-bit ECRL BEC. Table.2 shows Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v for 3-bit CMOS BEC, 3-bit PFAL BEC, and 3-bit ECRL BEC. Table.3 shows Power consumed versus supply voltage with Frequency kept constant at 50 KHz and load capacitance CL=200fF for 5-bit CMOS BEC, 5-bit PFAL BEC, and 5-bit ECRL BEC. Table.4 shows Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v for 5-bit CMOS BEC, 5-bit PFAL BEC, and 5-bit ECRL BEC.

Table.5 shows Power consumed versus supply voltage with Frequency kept constant at 50 KHz and load capacitance CL=200fF for 4-bit CMOS Adder-Subtractor, 4-bit PFAL Adder-Subtractor, and 4-bit ECRL Adder-Subtractor. Table.6 shows Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v for 4-bit CMOS Adder-Subtractor, 4-bit PFAL Adder-Subtractor, and 4-bit ECRL Adder-Subtractor.Table.7 shows Power consumed versus supply voltage with Frequency kept constant at 50 KHz and load capacitance CL=200fF for 8-bit CMOS Adder-Subtractor, 8-bit PFAL Adder-Subtractor, and 8-bit ECRL Adder-Subtractor.Table.8 shows Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v for 8-bit CMOS Adder-Subtractor, 8-bit PFAL Adder-Subtractor, and 8-bit ECRL Adder-Subtractor.

TABLE. 3. Power consumed versus Supply Voltage with load capacitance kept constant at CL=200fF and Frequency at 50 KHz

5-Bit BEC CIRCUIT FAMILY	NO. Of TRANSISTORS	POWER ANALYISIS	
		Supply Voltage (V)	Power (mW)
CMOS	66	2.5	0.0008986
		3.0	0.0014759
		3.5	0.0022478
PFAL	78	2.5	0.0002305
		3.0	0.0003624
		3.5	0.0006106
ECRL	62	2.5	0.0000871
		3.0	0.0000112
		3.5	0.0001430

TABLE. 4. Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v

5-Bit BEC CIRCUIT FAMILY	NO. Of TRANSISTORS	POWER ANALYISIS	
		Load Capacitance (fF)	Power (mW)
CMOS	66	300fF	0.0010796
		400fF	0.0012622
		700fF	0.0018132
PFAL	78	300fF	0.0002454
		400fF	0.0002705
		700fF	0.0003478
ECRL	62	300fF	0.0001142
		400fF	0.0001405
		700fF	0.0002002

TABLE. 5. Power consumed versus Supply voltage with Frequency kept constant at 50 KHz and Load Capacitance CL= 200fF

4-Bit ADDER-SUBTRACTOR CIRCUIT FAMILY	NO. of TRANSISTORS	POWER ANALYISIS	
		Supply voltage (V)	Power (mW)
CMOS	152	2.5	0.00282
		3.0	0.00452
		3.5	0.00676
PFAL	208	2.5	0.00043
		3.0	0.00069
		3.5	0.00105
ECRL	184	2.5	0.00020
		3.0	0.00026
		3.5	0.00034

TABLE. 6. Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v

4-Bit ADDER-SUBTRACTOR CIRCUIT FAMILY	NO. of TRANSISTORS	POWER ANALYISIS	
		Load Capacitance (fF)	Power (mW)
CMOS	152	300fF	0.00328
		400fF	0.00376
		700fF	0.00514
PFAL	208	300fF	0.00045
		400fF	0.00047
		700fF	0.00055
ECRL	184	300fF	0.00023
		400fF	0.00026
		700fF	0.00034

TABLE. 7. Power consumed versus Supply Voltage with load capacitance kept constant at CL=200fF and Frequency at 50 KHz

8-Bit ADDER-SUBTRACTOR CIRCUIT FAMILY	NO. of TRANSISTORS	POWER ANALYISIS	
		Supply voltage (V)	Power (mW)
CMOS	304	2.5	0.00563
		3.0	0.00900
		3.5	0.01343
PFAL	416	2.5	0.00064
		3.0	0.00106
		3.5	0.00150
ECRL	368	2.5	0.00033
		3.0	0.00044
		3.5	0.00057

TABLE. 8. Power consumed versus Load Capacitance with Frequency kept constant at 50 KHz and Supply voltage at 2.5v

8-Bit ADDER-SUBTRACTOR CIRCUIT FAMILY	NO. of TRANSISTORS	POWER ANALYISIS	
		Load Capacitance (fF)	Power (mW)
CMOS	304	300fF	0.0065
		400fF	0.0074
		700fF	0.0101
PFAL	416	300fF	0.00067
		400fF	0.00071
		700fF	0.00087
ECRL	368	300fF	0.00036
		400fF	0.00046
		700fF	0.00059

V.Conclusion

With the design of binary to excess-1 converters, Adder-Subtractors, in two different families of adiabatic logics namely ECRL and PFAL show a considerable improvement in power consumption even with the presence of higher number of transistors. The power analysis table shows clearly that these adiabatic circuits utilize very low power compared to conventional CMOS binary to excess-1 converter, Adder-Subtractor, at frequencies ranging in 50 KHz. Change in load capacitance shows a sizable difference in power consumption. Further reduction of power can be made by acting on other parameters of the circuit and including the transistor model also. In our analysis ECRL shows good energy saving than PFAL.

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