

Implementing Complex Wavelet Transform in Analog Circuit and Singular Value Decomposition Algorithm

MU LI¹, YIGANG HE², XIAOFENG WU¹, ZAIFANG XI¹

¹College of Information & Electrical Engineering of Hunan University of Science and Technology

²School of Electrical & Automation Engineering of Hefei University of Technology

Xiangtan, Hunan

China

limuucn@163.com

Abstract: - A new method for implementing complex wavelet transform (CWT) based on analog sampled-data circuit and singular value decomposition (SVD) algorithm is presented. To begin with, the real and imaginary parts functions of the complex wavelet base are approximated by using SVD algorithm. As the main advantage of this approximation approach is its computational simplicity and general applicability. Next, the complex wavelet circuit is implemented using multiple-loop feedback (MLF) architecture with switched-current (SI) bilinear integrators and current mirrors as basic elements. Finally, the CWT is realized by controlling the clock frequency of the designed SI filters. Simulation results demonstrate the proposed method of implementing the CWT is effective and would be suitable to design other SI circuits as well.

Key-Words: -Complex wavelet, wavelet transform, analog filters, switched-current circuits, singular value decomposition.

1 Introduction

For local analysis of nonstationary and fast transient signals, the wavelet transform (WT) has been shown to be a very promising mathematical tool, due to its good estimation of time and frequency localizations [1-3]. Conventionally, wavelet transform has been implemented using software and digital hardware technique. However, it is not suitable to the low power applications such as biomedical implantable devices, due to the high power consumption associated with the required analog-digital converter. Therefore analog WT are still widely used in practices.

Recently, there have been significant advances in the analog implementations of the WT and its practical application. In [4-6], the authors have been proposed an implementation method of the WT using continuous time log-domain circuit with bipolar transistors for ECG signal analysis. In [7-9], the gm-C circuit with MOS transistors is used to implement the WT. However, these approaches need either huge capacitors or bias currents of few pA to tens of nA, which are difficult to generate precisely. The analog sampled-data switched-capacitor (SC) circuit is applied to

implement the WT in [10]. The main advantage of sampled-data circuit for WT implementation is that the dilations of the circuit can be easily and precisely controlled by changing the clock frequency. However, the SC circuits are not fully compatible with current trends in digital CMOS process and their performance suffers as supply voltages are scaled down. Therefore, the sampled-data switched-current (SI) circuit for the implementation of WT system has aroused the scholars' research interest. The WT implementation based on cascade structure SI filter and Padé approximation is presented in [11]. However, the design SI filter with cascade structure has high sensitivity. In additional, Padé approximation has some disadvantages such as the stability of the transfer function, and the choice of the degrees for the numerator and denominator polynomials in the rational approximation function, which limit the practical applicability of this method. A modified analog WT realization method base on parallel structure SI filter and L_2 approximation is proposed in [12]. But the parallel structure SI filter still has high sensitivity. Moreover, L_2 approximation is a local optimization algorithm, a drawback of this approach is that a good

starting point is required for finding an optimal approximation. In order to solve this problem of L_2 method, the authors used differential evolution algorithm [13,14] or PSO-SQP method [15] to approximated wavelet base. However, it is different to set the parameters of those intelligence algorithms and they need long iteration time. Furthermore, the SI filter still is cascade or parallel structure, which these structures have high sensitivity, in particular as filter order increases.

In overall above literatures, the major researches are aimed to the real WT implementation. However, complex wavelet transform (CWT) has some significant advantages over real wavelet transform for certain signal processing problems. CWT is a form of the WT, which generates complex coefficients by using two wavelet filters to obtain their real and imaginary parts. What makes the complex wavelet basis exceptionally useful for denoising purposes is that it provides a high degree of shift-invariance and better directionality compared to the real WT. Therefore, it is very important to implement the CWT using analog circuit for the practical application of the WT.

A new method of the CWT implementation is presented using analog sampled-data SI circuit and singular value decomposition (SVD) algorithm in this work. Firstly, the selective complex wavelet base is approximated by using SVD algorithm. Next, the multiple-loop feedback (MLF) CWT filter whose impulse response is the approximated wavelet function is designed using SI bilinear integrators and current mirrors as basis building blocks. Finally, the CWT is realized by controlling the clock frequency of the circuits with the same structure. Simulation results of the proposed method show the effectivity of analog CWT implementation.

2 The CWT in Analog Circuit

The CWT of a function $x(t)$ at the scale a and position τ is given by

$$\begin{aligned} W_x(a, \tau) &= \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} x(t) \tilde{\psi}\left(\frac{t-\tau}{a}\right) dt = x(t) * \frac{1}{\sqrt{a}} \psi\left(\frac{-t}{a}\right) \\ &= x(t) * \left[\frac{1}{\sqrt{a}} \psi^r\left(\frac{-t}{a}\right) - j \frac{1}{\sqrt{a}} \psi^i\left(\frac{-t}{a}\right) \right] \\ &= W_x^r(a, \tau) + j W_x^i(a, \tau) \end{aligned} \quad (1)$$

where $\psi(t)$ is the complex wavelet base and $\psi(t) = \psi^r(t) + j\psi^i(t)$, $\tilde{\psi}(t)$ denotes the complex conjugation and $*$ denotes convolution. The factor $1/\sqrt{a}$ is used for energy normalization.

When a signal $x(t)$ is passed through a linear time-invariant (LTI) filter, the filter output is well known to be the convolution of $x(t)$ with the impulse response $h(t)$ of the filter, which is described as:

$$f(t) * h(t) = \int_{-\infty}^{+\infty} f(\tau) h(t-\tau) d\tau \quad (2)$$

From (1) and (2) it is immediate that analog computation of the CWT $W_x(a, \tau)$ at a selected scale a , can be achievable through implementation of the linear filters, which the impulse responses need to satisfy:

$$h_a^r(t) = \frac{1}{\sqrt{a}} \psi^r\left(\frac{-t}{a}\right) \quad (3)$$

$$h_a^i(t) = -\frac{1}{\sqrt{a}} \psi^i\left(\frac{-t}{a}\right) \quad (4)$$

Fig.1 shows an analog CWT system with multiple scales in parallel that can be used to compute the CWT in real time.

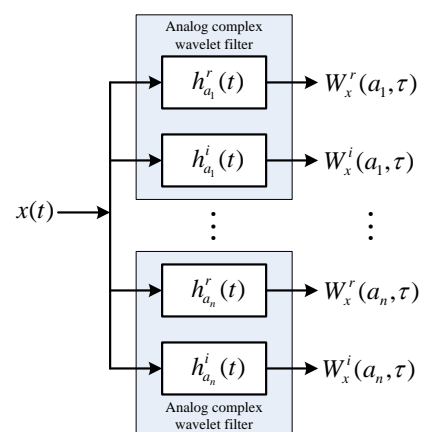


Fig.1 Analog complex wavelet transform system

3 Complex Wavelet Approximation

For obvious physical reasons only the hardware implementation of causal stable filters is feasible. In

other words, a realizable linear filter will have a proper rational transfer function $H(s)$ that has all its poles in the complex left half plane. We find that any mother wavelet $\psi(t)$ which does not have this property must be time-shifted $\psi(t-t_0)$ to facilitate an accurate approximation of its WT.

In this works, the complex Gabor wavelet is selected as an example. The singular value decomposition (SVD) algorithm will be employed to approximation this wavelet. The complex Gabor wavelet is defined by

$$\psi(t) = \psi^r(t) + j\psi^i(t) = \cos(2t)e^{-t^2} - j\sin(2t)e^{-t^2} \quad (5)$$

In order to obtain the realizable wavelet filters, $h^r(t)$ in (3) and $h^i(t)$ in (4) are used to approximate the real part $\psi^r(t-t_0)$ and imaginary part $\psi^i(t-t_0)$ of the time-shifted complex wavelet $\psi(t-t_0)$, respectively.

We first consider the discrete time state space model as the following:

$$\begin{cases} x(k+1) = Ax(k) + Bu(k) \\ y(k) = Cx(k) + Du(k) \end{cases} \quad (6)$$

where $u(k)$ and $y(k)$ are the input and output of the system, respectively. $x(k)$ and $x(k+1)$ are the present and advanced states of the system, respectively. A, B, C and D are the state, input, output, and direct matrices of the state space description, respectively. The direct feedthrough matrix D is set to zero to achieve strict causality. The impulse response of a state space system can be described as [16]:

$$h = [\dots 0 \ 0 \ 0 \ D \ CB \ CAB \ CA^2B \ \dots] \quad (7)$$

Now, we may put h into the form of a Hankel (H) matrix, such that:

$$H = \begin{bmatrix} CB & CAB & CA^2B & \dots \\ CAB & CA^2B & & \\ CA^2B & & \ddots & \\ \dots & & & \end{bmatrix} \quad (8)$$

From (8) we can see that the columns of H are shifted versions of the impulse response and the H matrix is a result of a multiplication of the observability matrix O and the controllability matrix K.

$$H = O \cdot K \quad (9)$$

The matrices O and K are respectively defined by:

$$O = [C \ AC \ A^2C \ \dots]^T \quad (10)$$

$$K = [B \ AB \ A^2B \ \dots] \quad (11)$$

In order to extract the A, B, C and D matrixes from H, the SVD on the Hankel matrix is employed to compute the O and K matrixes. The SVD on the Hankel matrix is described as:

$$H = U \cdot \Sigma \cdot V^T \quad (12)$$

where matrix Σ is a diagonal matrix with the singular values arranged in decreasing order. The O and K matrix can be calculated from the SVD respectively as:

$$O = \tilde{U} \cdot \tilde{\Sigma}^{1/2} \quad (13)$$

$$K = \tilde{\Sigma}^{1/2} \cdot \tilde{V}^T \quad (14)$$

where \tilde{U} , $\tilde{\Sigma}$ and \tilde{V} are the approximation of the original U, Σ and V matrixes, respectively. Next, we need to extract the A matrix of the state space description by dividing the O in two separate parts and again dividing them to extract the A matrix. Here, we choose the O matrix as [17]:

$$O = \begin{bmatrix} \overbrace{C \ CA \ CA^2 \ \dots \ CA^{n-1}}^{O_x} & CA^n \end{bmatrix}^T \quad (15)$$

$$O = \begin{bmatrix} C & \overbrace{CA \ CA^2 \ \dots \ CA^{n-1}}^{O_y} & CA^n \end{bmatrix}^T \quad (16)$$

We can see that $O_x \cdot A = O_y$, so $A = O_x^+ \cdot O_y$. Where O_x^+ is the pseudo-inverse of O_x . The B and C matrixes can be obtained from the first row and first column of the O and K matrixes, respectively. In this paper, we will use this method for obtaining the approximation function of the real and imaginary parts of the complex Gabor wavelet. We choose the approximation order is 7 and time-shifted is 2.5. The approximated real and imaginary parts are shown in Fig.2 and Fig.3, respectively.

The approximation mean-square errors (MSE) of the real and imaginary parts of complex Gabor wavelet are 3.2093×10^{-5} and 6.879×10^{-5} , respectively. The SVD method has been proven to be successful in the time domain for approximating complex wavelet. The 7th order transfer functions ($a=1$) of complex Gabor

wavelet for the real and imaginary parts are given as follows:

$$h_1^r(s) = (7.335s^6 - 1.611e2s^5 + 1.879e3s^4 - 1.384e4s^3 + 6.437e4s^2 - 1.979e5s + 1.948e5)/(s^7 + 6.392s^6 + 49.22s^5 + 1.807e2s^4 + 5.848e2s^3 + 1.131e3s^2 - 1.514e3s + 979.2) \quad (17)$$

$$h_1^i(s) = (-11.89s^6 + 2.007e2s^5 - 2.034e3s^4 + 1.139e4s^3 - 4.364e4s^2 + 7.413e4s - 1676)/(s^7 + 5.071s^6 + 39.69s^5 + 1.197e2s^4 + 3.778e2s^3 + 5.916e2s^2 + 7.401s + 327.6) \quad (18)$$

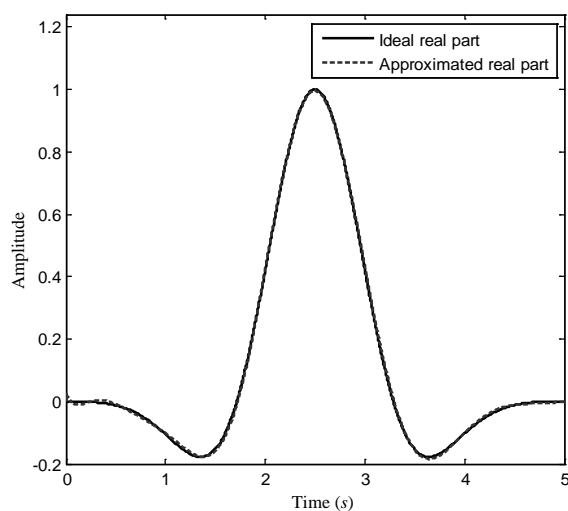


Fig.2 Real part approximation of Complex Gabor wavelet

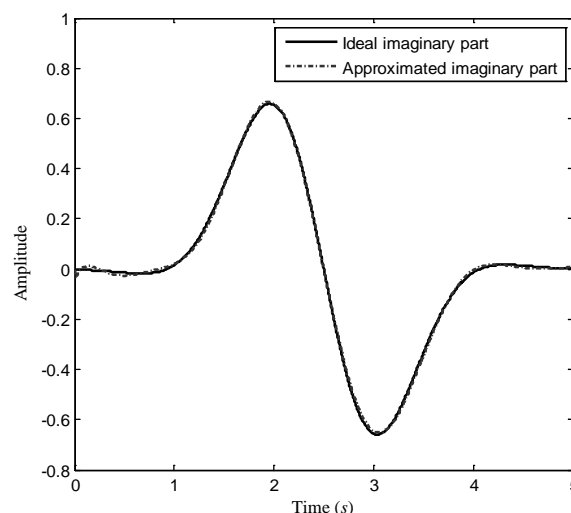


Fig.3 Imaginary part approximation of Complex Gabor wavelet

In the next section, we will design the SI filters whose impulse responses are the approximated real and imaginary parts of complex wavelet and their dilations.

4 Complex Wavelet Circuit Design

The complex wavelet circuit performance not only depends on the approximation accuracy of wavelet function but also on the circuit structure. Most wavelet circuit structures used are cascade and parallel topologies. It is easy to know that the common disadvantage of these topologies is that the sensitivity is higher, in particular as system order increases. Therefore, the MLF structure with low sensitivity will be used for implementing the complex wavelet circuit in this work. The SI is an analog sampled-data signal processing technique, which by overcoming the limitations of the SC offers full compatibility with digital CMOS process. There are some advantages to implement the complex wavelet circuit using this technique. One important advantage is the dilations of a given filter circuit may be easily and very precisely controlled. Implementing dilations via SI circuits, the easy approach involves controlling the various clock frequencies of the circuits with the same system architecture. Such accuracy is in general unachievable

using conventional analog designs. Then the complex wavelet circuit design will be based on MLF structure with SI bilinear integrators and current mirrors as the main building blocks.

Let us consider the arbitrary order analog filter function given by (19), where $A_i (i = 0, 1, \dots, n)$ and $B_i (i = 0, 1, \dots, n)$ are real coefficients.

$$H(s) = \frac{A_n s^n + A_{n-1} s^{n-1} + A_{n-2} s^{n-2} + \dots + A_1 s + A_0}{B_n s^n + B_{n-1} s^{n-1} + B_{n-2} s^{n-2} + \dots + B_1 s + B_0} \quad (19)$$

The signal flow graphs (SFG) of possible candidates for realizing the transfer function in (19) is given in Fig.4. The SFG in Fig.4 corresponds to a Follow the Leader Feedback (FLF) topology. The transfer function that is derived according to the SFG in Fig.4 is given by (20) as:

$$H(s) = \frac{a_n s^n + \frac{a_{n-1}}{\tau_1} s^{n-1} + \frac{a_{n-2}}{\tau_1 \tau_2} s^{n-2} + \dots + \frac{a_1}{\tau_1 \tau_2 \tau_3 \dots \tau_{n-1}} s + \frac{a_0}{\tau_1 \tau_2 \tau_3 \dots \tau_n}}{b_n s^n + \frac{b_{n-1}}{\tau_1} s^{n-1} + \frac{b_{n-2}}{\tau_1 \tau_2} s^{n-2} + \dots + \frac{b_1}{\tau_1 \tau_2 \tau_3 \dots \tau_{n-1}} s + \frac{b_0}{\tau_1 \tau_2 \tau_3 \dots \tau_n}} \quad (20)$$

$$= \frac{a_n s^n + \sum_{j=1}^{n-i} (a_i / \prod_{j=1}^{n-i} \tau_j) s^i}{b_n s^n + \sum_{j=1}^{n-i} (b_i / \prod_{j=1}^{n-i} \tau_j) s^i}, i = 0, 1, 2, \dots, n-1$$

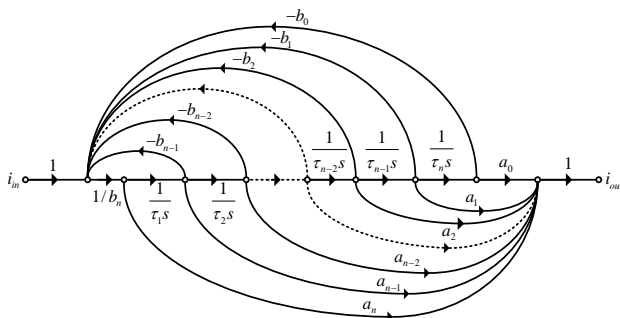


Fig.4 The SFG of FLF structure in the current model

By equating both numerator and denominator coefficients of (19) and (20), the values of a_i and b_i are readily obtained as:

$$a_n = A_n, a_i = A_i / \prod_{j=1}^{n-i} \tau_j, i = 0, 1, 2, \dots, n-1 \quad (21)$$

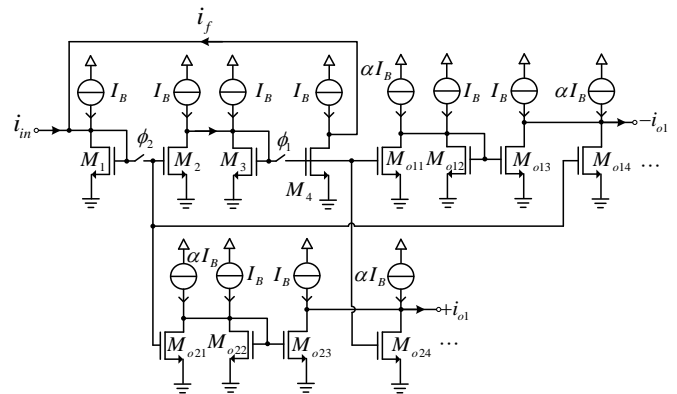
$$b_n = B_n, b_i = B_i / \prod_{j=1}^{n-i} \tau_j, i = 0, 1, 2, \dots, n-1 \quad (22)$$

As is well known, the SFG in Fig.4 corresponds to the continuous time systems. In order to implement the complex wavelet circuit using analog sampled-data SI technology, the s -domain FLF topology as shown in Fig.4 should be mapped into z -domain by applying bilinear transform ($s \rightarrow 2(z-1)/T(z+1)$). The basic building blocks of the complex wavelet circuit such as SI bilinear integrators and current mirrors will be described in the following.

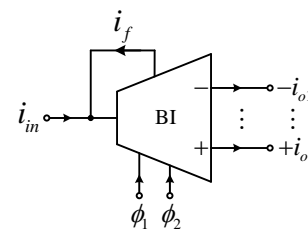
A single-input multiple-output SI bilinear integrator and symbol are shown in Fig.5. The transfer function of this SI integrator is:

$$H(z) = \frac{\pm i_{o1}}{i_{in}} = \pm \alpha \frac{z+1}{z-1} \quad (23)$$

where $+i_{o1}$ and $-i_{o1}$ are in phase and reverse phase output of the integrator, respectively. α is the parameter value of the transistor.



(a) Switched-current bilinear integrator



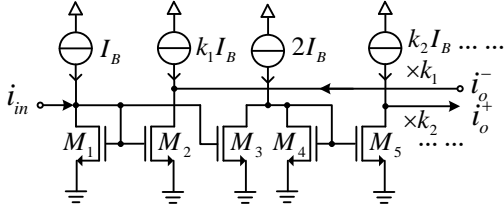
(b) Symbol

Fig.5 Switched-current bilinear integrator and symbol

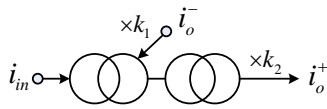
The typical topology of a multiple output current mirror, with arbitrary gain at each output, is that depicted in Fig.6. The required scaling factors are realized by properly sizing the corresponding NMOS transistors of the branch associated with this factor. The input-output relation is

$$\frac{i_o^-}{i_{in}} = -k_1, \quad \frac{i_o^+}{i_{in}} = k_2 \quad (24)$$

where i_o^- and i_o^+ are in phase and reverse phase output of the current mirror, respectively. k_1, k_2 are the scaling factors.



(a) Current mirror



(b) Symbol

Fig.6 Current mirror and symbol

According to the transfer functions in (17) and (18), the common complex Gabor wavelet circuits with SI bilinear integrators and current mirrors as the basic elements can be realized as shown in Fig.7. The general formulas of $\alpha_i, \alpha_{fi}, \alpha_{ci}, k_1$ and k_2 in the designed circuits are given as:

$$\alpha_i = T / 2\tau_i, i = 1, 2, \dots, n \quad (25)$$

$$\alpha_{f(n-i)} = \alpha_i \cdot b_{n-i} = (T / 2\tau_i) B_{n-i} \prod_{j=1}^i \tau_j, i = 1, 2, \dots, n \quad (26)$$

$$\alpha_{c(n-i)} = \alpha_i \cdot a_{n-i} = (T / 2\tau_i) A_{n-i} \prod_{j=1}^i \tau_j, i = 1, 2, \dots, n \quad (27)$$

$$k_1 = 1/b_n, \quad k_2 = \pm a_n / b_n \quad (28)$$

The behavior of the circuits in Fig.7 will be evaluated through simulation results by employing the ASIZ software.

5. Simulations and Analysis

To validate the system principle and to check the circuit performance, the whole system has been simulated in ASIZ. Firstly, we may calculate the circuit

parameters of real and imaginary outputs of the complex wavelet circuit from (25) to (28), respectively. The obtained circuit parameters are described as follows:

$$\begin{aligned} \alpha_{f_0}^r &= 0.0956, \alpha_{f_1}^r = 0.2957, \alpha_{f_2}^r = 0.4418, \alpha_{f_3}^r = 0.4569, \\ \alpha_{f_4}^r &= 0.2823, \alpha_{f_5}^r = 0.6153, \alpha_{f_6}^r = 0.3196, \alpha_{c_6}^r = 0.3668, \\ \alpha_{c_5}^r &= 2.0138, \alpha_{c_4}^r = 2.9360, \alpha_{c_3}^r = 10.8125, \alpha_{c_2}^r = 25.1445, \\ \alpha_{c_1}^r &= 38.6523, \alpha_{c_0}^r = 19.0234, \alpha_1^r = 0.2, \alpha_2^r = 0.4, \alpha_3^r = 0.1, \\ \alpha_4^r &= 0.1, \alpha_5^r = 0.1, \alpha_6^r = 0.1, \alpha_7^r = 0.1, k_1^r = 1, k_2^r = 0 \end{aligned} \quad (29)$$

$$\begin{aligned} \alpha_{f_0}^i &= 0.0320, \alpha_{f_1}^i = 0.1446, \alpha_{f_2}^i = 0.2311, \alpha_{f_3}^i = 0.2952, \\ \alpha_{f_4}^i &= 0.1870, \alpha_{f_5}^i = 0.4961, \alpha_{f_6}^i = 0.2536, \alpha_{c_6}^i = 0.5949, \\ \alpha_{c_5}^i &= 2.5088, \alpha_{c_4}^i = 3.1781, \alpha_{c_3}^i = 8.8984, \alpha_{c_2}^i = 17.0469, \\ \alpha_{c_1}^i &= 14.4785, \alpha_{c_0}^i = 0.1637, \alpha_1^i = 0.2, \alpha_2^i = 0.4, \alpha_3^i = 0.1, \\ \alpha_4^i &= 0.1, \alpha_5^i = 0.1, \alpha_6^i = 0.1, \alpha_7^i = 0.1, k_1^i = 1, k_2^i = 0 \end{aligned} \quad (30)$$

Then we set the transconductances of the transistors in the relevant circuits according to (29) and (30). Other unlisted transconductances of the transistors in the circuits are all set as 1. Meanwhile, the sampling frequencies are selected as 1kHz, 500Hz and 250Hz, respectively. The different scale impulse responses of the real and imaginary outputs of the complex Gabor wavelet circuit are shown in Fig.8 and Fig.9, respectively. In Fig.8, the impulse responses of different scale ($a=1,2,4$) real part circuits achieve the positive peak values 0.9459A at 26ms, 52ms and 104ms, which is in agreement with the normalized ideal value. In Fig.9, the impulse responses of imaginary part circuits at $a=1, 2, 4$, achieve the positive peak values 0.6555A at 20.5ms, 41ms and 82ms, which is highly closed to the normalized ideal value. The time-domain simulation results of the complex Gabor wavelet circuit can be compared with the ideal Gabor function to confirm the performance of the designed circuit.

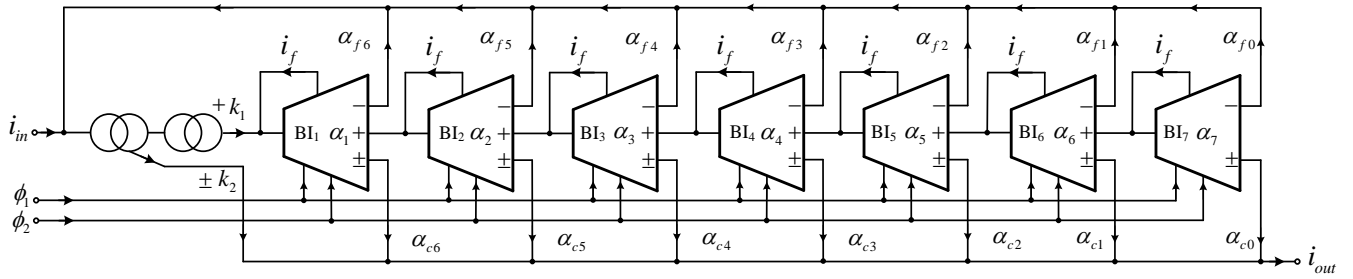


Fig.7 The real and imaginary parts circuit using SI bilinear integrators and current mirrors

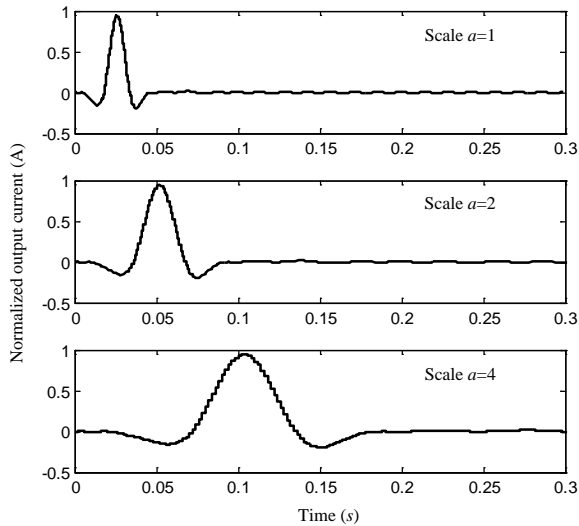


Fig.8 Simulated impulse responses by changing clock frequency of the real part circuit

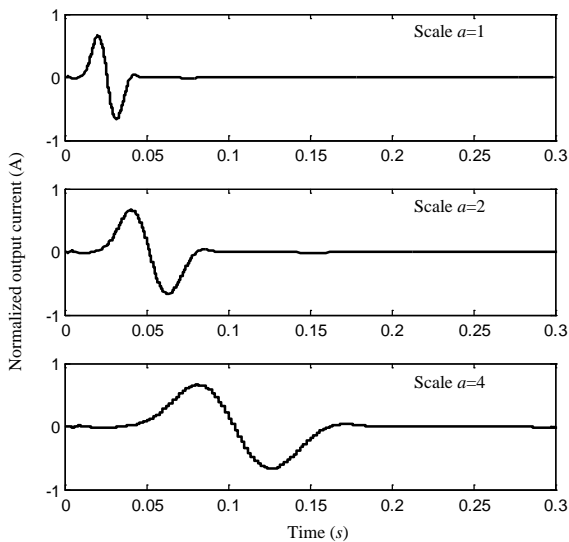


Fig.9 Simulated impulse responses by changing clock frequency of the imaginary part circuit

The designed SI complex Gabor wavelet circuit has the merit of low sensitivity. In order to testify this characteristic, we will calculate the error margins of frequency response curve due to the uncorrelated errors in the components. Uncorrelated 3% random errors are considered for all the transconductances in the proposed circuits. Fig.10

and Fig.11 show the gain curves with errors computed for the real and imaginary part circuits, respectively, using the ASIZ program. The dotted lines represent the error margins for the designed circuits, computed as the statistical deviation of the gain. The transistors are considered as ideal current sources in the sensitivity analysis. The curves show the lower sensitivity of the SI complex wavelet circuits, due to the MLF structure, and the advantage of the circuit with SI bilinear integrators.

Overall, it is clear that the proposed approach here has excellent performance for the implementation of the complex Gabor wavelet transform and can be used for other SI circuit design as well.

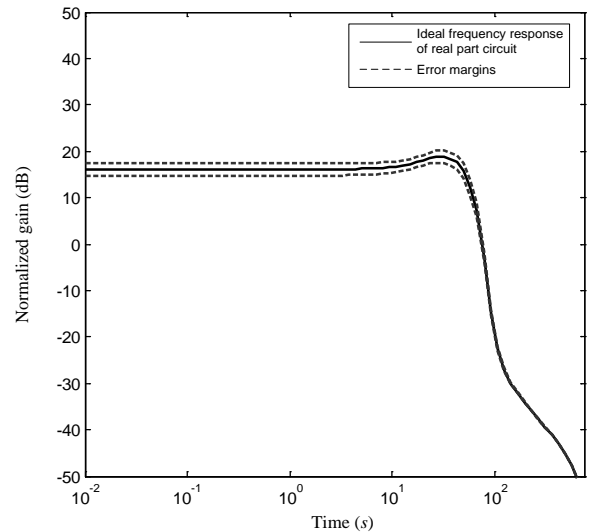


Fig.10 Frequency responses with error margins of the real part circuit

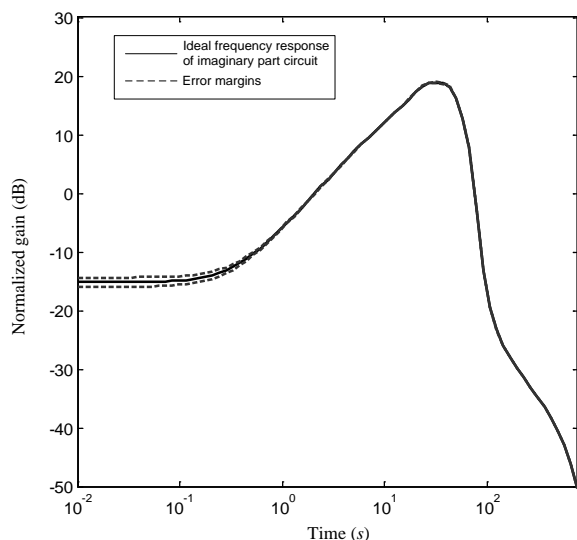


Fig.11 Frequency responses with error margins of the imaginary part circuit

5 Conclusion

The complex Gabor wavelet transform circuit with FLF MLF structure realized using SI bilinear integrators and current mirrors as basic elements, has been presented in this brief. The SVD approximation approach for fitting the impulse response of the analog system performs markedly simpler than earlier methods such as Padé, L_2 and those intelligent optimization algorithms. In addition, it can easily be applied to other wavelet approximation as well. The designed complex wavelet transform circuit has low sensitivity and litter effect to the transistor errors. From the results obtained, we deduced that the proposed method could very well be used to implement other CWT and to design other SI circuits for signal processing in the analog fashion.

6 Acknowledgment

This work was supported by the National Natural Science Foundation of China under Grant Nos. 61404049 and 61274026, the National Natural Science Foundation of China for Distinguished Young Scholar under Grant No.50925727, the Science and Technology Plan Foundation of Hunan Province under Grant Nos. 2013FJ2011 and 2014FJ2017, and the Xiangtan Science and Technology Foundation of China under Grant No. CG20121006.

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