Design of 33-40GHz Low Power VCO in 90-nm CMOS Technology

ZHU LI[1,2], ZhIGONG WANG[1], ZHIQUN LI[1], QIN LI[1]
[1]Institute of RF- & OE-ICs (IROI) of Southeast University (SEU)
[2]Nanjing University of Science and Technology (NUST)
No. 2, Si Pai Lou, Nanjing 210096
PEOPLE'S REPUBLIC OF CHINA
zhuli7794@163.com

Abstract:-This paper presents the IC design of a low power, wide tuning range and low phase noise voltage-controlled oscillator (VCO) in a standard 90-nm CMOS technology. The newly proposed current-reuse cross-connected pair is utilized as a negative conductance generator to compensate the energy loss of the resonator. The supply current is reduced by half compared to that of the conventional LC-VCO. An LC tank with switched capacitor is used to extend the overall VCO tuning range. The VCO achieves a tuning range of 33~40.4 GHz exhibiting a frequency tuning range (FTR) of 20.2%, a phase noise of -103.4 dBc/Hz at 1-MHz offset from 36-GHz carrier and showed an excellent FOM of –189dB. With the voltage supply of 1.5 V, the core circuit of VCO draws only 1.9mA DC current. The VCO is fully differential and integrated in a PLL circuit in the 90-nm CMOS technology.

Keywords:- CMOS, Microwave, millimeter wave, Switched capacitor, Phase noise, VCO.

1 Introduction

There has been growing interest in millimeter wave communication systems promoted by the ever increasing bandwidth requirement from the emerging low-power smart devices. The continued down-scaling of silicon technology presents numerous challenges for the design of wide tuning range VCOs, especially in microwave and mm wave band[1]. In the transmitter and receiver of mm-wave communication, the VCO is generally used in a PLL (phase-locked loop) or a frequency synthesizer circuit and therefore plays a critical role.

In this paper, a proposed VCO topology which replaces one of the NMOSs of a conventional all-NMOS differential LC-VCO with a PMOS is presented. The design guidelines and implementation of the new VCO are reported. Frequency tuning is accomplished using AMOS varactors. The impact of gate length(l) on the capacitance ratio(r) and the quality factor(Q) of the AMOS varactor is analyzed in great detail. In order to achieve a better phase noise performance, a switched capacitor in parallel with the varactor is used to divide the tuning range into two sub−bands, such that a wide tuning range can be realized with a smaller KVCO for each sub-band[2] . The VCO achieves a tuning range of 33~40.4 GHz, a phase noise of –103.4dBc/Hz at 1-MHz offset from 36-GHz carrier and showed a FOM of –189dBc/Hz. The frequency tuning range increased to 20.2%. The DC current is only1.9 mA under 1.5-V supply.

2 Design Theory

2.1 Principles of the LC Oscillators

The typical circuit of an LC oscillator is shown in Fig.1(a), and it is usually described as a negative-resistance model.

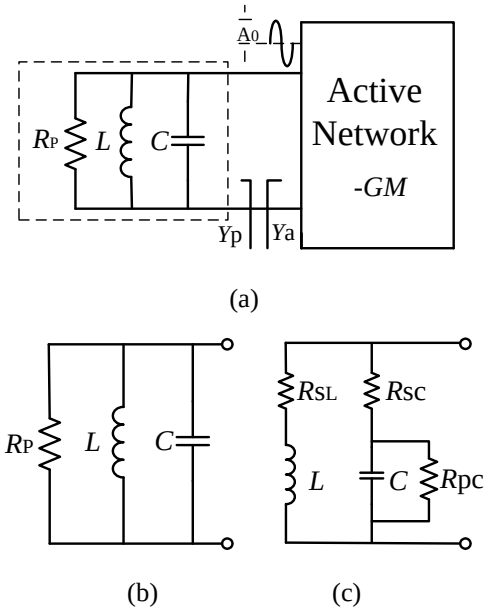


Fig.1 LC oscillator model

The input admittance (Y_a) of the active network in Fig.1(a) is (-*GM*).The oscillation takes place when negative admittance (-*GM*) cancels the conductance (Y_p=1/R_p) and the whole network reduces to an ideal LC resonant tank. At resonance, the capacitive and the inductive reactance cancel each other out and the oscillation frequency is determined by $\omega_o=(LC)^{-1/2}$. Note that R_p is just a model component, in order to analyze the real losses of the reactive components, Fig.1(c) shows a more realistic model for both the inductor and the capacitor shown in Fig.1(b). The components are shown with their series resistances R_{SL} and R_{SC}, which account for the losses through the current path. The shunt resistor R_{PC} represents dielectric losses of the capacitor. The *Q* factor of the capacitor affected by losses due to the resistance R_{SC} is $Q_{SC}=1/(\omega_o R_{sc} C)$ and $Q_{PC}=\omega_o R_{pc} C$. For the inductor, the quality factor is $Q_L=(\omega_o L)/R_{sL}$. Assume that $R_{sL}<<\omega_o L$, $R_{sc}<<1/(\omega_o C)$ and $R_{pc}>>1/\omega_o C$, A_0 is the oscillation amplitude, the peak inductor current is approximately $A_0/\omega_o L$. The average power dissipated across R_{SL}, R_{SC} and R_{pC} are given as follows, respectively:

$$P_{sL} \approx \frac{1}{2}\left(\frac{A_0}{\omega_0 L}\right)^2 R_{sL} \quad (1)$$

$$P_{sC} \approx \frac{1}{2}(A_0\omega_0 C)^2 R_{sC} \quad (2)$$

$$P_{PC} \approx \frac{1}{2}\frac{A_0^2}{R_{PC}} \quad (3)$$

The *Q* factor definition is:

$$Q = 2\pi(E_r / E_d) \quad (4)$$

E_r is the maximum energy stored by the reactive components and E_d is the dissipated energy per cycle, T_0 is the oscillation period.

$$E_r = C\frac{A_0^2}{2} \quad (5)$$

$$E_d = (P_{SL} + P_{SC} + P_{PC})T_0 \quad (6)$$

According to (4) (5) and (6), the overall *Q* factor of the tank is given by[3]:

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_{SC}} + \frac{1}{Q_{PC}} \quad (7)$$

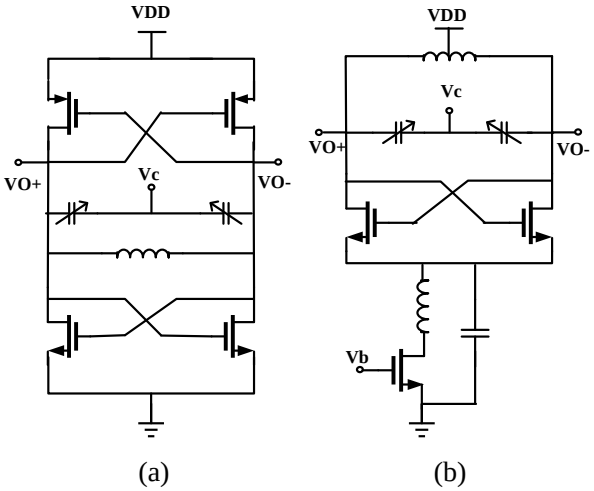
Equ.(7) above links the *Q* factor to the losses of each reactive components. It shows that the overall quality factor is limited by the reactive element with the highest losses, i.e., with lowest quality factor.

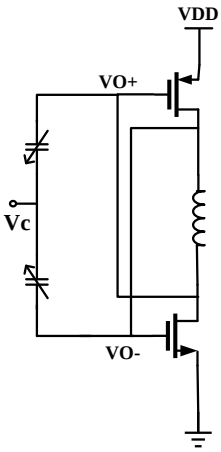
The formula of Lesson phase noise can be written as:

$$L(\Delta\omega) = \frac{KT}{C}\left(\frac{\omega_0}{Q}\right)\frac{(1+F)}{(A_0\Delta\omega)^2} \quad (8)$$

where *F* is the excess noise factor of the amplifier[4], Δω is the frequency offset from the carrier. From Equ.(8), we can see that the higher the *Q* is, the better the phase noise would be.

2.2 Circuit Topology



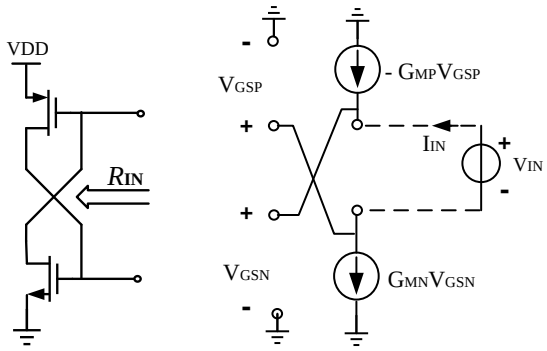


(c)

Fig.2 Schematics of oscillator
(a) (b):Conventional VCO topology
(c):Proposed VCO topology

Fig.2(a) shows an LC-tuned oscillator using complementary crossed coupled transistor pairs. The advantage of this kind of topology is the re-use of the bias current to make it possible to reach twice the transconductance for a given bias current. However, in the design of an oscillator, transistor parasitic capacitances of the NMOS pair and the PMOS pair reduce the achievable tuning range and operation frequency, especially in millimeter wave band. Meanwhile, the second-harmonic terms at the common-source nodes of N- and P-MOS pairs degrade the performance of phase noise. An all-NMOS VCO is shown in Fig.2(b) and an NMOS transistor is presented with an LC filter as a current source. Because the noise around the frequency $2Nf_0$ can affect the VCO's phase noise significantly through the up-conversion, the LC filter is optimized to oscillate at $2f_0$ to eliminate the influence of this kind of noise. However, this topology can't meet the demand of the wide tuning range of this project, since the LC tank is inherently a narrow band filter.

Considered the wide tuning range and the high frequency utilization, the schematic of the newly proposed current-reuse differential LC-VCO is shown in Fig.2(c).The new LC-VCO replaces one of the NMOSs of a conventional all-NMOS differential LC-VCO(shown in Fig.2(b)) with a PMOS. The new VCO uses both NMOS and PMOS transistors in the cross-connected pair as a negative conductance generator to compensate the losses in the LC-tanks.



(a) (b)

Fig.3 (a)The proposed cross-connected pair
(b)Small-signal equivalent circuits of (a)

Fig.3 shows the proposed cross-connected pair and the small-signal equivalent circuits of the topology. The negative conductance of the new LC-VCO can be derived as follows.

$$V_{GSP} = -V_{GSN}, \quad I_{IN} = -G_{MN}V_{GSN} \qquad (9)$$

$$R_{IN} = \frac{V_{IN}}{I_{IN}} = \frac{V_{GSN} - V_{GSP}}{I_{IN}} = -\frac{2}{G_{MN}} \qquad (10)$$

The advantages of the new VCO topology are:

1) The series stacking of N- and P-MOSs allows the power dissipation to be reduced by half compared to that of the conventional LC-VCO while providing the same negative conductance, and the utilization of PMOS transistor in the cross-connected pair can help to obtain a lower phase noise than all-NMOS VCOs, owing to $1/f$ noise and the hot carrier effect of PMOS transistors being much less than NMOS transistors.

2) Compared with the conventional differential VCO where the transistors switch alternately, this VCO does not have a common-source node because the transistors switch on and off at the same time. Therefore, the proposed VCO is inherently immune to the phase noise degradation caused by second-harmonic terms at the common-source node.

3) The proposed VCO can offer a wide tuning range because the DC levels of the two outputs are approximately half of the supply voltage.

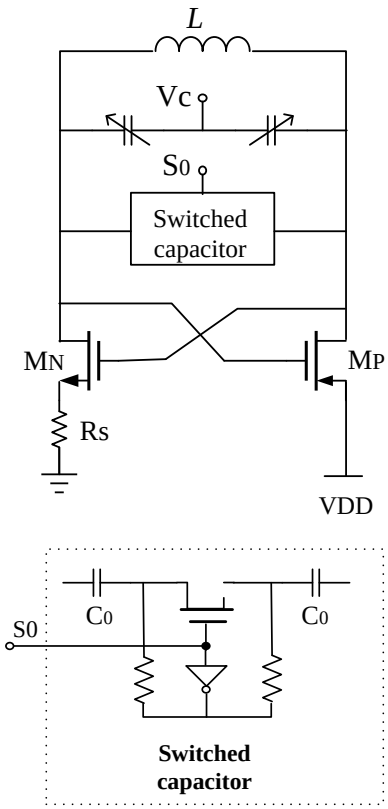
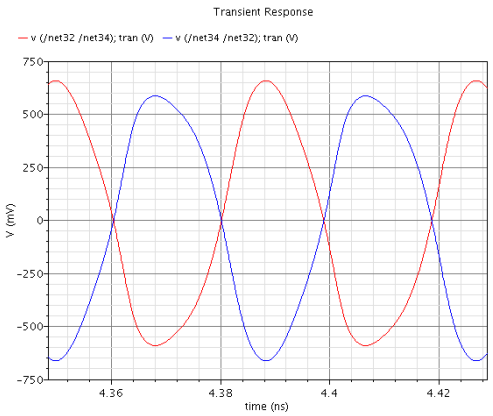
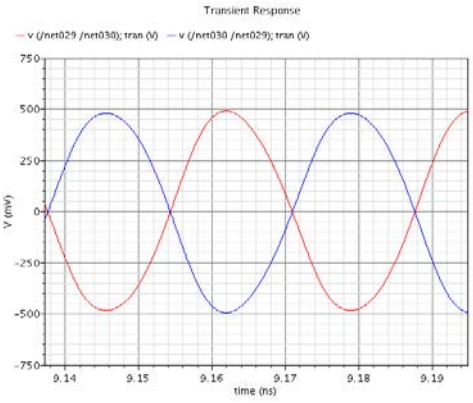


Fig.4 The schematic of VCO



(a)



(b).

Fig.5 Differential output voltage
(a) Voltage limited mode (Rs=0)
(b) Current limited mode (Rs≠0).

The schematic of the cross-connected differential VCO of this work is shown in Fig.4. Resistor R_s, in series of NMOS MN, is used to control the DC current as well as the peak dynamic current of the proposed VCO. When R_s=0, the oscillator can operate in a voltage-supply-limited mode and lead to voltage-waveform distortion. Therefore, by properly selecting the resistor, the proposed VCO can operate in a current-limited mode, rather than the voltage limited mode. Fig.5 shows the output voltage of the proposed VCO when it operates in the voltage limited mode (R_s=0) and the current limited mode (R_s≠0). The output voltage shows that, in the current-limited mode, the voltage swing represent well-balanced behavior during the two half periods.

The LC-tank in the Fig.4 consists of 1) a single-loop differential spiral copper inductor that is estimated to be 210 pH with a quality factor about 25 at 30 GHz, simulated by EM simulator HFSS[5], 2) the AMOS varactors. The outputs are buffered using source-followers for measurement purposes, and 3) switched MIM (mental-insulator-mental) capacitors which are used to widen the frequency tuning range. When the switching transistors are off, the parasitics of the transistors could degrade the switched capacitor. The switched components have to be carefully designed and laid out to maintain better performance and the details are given in the following subsections.

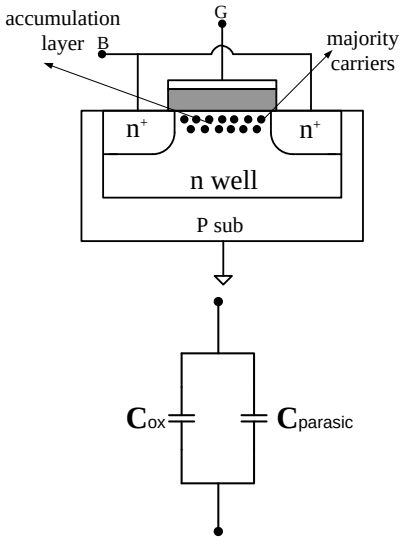
3 Design of the Passives

3.1 AMOS Varactor

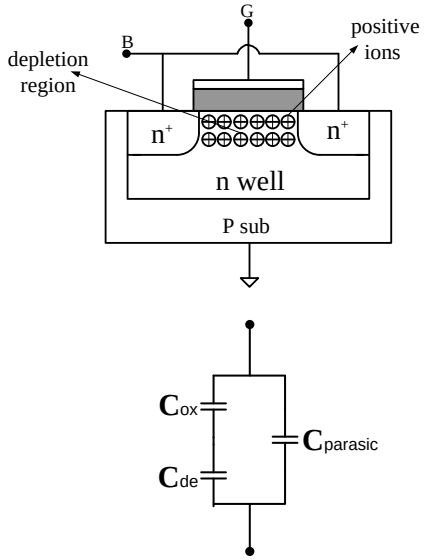
Frequency tuning in integrated LC VCO is accomplished using a variable capacitance, The AMOS varactor has recently been a popular choice for an LC resonator. In this application, the AMOS varactor is characterized by its quality factor(Q) and by the capacitance ratio factor $r=C_{max}/C_{min}$. In general, in order to achieve better phase-noise performance, it is desirable for the LC resonator to have a high Q value and a large varactor with high capacitance ratio for a wider frequency tuning range, because

$$TR(\%)=\frac{\Delta f}{f_0}\times 100\%=2\frac{\sqrt{1/LC_{min}}-\sqrt{1/LC_{max}}}{\sqrt{1/LC_{min}}+\sqrt{1/LC_{max}}}\times 100\% \quad (11)$$
$$=\frac{\sqrt{r}-1}{\sqrt{r}+1}\times 200\%$$

where Δf is f_H-f_L the maximum frequency change around the center frequency $f_0=(f_H+f_L)/2$. Unfortunately, its Q factor drops quickly as frequency rises and r is influenced by parasitic capacitance when operating at high frequency especially in the mm-wave region. In this section, the structure and operation of the AMOS capacitor is reviewed and explained briefly using basic device physics and a simplified varactor model.



(a)



(b)

Fig.6 An n-type AMOS varactor structure and simplified equivalent model
(a) Accumulation mode, (b) Depletion mode

The cross-section of an n-type AMOS varactor and its simplified equivalent models are shown in Fig.6. The structure is very similar to an n-type MOSFET, except that both the channel and source/drain regions are doped with the same dopants, which is n-type in this case. The capacitance is measured between the bulk and the gate, when V_{GB} is biased at a positive voltage. An accumulation layer of electrons is created below the gate and the capacitance is almost equal to the gate oxide contribution (C_{ox}) (Fig.6(a)) which is the maximum capacitance C_{vmax}. Instead, when V_{GB} decrease to be negative, more electrons are attracted to the substrate connection, leaving the positive ions in the gate area and the depletion region is formed (Fig.6(b)). Therefore, the small-signal capacitance of the varactor is the series of the oxide and the depletion capacitance. Because of the suppression of injection of holes in the MOS channel, the strong, moderate, and weak inversion regions is inhibited[6]. The capacitance decrease until the inversion region is reached and the minimum capacitance is obtained. With the continued dropping of V_{GB}, the capacitance almost maintains constant and owing to the larger C_{ox} value, the minimum varactor C_{vmin} capacitance may be approximated equal to the depletion capacitance C_{de}. The parasitic capacitor $C_{parasic}$ will be discussed

latter.

The Q factor of A-MOS varactor is defined as:

$$Q_{\text{var}} = \frac{1}{\omega C_{\text{var}} R_{\text{var}}} \tag{12}$$

C_{var} can be expressed as:

$$C_{\text{var}} = \hat{C}_{ox} \cdot w \cdot l \tag{13}$$

where $\hat{C}_{\text{ox}}$ is the gate-oxide capacitance per square. In accumulation mode, $\hat{C}_{\text{ox}} = \varepsilon_{ox}/t_{ox}$ and then

$$C_{\text{var}} = C_{\text{ox}} = C_{v\max} = \hat{C}_{ox} \cdot w \cdot l \tag{14}$$

which represent the maximum capacitance. With the reduction of V_{GB}, the depletion region is formed and the varactor gradually reduced to the minimum capacitance. Then

$$C_{\text{var}} = C_{\text{de}} = C_{v\min} = \hat{C}_{de} \cdot w \cdot l \tag{15}$$

where $\hat{C}_{\text{de}}$ is the depletion capacitance per unit of gate area.

The main contributions to R_{var} losses are two resistors, one is the drain-source resistance R_{ch} of the channel, another is the gate resistance R_{G} due to the finite poly-silicon conductivity. Both of them are in series with the C_{var}.

$$R_{\text{var}} = R_{Ch} + R_G \propto \left(\frac{l}{w} R_{Ch}^{\ sq} + \frac{1}{n_f}\frac{w}{l} R_G^{\ sq}\right) \tag{16}$$

Where $R_{\text{ch}}^{\text{sq}}$ and R_G^{sq} are sheet resistance of the channel and of the polysilicon and n_f is the number of fingers. If double-sided taped gate and multi-fingers are employed, the second resistance R_{G} is usually less important than R_{ch} and can be negligible. Solving (12)-(16) gives the relationship

$$Q \propto \frac{t_{\text{ox}}}{\omega_0 \varepsilon_{\text{ox}} l^2 R_{ch}^{\ sq}} \propto \frac{1}{l^2} \tag{17}$$

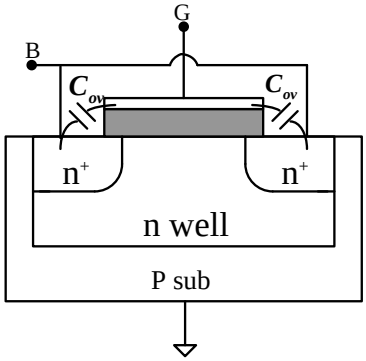


Fig.7 Parasitic capacitances in a MOS varactor

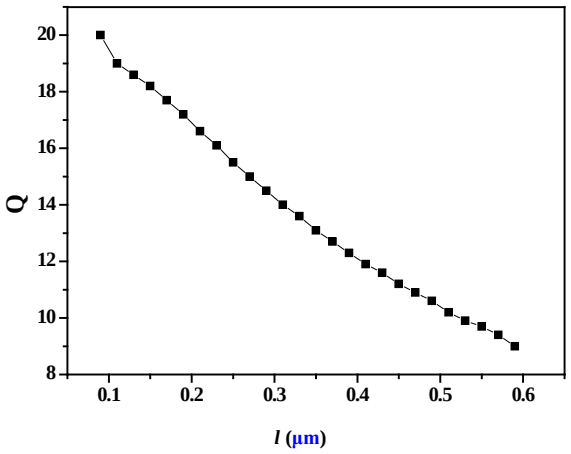
Therefore, for a given technology, the quality factor Q of the AMOS varactor reaches the maximum by using minimum gate length. However, the tuning range varied in the opposite way. Considering the parasitic overlap capacitance C_{ov}, shown in Fig.7, this term can be presented as $C_{\text{ov}} = 2w\hat{C}_{\text{ov}}$ where $\hat{C}_{\text{ov}}$ is the parasitic capacitance per unit of gate width. The tuning range can be given by

$$r = \frac{C_{\max}}{C_{\min}} = \frac{C_{v\max} + C_{ov}}{C_{v\min} + C_{ov}} = \frac{\hat{C}_{ox} \cdot wl + C_{ov}}{\hat{C}_{de} \cdot wl + C_{ov}} \tag{18}$$

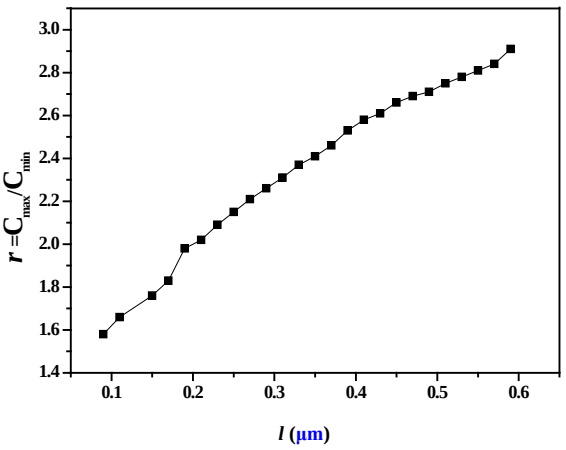
As the capacitance of C_{ox} is much larger than that of C_{de} and C_{ov}, it turns out that

$$\tilde{r} = \frac{\hat{C}_{ox} \cdot wl}{\hat{C}_{de} \cdot wl + C_{ov}} = \frac{\hat{C}_{ox} \cdot wl}{\hat{C}_{de} \cdot wl + \hat{C}_{ov} \cdot 2w} = \frac{\hat{C}_{ox} \cdot l}{\hat{C}_{de} \cdot l + \hat{C}_{ov} \cdot 2} \tag{19}$$

Obviously, r improves as l increases and the maximum value is $\hat{C}_{\text{ox}}/\hat{C}_{\text{de}}$.



(a)



(b)

Fig.8The dependence of the *Q* and *r* values as functions of the channel length *l*

(a) *Q* factor versus channel length *l*

(b) Capacitance ratio *r* versus channel length *l*

The two-port S-parameters were simulated with the drain node (S, D) and the gate node as the ports. From the two-port S-parameters, the admittance looking from the drain was calculated from (20), while the *Q* was calculated as in (21):

$$Y = Y_0 \frac{1 - S_{11}}{1 + S_{11}} \tag{20}$$

$$Q = \frac{Im(Y)}{Re(Y)} \tag{21}$$

The AMOS varactor used for simulation has a width (*W*) of 2um and 10 fingers. Fig.8 shows the dependence of the *Q* and *r* values as functions of the channel length *l* for the component in 90nm technology at 30 GHz. The quality factor *Q* improves by reducing the channel length *l* but the ratio *r* drops instead and tradeoff exists between the tuning range and the quality factor(*Q*). In this work, the length (*l*) of AMOS varactor is 400 nm.

3.2 Switched Capacitor

A wider VCO frequency band can be tuned by combination of MOS varactors and switched fixed MIM capacitors as shown in Fig.9.

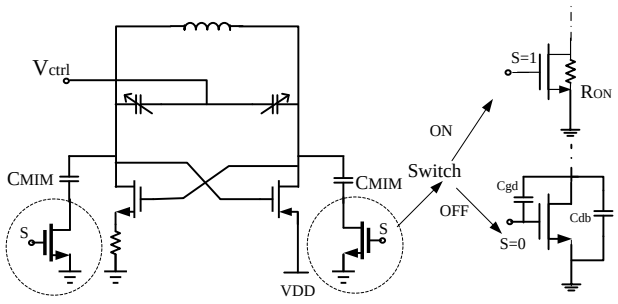


Fig.9 VCO with switched fixed MIM capacitors

The switch is implemented by an NMOS transistor. The switch has two states, ON and OFF. When the transistor is in the ON state（S=1）, it can be replaced by a resistor equals to R_{ON} and the mental capacitance C_{MIM} loads the tank. Using a simple transistor model, the ON resistance can be calculated as:

$$R_{ON} = \frac{1}{(w/l)\mu C_{ox}(V_{DD} - V_{th})} \tag{22}$$

Where μ, C_{ox}, *w*, and *l* are the mobility, gate oxide capacitance per area, width, and length of the transistor. The quality factor of the resulting series *RC*-link is equal to

$$Q = \frac{1}{2\pi f R_{ON} C_{MIM}} \tag{23}$$

The *Q* value may be improved by increasing the transistor width, *w*. When the transistor is turned OFF(S=0), ideally, the capacitance is floating, and does not load the tank. In reality, the transistor is instead dominated by the parasitic capacitance C_p which is usually much small than C_{MIM}. C_p includes gate–drain overlap capacitance C_{gd} and drain-bulk capacitance C_{db}, and $C_p = C_{gd} + C_{db}$. All these parasitic capacitances are proportional to the width of the transistor. A wider MOS switch has a lower R_{ON} and a higher quality factor, at the expense of a reduced capacitance ratio. Again, a trade-off between capacitance ratio and quality factor exists.

The use of two identical tuning circuits enables switched tuning of a differential oscillator, as shown in Fig.9. The major drawbacks of this topology are that when a branch is turned ON it will contain two R_{ON} in series with the C_{MIM}. This limits the achievable quality factor. An improved switched tuning circuit for differential oscillator is shown In Fig.10. The function of the inverter and

the resistors here is that the transistor can get maximum gate to source (and drain) voltage to make sure it is on at all times in the on state. In the off state, the large resistors is used to fix the drain (and source) voltage to VDD and then reduce and get a better control of the parasitic capacitance due to the reverse biased drain-substrate junction.

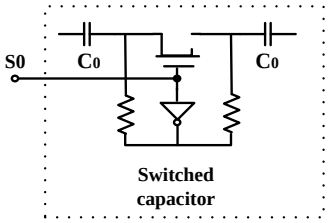
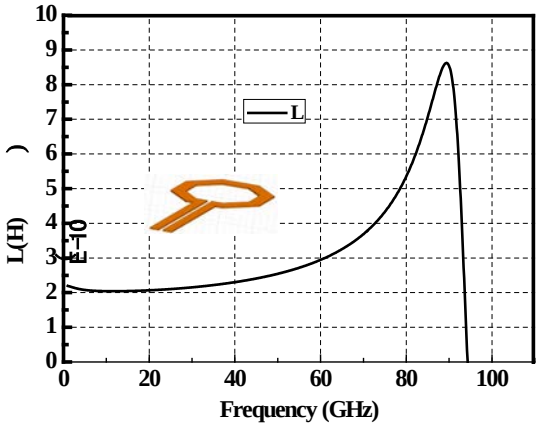


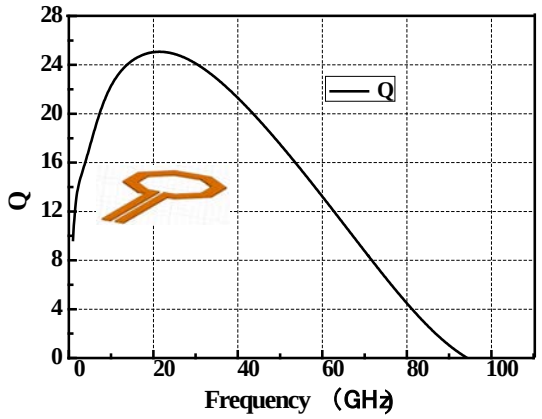
Fig.10 An improved switched tuning circuit for differential oscillator

3.3 Inductor

As the operating frequency increases to the mm-wave band, the inductance required for the LC tank decreases in proportion. The use of a smaller single-loop inductor allows larger varactors (hence, better tuning) and has lower substrate capacitance due to smaller area. At the same time, the single-turn structure eliminates interwinding parasitic capacitance and hence improves the self-resonance frequency. In this design, a single-loop octagon inductor used in the VCO has a diameter of 40 μm. The inductor is constructed by the top layer of 3.4-μm-thick copper in a standard CMOS process. Electromagnetic (EM) simulators HFSS was used for simulation. The simulated characteristics of L and Q are shown in Fig.11(a) and (b). The inductor is estimated to be 210pH with a quality factor about 25 at 30 GHz.



(a)



(b)

Fig.11 The simulated characteristics of the inductor

4 Measured Results

The proposed circuit was fabricated in standard TSMC 90-nm CMOS technology. Source follow buffers were employed at each output to drive the 50-Ω input impedance of testing instruments. Fig. 12 shows the microphotograph of the test chip with an area of 530*470μm^2 including output buffers and input/output (I/O) pads.

Fig.13 shows the oscillation frequency of the VCO, according to the measured results, a tuning range of approximately 20.2%, from 33 to 40.4GHz, is achieved. The tuning range without switched capacitor（S=0）is from 36 GHz to 40.4 GHz, With switched capacitor（S=1）, the tuning range is from 33 GHz to 36.1 GHz.

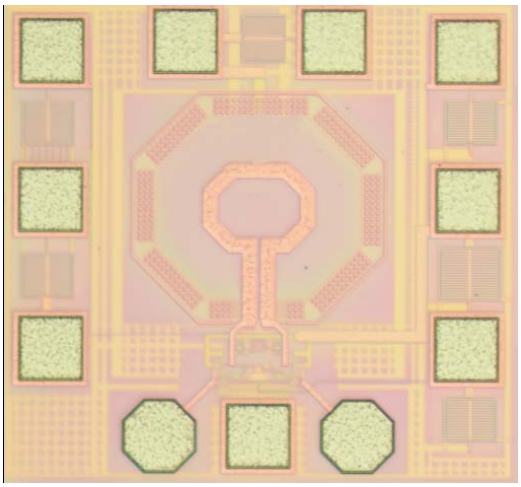


Fig.12 Layout of VCO

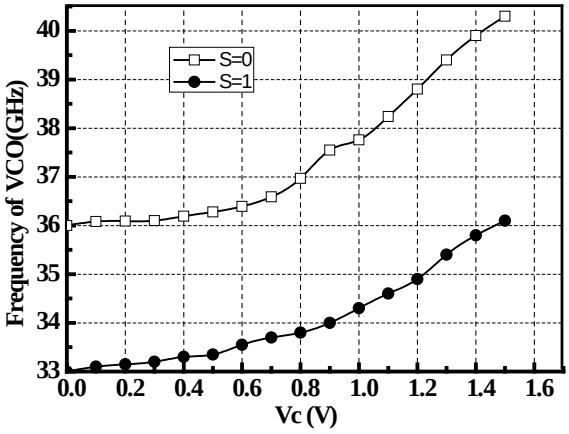


Fig.13 Frequency versus tuning voltage of VCO

The frequency spectrum and phase noise of the VCO's single-end output, measured by an Agilent E4448A spectrum analyzer, are shown in Fig.14 and Fig.15.

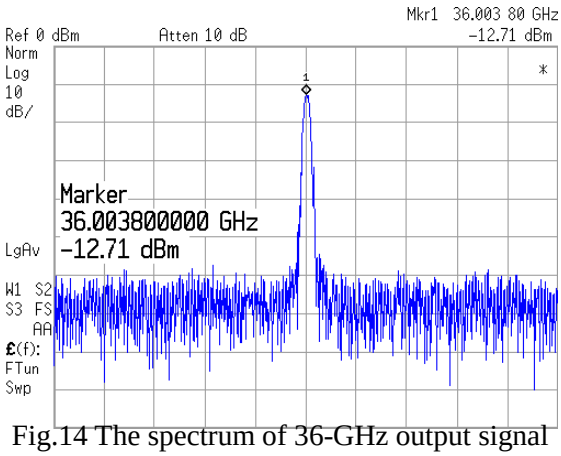


Fig.14 The spectrum of 36-GHz output signal

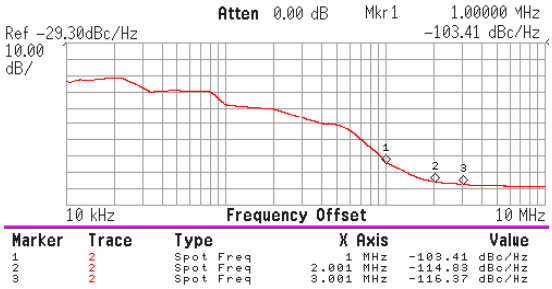


Fig.15 Phase noise of the VCO

The figure of merit (FOM)[7] is defined as

$$\mathrm{FOM} = L(f_{\mathrm{offset}}) - 20\lg\left(\frac{f_0}{f_{\mathrm{offset}}}\right) + 10\lg\left(\frac{P}{1\mathrm{mW}}\right) \quad (24)$$

where $L(f_{\mathrm{offset}})$ is the measured phase noise at the frequency offset from the carrier at f_0, P is the measured dc power dissipation in milliwatt. The *FOM*, calculated using the measurement at 1.5-V with the phase noise at 1-MHz offset from the 36-GHz carrier, is -189dB. Table 1 shows the comparison of the performances for the currently published VCOs. As shown in Table 1, the performance of the proposed VCO is better than the other prior studies.

5 Conclusion

In this paper, we have designed and measured a newly proposed cross-connected VCO working up to 40.4 GHz in a 90-nm CMOS technology. The power consumption was only 2.9mW. The VCO using AMOS varactors in parallel with the switched capacitor provided a wide tuning range of 20.2% from 33 to 40.4 GHz. and the phase noise was –103.4dBc/Hz at a 1-MHz offset frequency at 36 GHz and showed an excellent FOM of –189dB. In summarize, the newly proposed architecture of the VCO shows the advantages of low power, wide tuning range and low phase noise.

6 Acknowledgement

This Project is supported by National Basic Research Program (No. 2010CB327404), National High Technology Research and Development Program (No. 2011AA10305) and the National Natural Science Foundation of China (No. 60901012).

Table 1 Comparison of the Performances for the currently published VCOs

References	[8]	[9]	[10]	This Work
Process	0.13-μm CMOS	65nm CMOS	65nm CMOS	90-nm CMOS
VDD (V)	1.2	1.2	1.2	1.5
Freq.(GHz）	39.6–45.2	34.3-39.9	43.2-51.8	33-40.4
TR (%)	13.2	15	22.9	20.2
Power(mW)	8	14.4	15	2.9
PN(dBc/Hz)@1MHz	-94.6	-118	-117	-103.4
FOM(dB)	-181	-178.4	-179	-189

References

[1] ChanghuaCao,KennethK.O, “Millimeter-Wave Voltage-Controlled Oscillators in 0.13-μm CMOS Technology,” *IEEE JSSC*, vol. 41, pp. 1297-1304, June 2006.

[2] T. Nakamura et al., “A Wide−tuning−range VCO with Small VCO−gain Fluctuation for Multi−band W−CDMA RFIC,” *Proceedings of the European Solid State Circuits Conference*, pp. 448 – 451, Sept. 2006.

[3] Andrea Lacaita ,Salvatore Levantino, Carlo Samori “*Integrated Frequency Synthesizers for Wireless Systems*”

[4] A. jerng and Sutudent member, “The Impact of device Type sizing of Phase noise Mechanisms,” *IEEE Journal of Soled-State Circuits*, vol. 40, no. 2, pp. 360-369, Feb. 2005.

[5] *Electromagnetic Simulation and Optimization. Bay Technology*, Aptos, CA.

[6] Pietro Andreani and Sven Mattisson “On the Use of MOS Varactors in RF VCO’s”， *IEEE Journal of Soled-State Circuits*, Vol. 35, NO. 6, JUNE 2000.

[7] P. Kinget, *Integrated GHz Voltage Controlled Oscillators*. NewYork:Kluwer, 1999.

[8] Ching-Yuan Yang, Chih-Hsiang Chang, Jung-Mao Lin, and Hsuan-Yu Chang “A 20/40-GHz Dual-Band Voltage-Controlled Frequency Source in 0.13-μm CMOS” *IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES*, Vol. 59, NO. 8, AUGUST 2011

[9] M.Nariman, R.Rofougaran, F.D.Flaviis, “A Switched-Capacitor mm-Wave VCO in 65 nm Digital CMOS,” in Proc. *RFIC Conf*. 2010, May. 23–25,2010, pp.157–160.

[10] D.Murphy et al., “A Low Phase Noise, Wideband and Compact CMOS PLL for Use in a Heterodyne 802.15.3c Transceiver,” *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1606–1617, July 2011.