# Simulator Based Device Sizing Technique For Operational Amplifiers

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*Abstract:* In this work, design of CMOS operational amplifiers (opamps) is discussed using a new technique of transistor sizing, called as Potential Distribution Method (PDM). PDM is a technique proposed to simplify analog design and is primarily based on voltage and current distribution at different nodes of a circuit. Apart from being technology independent, PDM is also free from complex mathematical expressions governing the devices and the circuit. Instead of relying on traditional analytical methods, PDM directly uses the simulator as a device sizing tool to meet the desired performance from the circuit. This is achieved by first designing the circuit with moderate performance by logically allocating node voltages and currents, and then modifying the potentials and currents (dc operating points) to meet the target specifications. A fully differential folded cascode opamp is thus designed to illustrate the design methodology. The effect of node voltages and branch currents on response of the opamp is also examined. Thereafter, using these dependencies, the guidelines for tuning the performance parameters to achieve the target specifications are discussed. The methodology demonstration is carried out using UMC 180 $\mathrm{nm}$ CMOS technology at 1.8 $\mathrm{V}$ supply and the simulation results are presented.

*Key–Words:* Analog design, CMOS, operational amplifier, transistor sizing, simulation, fully differential folded cascode.

## 1 Introduction

Designing an analog circuit is becoming more and more difficult as device dimensions are scaling down. Typically, analog designers first design any analog circuit with pen and paper using some device model whose equations can be manipulated with hand calculations [1, 2, 3, 4, 5, 6, 7, 8, 9]. Usually, these models are based on long channel devices (SPICE level 1 or 2), whereas actual devices are deep submicron (DSM) devices which are totally different from long channel in physical and electrical characteristics. Once the device dimensions are obtained mathematically using long channel model, the designer implements the schematic on a simulator. If targeting fabrication, the designer then combines a state-of-the-art simulator with an extremely complex and accurate (DSM) device models like BSIM3,4 etc. When this schematic, based on inaccurate long channel model, is implemented on simulators, it is seen that the simulation results do not match with mathematical expectations, with most common outcome being devices coming out of saturation. It may be mentioned that this error is primarily due to use of oversimplified long channel model model to predict the sizes of short channel devices. The designer now adopts an ad-hoc mechanism, adjusts the device dimensions and attempts to bring all transistors in saturation to ensure that the circuit operates in desired operating condition and meet the desired response from the circuit. The difference in predicted and final design variables can be reduced if complex models like BSIM etc. are used while carrying out the design analytically. To handle such complex equations, the designer seeks help of an add-on simulator, optimizer or programming method [10, 11, 12, 13], which requires additional skill and expertise to handle the additional tool along with the the primary simulator. Whatever may be the approach, the net time to design any analog block increases, specially for circuits with short channel devices. Moreover, such methods increase the design complexity and makes the task difficult for novice designers. Some alternate methods for transistor sizing which are less dependent on analytical models have also been proposed [14, 15, 16].

Potential Distribution Method (PDM) [17, 18, 19, 20] is a technology independent approach which is free from complex device equations and can be applied to all kind of devices, both long and short chan-

nel. Simple and basic equations governing the voltage and current levels in the circuit are required to be known by the designer. Presently, design of electronic circuits involve extensive use of simulation tools. Employing such tools in the design process will make the design time shorter and even novice designers can design any analog block including opamps with reasonably good performance and within short time. For designing a block, PDM directly utilizes a simulator as a device sizing tool for finding the device dimensions. PDM also enables us to fine tune the block's response to meet the target specifications. Since the simulator is capable of using accurate device models like BSIM3,4 etc, the results obtained by this method (primarily W/L) is quite reliable and is expected to generate same current and voltage in the circuit for which it has been designed.. While designing a CMOS opamp, the designer often finds it difficult to keep the transistors in saturation. This problem becomes even more serious when cascode structures are being designed. It is to be mentioned that PDM inherently eliminates this problem and provides the sizes of the devices based on the saturation condition. PDM guarantees that all transistors based on predefined bias point would remain in saturation.

In the following sections, the principles of PDM is illustrated and application of PDM in designing a fully differential folded cascode opamp using UMC 180 $\mathrm{nm}$ CMOS technology is demonstrated. The guidelines for fine tuning the performance is also discussed. The tuning guidelines established for a given channel length and process technology holds true for other lengths and technologies as well.

# 2 Principles of Potential Distribution Method

In analog circuits, the DC operating points play an important role in deciding the response of the circuit. The first task of PDM is to stabilize these DC operating points. Once the DC bias points are stabilized with devices in their desired region of operation, the bias conditions are fine tuned to meet the target specifications. In PDM, the simulator is used to find the device dimensions at a pre-defined bias which are based on MOS saturation condition. This is to ensure that all transistors are in saturation even during the first DC simulation. The process of PDM comprises of the following steps.

## 2.1 Initial Bias Conditions

In general, the specifications of an analog circuit are given in terms of DC, AC and transient response. This can be met only when the circuit is biased at a desired operating point. Deciding the initial bias conditions for individual transistors is the first step in PDM.

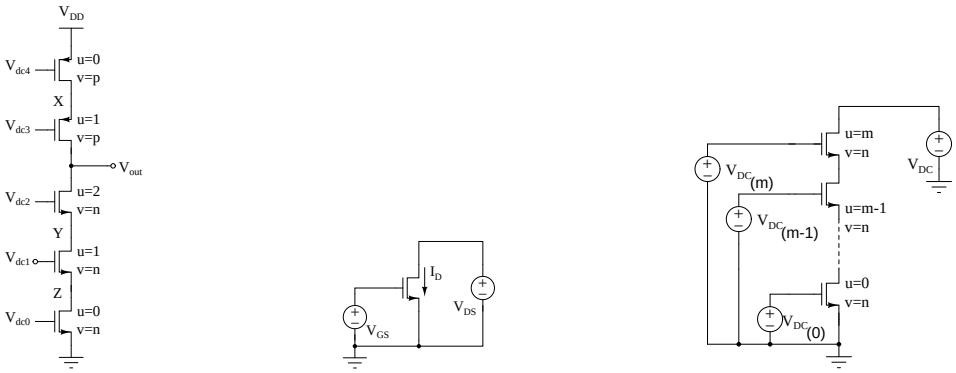
1. PDM starts by first choosing a schematic. For illustration, a cascoded transistor chain as shown in Fig. 1(a) is assumed. The process technology sets the supply level and the minimum channel length of devices. To achieve better matching and higher output impedance, in a typical CMOS analog circuit, the length of all transistors are set to 2 to 3 times the minimum channel length [21]. As per application and accuracy requirement, a suitable simulator is chosen. State-of-the-art simulators typically use highly complex and accurate device models like BSIM3, 4 etc.

2. For ease of illustration, all transistors are assigned a $u$ and $v$ value. Where $u$ is the number of transistors between the chosen device and the supply rail ($GND$ for NMOS and $\mathrm{V}_{DD}$ for PMOS), and $v$ denotes whether the device is of type NMOS or PMOS and takes notation $n$ or $p$ respectively. Assignment of $u$ and $v$ is also shown in Fig. 1(a).

3. Starting from slew rate, power dissipation and unity gain frequency (UGF) requirements, the drain current of all the transistors are estimated. Care is taken that total current does not exceed the maximum power dissipation constraint.

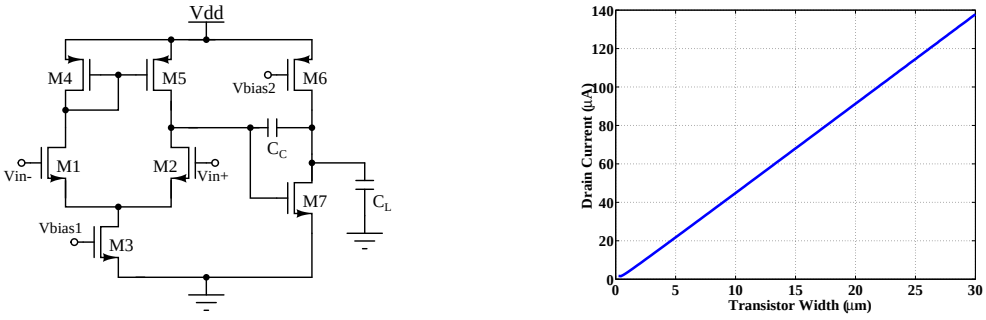
4. The nodes along the drain-source path are labeled in the schematic shown as X, Y, Z, etc. in Fig. 1(a). Nodes which are kept at known potentials like common mode level are identified. For instance, in a single supply circuit, the input and output terminals are typically kept at a common mode level of $\mathrm{V}_{CM} = \mathrm{V}_{DD}/2$.

5. Node voltage distribution is typically started from the output node, first distributed along the drain source path of the output transistors, and then the gate biases are allocated. If the input to the circuit lies on a different branch, the next branch closer to the input is taken up. Again, first drain source and then gate biases are allocated. Typically, none of the transistors in the output side have a predefined gate bias. Thus, the designer has a liberty to arbitrarily set gate bias based on some overdrive condition. For instance, consider the two stage opamp shown in Fig. 2(a). Since the output branch (transistors M6 and M7) and input branch (transistors M1 to M5) are different, we first carry out voltage




(a) (b) (c)

Figure 1: (a) Cadcoded structure (b) Sizing transistor with $u = 0$ (c) Sizing transistor with $u = m$




(a) (b)

Figure 2: (a) A typical two stage opamp (b) Plot of width versus drain current for UMC 180 $\mathrm{nm}$ NMOS at predefined bias conditions with L=500 $\mathrm{nm}$

distribution at the output. Once done, we move towards the input branch. If the input and output lie on the same branch (single stage differential amplifier), we simply start voltage distribution about the differential pair maintaining suitable overdrive. This principle remains valid for other topologies as well. Voltage distribution along drain source path is usually achieved by simply distributing the voltages evenly across the transistors and about the known node potentials. If any other branched path exists (like in folded cascode amplifier or multistage architectures), voltage distribution is carried out on those paths after distributing voltages in the output branch. Voltages set at nodes closer to the output is taken as reference for distributing voltages on branches closer to the input. It is to be mentioned, that usually the input common mode of an amplifier is predefined. Thus, the gate bias of amplifying transistor is fixed and the designer thus has limited liberty while assigning node voltages at the source terminal of the input transistors.

6. In a cascoded structure, leaving the top and bottom transistors, all other transistors are affected by body bias. For threshold voltage estimation of these transistors, a plot of body bias versus threshold voltage ($|\mathrm{V}_{SB}|$ Vs. $|\mathrm{V}_{TH}|$) for NMOS and PMOS is generated for the chosen technology using the simulator. For the resulting body bias of each transistor, the ($|\mathrm{V}_{SB}|$ Vs. $|\mathrm{V}_{TH}|$) plot is referred and the threshold voltage of all transistors are estimated.

7. As per the threshold voltage of individual transistors, the gate drives are allocated. For analog design, the gate overdrive ($\mathrm{V}_{ov}$) is usually set from 5% to 10% of $\mathrm{V}_{DD}$ [21, 22]. As a starting point, gate voltage is chosen such that the overdrive is small (at around 5% of $V_{DD}$). This allows adequate inversion with large transconductance ($\mathrm{g}_m$) and output impedance ($\mathrm{r}_o$). This also provides large input common mode range (ICMR) and output swing. A complete database of all transistors and their operating points ($\mathrm{V}_D$, $\mathrm{V}_G$, $\mathrm{V}_S$, $\mathrm{V}_B$, $\mathrm{I}_D$) is created.

8. Before the transistor sizing is begun, it is ensured that all transistors are on and are biased in saturation region. If not, then drain to source voltage allocation of the transistor in triode is increased. Other node voltages and threshold voltages are recalculated and gate biases are adjusted accordingly. It may be mentioned that if uniform voltage distribution does not allow transistor to be in saturation, then voltage distribution has to be adjusted logically so that saturation condition is satisfied. When voltages across all transistors satisfy the saturation criterion, transistor sizing is carried out.

### 2.2 Transistor Sizing

The transistor sizing procedure is as discussed below:

1. For sizing a branch, transistors with $u = 0$ is selected as the starting point. The predefined terminal voltages are applied, and using the simulator the width of the device is found which sets the desired drain current. A sample circuit for a transistor with $u = 0$ and $v = n$ is shown in Fig. 1(b). A similar circuit may be considered for $u = 0$ and $v = p$. The simulator is used to sweep the width of the device and plot the corresponding drain current. From the graph, the width of the device which sets the desired current at the predefined bias condition is selected. One such graph generated for an NMOS with length L=500 $\mathrm{nm}$ using UMC 180 $\mathrm{nm}$ technology is shown in Fig. 2(b). Next, transistors with $u = 1$ is targeted and transistor with $u = 0$ of the same type is included in its sizing schematic. A similar plot is generated and width of transistor with $u = 1$ is selected.

2. Generalizing the sizing algorithm, to find the width of a transistor with $u = m$, we draw a schematic comprising of transistors with $u = m,\ m-1,\ ...,\ 0$, of either $v = n$ or $v = p$, and connect them as in original schematic. Along with all gate potentials, only the end terminal voltages are applied, i.e., for transistor with $u = m$, topmost drain voltage and bottom-most source voltage is applied if $v = n$ (NMOS), or topmost source voltage and bottom-most drain voltage if $v = p$ (PMOS). The intermediate drain-source nodes need not be biased since their potentials are generated by transistors with $u = m-1,\ m-2,\ ...,\ 0$ which are already sized before sizing transistor with $u = m$. A sample schematic to estimate the size of transistor with $u = m$ is shown in Fig. 1(c). The current through the branch is plotted by varying the width of the transistor with $u = m$. From this, the width of the transistor with $u = m$ is selected. Thus all transistors in a branch are sized to carry the same current at a predefined operating point.

3. Once all the transistor dimensions are known and fed into the simulator, the entire circuit is simulated for DC operating points. It would be seen that the transistors are carrying the desired drain current and all the nodes have achieved the predefined voltage levels. If initial node potentials are selected based on saturation condition, all transistors would be in saturation.

The first task of stabilizing the DC operating point is now complete and the circuit is checked for AC response. PDM allows us to fine tune the opamps AC response by varying the dc operating points and meet the target specifications.

### 2.3 Performance Tuning

As mentioned earlier, in any analog circuit, the DC node voltages play a significant role in deciding its response. The performance parameters of the circuit can thus be tuned by altering the operating points. To achieve this, the voltage and current distribution are altered and new device dimensions are found. It is to be mentioned that different circuits would exhibit different tuning techniques. Thus, for a given circuit, tuning mechanisms are to be established once, which would be valid for all technologies. In this work, the guidelines for tuning the performance of a fully differential folded cascode amplifier are illustrated and discussed.

A flowchart briefly explaining the principle and process of PDM is shown in Fig. 3. Application of PDM for designing a fully differential folded cascode opamp is addressed in the next section.

## 3 Design of A Fully Differential Folded Cascode Opamp

A fully differential folded cascode opamp is shown in Fig. 4 with nodes labeled as A, B, C, etc. Let $\mathrm{V}_X$ denote the DC voltage at node *X* where *X* may take values such as A, B, C etc. Node X and X′ are image potentials and $\mathrm{V}_X$=$\mathrm{V}_{X'}$. Let $\mathrm{V}_{DS(MY)}$ and $\mathrm{V}_{GS(MY)}$ denote the DC level of drain to source and gate to source voltages of transistor *MY* where *Y* may take values 1, 2, 3... and *MY* represents the transistor as labeled in Fig. 4. Also, let $\mathrm{I}_{(MY)}$ denote the DC level of

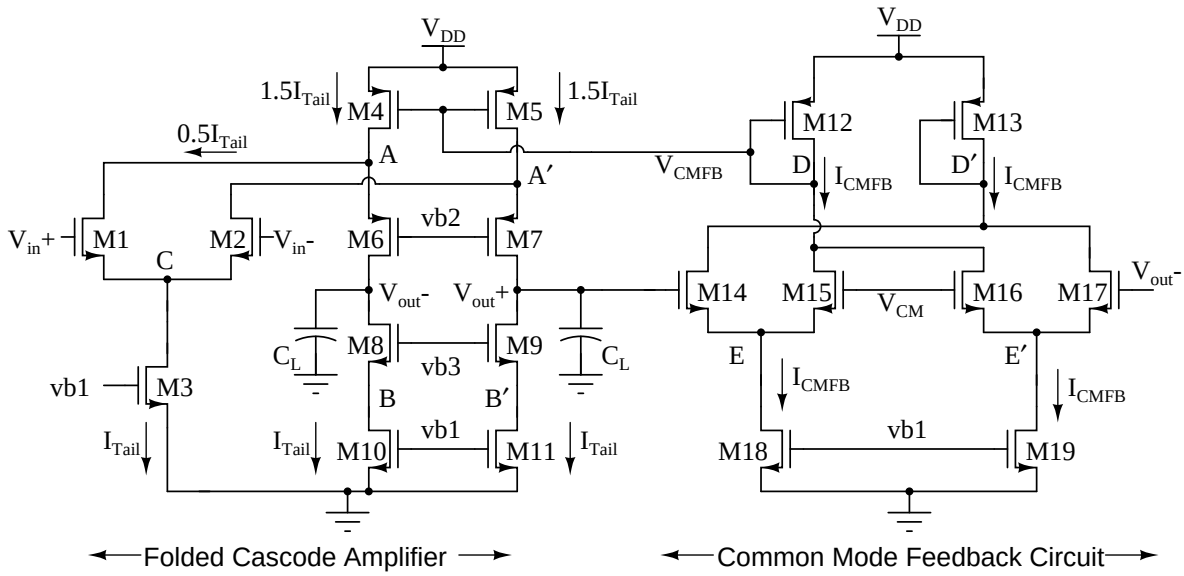



Figure 4: Fully Differential Folded Cascode Amplifier with Common Mode Feedback Circuit

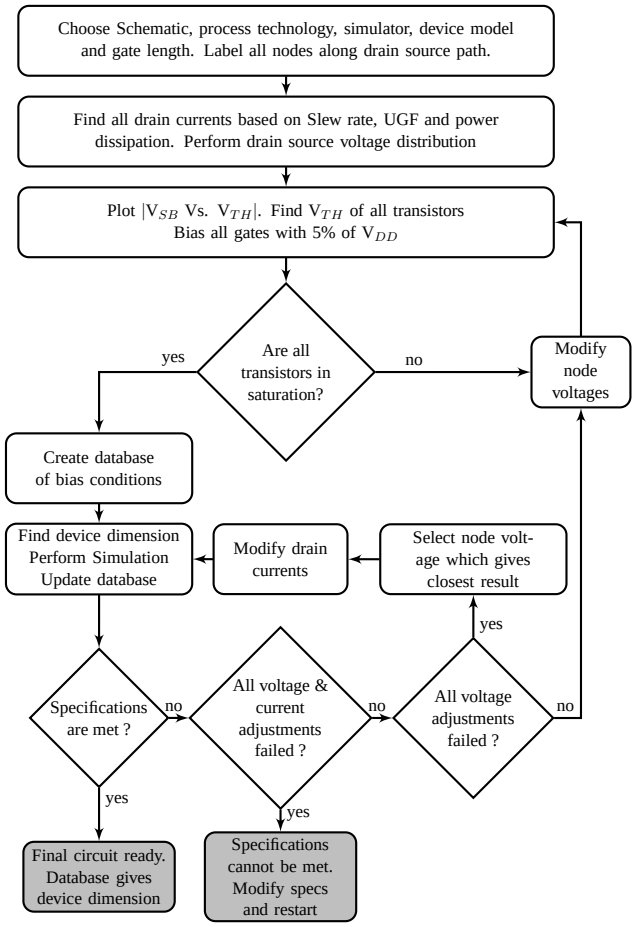



Figure 3: Flowchart depicting principles and process of PDM

drain current of transistor labeled as *MY*. Other voltages are also DC voltages unless explicitly mentioned. Table 1 lists the desired response of the amplifier.

Table 1: Desired response of the amplifier

| |
|---|
| DC Gain $\geq 55$ dB |
| Bandwidth $\geq 200$ kHz |
| Unity Gain Frequency (UGF) $\geq 150$ MHz |
| Phase Margin (PM) $\geq 60^{\circ}$ |
| ICMR$^{-} \leq 600$ mV |
| ICMR$^{+} \geq 1.8$ V |
| Output Swing$^{-} \leq 200$ mV |
| Output Swing$^{+} \geq 1.6$ V |
| Slew Rate (SR) $\geq 100$ V/$\mu$s |
| $C_L = 100$ fF |
| Max. Power Dissipation (P$_{d,max}$) $\leq 250$ $\mu$W |

In PDM, the first version of the opamp is designed without caring much about its response. Once a schematic with all transistors in saturation is ready, the bias conditions are altered, devices are re-sized and target specifications are met. For 180 nm CMOS process, $V_{DD} = 1.8$ V, $V_{SS} = 0$ V $=$ GND is used with L=500 nm (2 to 3 times minimum length [1, 7]). However, it should be noted that the designer is free to choose any length as this does not impose any problem with PDM.

### 3.1 Initial Bias Conditions

The initial bias conditions of the opamp is decided by the steps mentioned below.

### 3.1.1 Current Constraint

As per the maximum power dissipation ($P_{d,max}$), the maximum current ($I_{max}$) drawn from the supply is given by:

$$I_{max} = \frac{\text{Maximum Power Dissipation } (P_{d,max})}{\text{Supply Level } (V_{DD})} \quad (1)$$

Assuming a maximum power dissipation of 250 μW, the maximum allowable current becomes approximately 135 μA at 1.8 V supply. For safe boundaries, $I_{max}$=120 μA is assumed.

As per [22], if SR denotes the slew rate requirement and $C_L$ is the load capacitance, the minimum tail current necessary to meet the slew rate requirement ($I_{Tail,min1}$) of the fully differential folded cascode amplifier is given by:

$$I_{Tail,min1} = 2 \times \text{SR} \times C_L \quad (2)$$

Assuming a slew rate requirement of 100 $\text{V}/\mu\text{s}$, a tail current of 20 μA is required when $C_L$=100 fF.

Besides slew rate, the lower limit on tail current is also dependent on the UGF requirements. The UGF of the amplifier is given by:

$$\text{UGF} = \frac{g_{m(M1,M2)}}{C_L} \quad (3)$$

If $I_{Tail,min2}$ denotes the minimum tail current from UGF constraints, the $g_m$ of differential pair can be given by:

$$g_{m(M1,M2)} = \frac{2 \times \text{Drain Current}}{\text{Overdrive}} = \frac{I_{Tail,min2}}{5\% \text{ of } V_{DD}} \quad (4)$$

The reason for selecting this overdrive is illustrated earlier and is also given in 3.1.2. Now, combining (3) and (4) we get

$$I_{Tail,min2} = \text{UGF} \times C_L \times 5\% \text{ of } V_{DD} \quad (5)$$

Assuming a UGF requirement of 150 MHz with a load of 100 fF, the minimum tail current required to satisfy UGF criteria becomes 1.5 μA. The tail current must satify both, (2) and (5) and may be given by:

$$I_{Tail,min} = \max(I_{Tail,min1}, I_{Tail,min2}) = 20 \ \mu\text{A} \quad (6)$$

Generally, in a folded cascode opamp, it is assumed that transistor M4 carries a current larger than $I_{Tail}$. This prevents the cascoded load current from becoming zero when opamp is slewing [7]. Typically, current through M4 is $1.5I_{Tail}$ [22]. Thus, as a starting condition,

$$I_{(M4)} = 1.5 \ I_{Tail} \quad (7)$$

Numerically,

$$I_{Tail} = 20 \ \mu\text{A} \ ; \ I_{(M4)} = 30 \ \mu\text{A} \quad (8)$$

For the common mode feedback (CMFB) circuit shown in Fig. 4, the CMFB loop gain is given by [22]

$$A_{CMFB} = \frac{I_{(M4)}}{I_{CMFB}} \quad (9)$$

where $I_{CMFB}$ is the current drawn by each diode connected PMOS (M12 and M13) in CMFB circuit as shown in Fig. 4. The designer is free to choose a CMFB loop gain as per his requirement. This does not pose any problem with PDM. Here, assuming a CMFB loop gain of two,

$$I_{CMFB} = \frac{I_{(M4)}}{2} = 15 \ \mu\text{A} \quad (10)$$

Referring Fig. 4, the total current drawn by the opamp may be expressed as

$$I_{Total} = 2I_{(M4)} + 2I_{CMFB} \quad (11)$$

Combining (10) and (11),

$$I_{Total} = 3I_{(M4)} = 90 \ \mu\text{A} \quad (12)$$

It should be ensured that $I_{Total} < I_{max}$. If not, then $I_{(M4)}$ and (or) $I_{CMFB}$ must be reduced so as to bring $I_{Total}$ below $I_{max}$. However, care should be taken that $I_{(M4)} > I_{Tail}$ due to the reason discussed earlier.

### 3.1.2 Node Voltage Distribution

While deciding the initial bias conditions of the transistors, minimum values of overdrive and drain to source drop is decided first. Literature suggests that 5 to 10 % of $V_{DD}$ as overdrive is suitable for analog circuits. This gives large $g_m$ and $r_o$. The overdrive of all transistors are thus initially kept low at around 5% of $V_{DD}$. If $V_{ov}$ represents the overdrive voltage, then

$$V_{GS} - V_{TH} = V_{ov} \approx 5\% \text{ of } V_{DD} \quad (13)$$

It is known that for biasing transistors in saturation region, the drain to source drop should be larger than its overdrive. For safe operation, drain to source drop is kept around 5% of $V_{DD}$ above overdrive. Thus, the minimum drain to source drop becomes:

$$V_{DSmin} \approx 10\% \text{ of } V_{DD} \quad (14)$$

Voltage distribution begins by first identifying the nodes which are to be kept at fixed DC level. For instance, in a single supply circuit, the input and output nodes are typically kept at common mode level

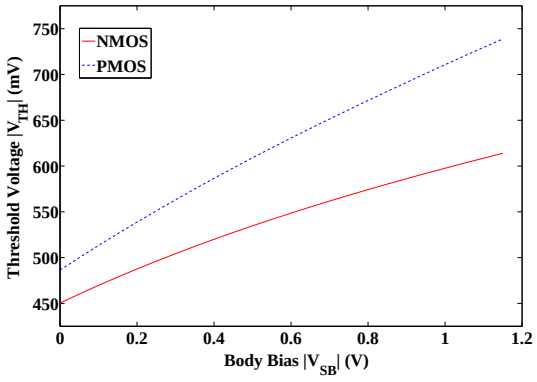



Figure 5: Effect of body bias for UMC 180 nm process with L = 500 nm

of $V_{DD}/2$ (0.9 V in this case). This allows maximum space for input and output voltage swing on both sides of common mode level. In CMFB circuit, gate terminal of transistors M15 and M16 are also kept at common mode level, which is 0.9 V.

Node voltage distribution is now begun from the output side. It can be seen that transistors M4 through M11 constitute the output branch. Voltages at node A and B are thus allocated first. The potential at node A ($V_A$) is taken as the arithmetic mean of known potentials above and below it. Potential at node B ($V_B$) is also set similarly. This causes uniform and even voltage distribution among transistors M4 to M11. Therefore, node A is kept at 1.35 V and node B at 0.45 V.

$$V_A = mean(V_{DD}, V_{out}) = \frac{1.8\text{ V} + 0.9\text{ V}}{2} = 1.35\text{ V} \quad (15)$$

$$V_B = mean(V_{out}, GND) = \frac{0.9\text{ V} + 0\text{ V}}{2} = 0.45\text{ V} \quad (16)$$

After distributing voltages in the output branch, the input branch is taken up. Using the principle of uniform voltage distribution, the potential at node C ($V_C$) can be given by

$$V_C = mean(V_A, GND) = \frac{1.35\text{ V} + 0\text{ V}}{2} = 0.675\text{ V} \quad (17)$$

As mentioned earlier, the gate of the differential pair is at 0.9 V. This allows only 0.225 V of gate to source voltage for differential pair. Moreover, referring to Fig. 5, the approximate threshold voltage for differential pair with body bias of 0.675 V would be around 0.55 V. This bring the overdrive to -0.325 V. It may thus be concluded that if $V_C$ is found using (17), the overdrive of differential pair goes below its effective threshold voltage and it enters sub-threshold region. This creates a need to logically set the potential at node C.

The NMOS differential pair experiences a body bias of $V_C$, due to which its threshold voltage increases and can be read from Fig. 5. The gate to source voltage is ($V_{CM} - V_C$). To keep them on, care should be taken that this gate to source drive is greater than its effective threshold voltage. As $V_C$ increases, the overdrive of the differential pair decreases due to decrease in its gate to source voltage and increase in its effective threshold voltage. A smaller overdrive is particularly of interest since it leads to large transconductance of the amplifier. Thus, the largest value of $V_C$ is that voltage which establishes an overdrive of differential pair of atleast 5% of $V_{DD}$ under the influence of body bias of $V_C$. Mathematically,

$$V_{C,max} = V_{CM} - V_{TH(M1)} + 0.05V_{DD} \quad (18)$$

where, $V_{TH(M1)}$ is threshold voltage of differential pair when $V_{SB(M1)} = V_{C,max}$. Since $V_C$ accounts for drain-source drop of transistor M3, the lower limit of $V_C$ becomes

$$V_{C,min} = V_{DSmin} \approx 10\% \text{ of } V_{DD} \approx 0.2\text{ V} \quad (19)$$

For 180 nm technology with 1.8 V supply, it is seen that $V_C = 0.35$ V is the largest allowable potential at node C with $V_{CM} = 0.9$ V. Beyond this, the differential pair enters sub-threshold region. Thus (19) gives the lower limit on $V_C$ and subjected to the condition that (18) holds true for the upper limit. Thus,

$$V_C = V_{C,max} = 0.35\text{ V} \quad (20)$$

If the designer chooses to have a cascode current sink instead of one transistor (M3), $V_C$ is then distributed equally along the drain source of the two sink transistors.

In the CMFB circuit, M12 and M13 are diode connected transistors which generate the feedback voltage. For 5% overdrive of PMOS transistors M4 and M5, the feedback voltage is initially biased at 1.2 V. Thus,

$$V_D = V_{CMFB} = 1.2\text{ V} \quad (21)$$

For ease of design, node E is kept at the same potential as node C in the folded cascode structure. Also transistors M18 and M19 share the same gate bias as transistor M3.

$$V_E = 0.35\text{ V} \quad (22)$$

Table 2: Node Potentials at Initial Design

| Node | Potential (V) | Node | Potential (V) |
|---|---|---|---|
| A, A′ | 1.35 | B, B′ | 0.45 |
| C | 0.35 | D, D′ | 1.2 |
| E, E′ | 0.35 | vb1 | 0.55 |
| vb2 | 0.625 | vb3 | 1.075 |
| $V_{in}+$, $V_{in}-$ | 0.90 | $V_{CM}$ | 0.9 |
| $V_{out}+$, $V_{out}-$ | 0.90 | $V_{CMFB}$ | 1.2 |

Table 3: Bias Conditions at initial design

| Transistor | $V_D$ (V) | $V_G$ (V) | $V_S$ (V) | $V_B$ (V) | $I_D$ (μA) |
|---|---|---|---|---|---|
| M1, M2 | 1.35 | 0.9 | 0.35 | 0 | 10 |
| M3 | 0.35 | 0.55 | 0 | 0 | 20 |
| M4, M5 | 1.35 | 1.2 | 1.8 | 1.8 | 30 |
| M6, M7 | 0.9 | 0.625 | 1.35 | 1.8 | 20 |
| M8, M9 | 0.9 | 1.075 | 0.45 | 0 | 20 |
| M10, M11 | 0.45 | 0.55 | 0 | 0 | 20 |
| M12, M13 | 1.2 | 1.2 | 1.8 | 1.8 | 15 |
| M14 - M17 | 1.2 | 0.9 | 0.35 | 0 | 7.5 |
| M18, M19 | 0.35 | 0.55 | 0 | 0 | 15 |

#### 3.1.3 Gate Bias

Once the internal node potentials are allocated, the threshold voltage of the transistors are read from Fig. 5 for their corresponding body bias. As per these threshold voltages, gate biases are allotted in accordance to (13). Primarily, there are four basic reasons for selection of small overdrive: large DC gain, large output resistance, wide ICMR and wide output swing.

The voltage gain of the folded cascode amplifier is $g_{m(M1,M2)}R_{out}$, where $R_{out}$ is the effective resistance at the output node. Setting a small overdrive results to large values of both, $g_m$ and $R_{out}$, thereby leading to a large DC gain. At the same time, smaller overdrive leads to smaller $V_{DSsat}$ of transistors, which in turn gives wider ICMR and output swing, but at the cost of larger device and increased parasitic capacitance.

Table 2 lists the initial node voltages of the circuit. A simple algorithm as given in Algorithm 1 could be followed to obtain the DC operating points of any transistor stack like the one showed in Fig. 1(a).

**Algorithm 1** Calculation of DC operating points

$n_n \leftarrow$ No. of NMOS transistors in stack
$V_{top,n} \leftarrow$ Drain potential of top-most NMOS transistor
$V_{bottom,n} \leftarrow$ Source potential of bottom-most NMOS transistor
**for** $u = 0$ **to** $(n_n - 1)$ **do**
  $V_{S,n}[u] \leftarrow [u \times (V_{top,n} - V_{bottom,n})] / n_n$
  $V_{D,n}[u] \leftarrow [(u+1) \times (V_{top,n} - V_{bottom,n})] / n_n$
  $V_{B,n}[u] \leftarrow 0$
  $V_{TH,n}[u] \leftarrow \text{threshold}_n(V_{S,n}[u])$
  $V_{G,n}[u] \leftarrow V_{S,n}[u] + V_{TH,n}[u] + 0.05V_{DD}$
**end for**
$n_p \leftarrow$ No. of PMOS transistors in stack
$V_{top,p} \leftarrow$ Source potential of top-most PMOS transistor
$V_{bottom,p} \leftarrow$ Drain potential of bottom-most PMOS transistor
**for** $u = 0$ **to** $(n_p - 1)$ **do**
  $V_{S,p}[u] \leftarrow V_{DD} - [u \times (V_{top,p} - V_{bottom,p})] / n_p$
  $V_{D,p}[u] \leftarrow V_{DD} - [(u+1) \times (V_{top,p} - V_{bottom,p})] / n_p$
  $V_{B,p}[u] \leftarrow V_{DD}$
  $V_{TH,p}[u] \leftarrow \text{threshold}_p(V_{DD} - V_{S,p}[u])$
  $V_{G,p}[u] \leftarrow V_{S,p}[u] - V_{TH,p}[u] - 0.05V_{DD}$
**end for**

### 3.2 Transistor Sizing

Once the initial bias conditions are finalized, a database is created as shown in Table 3, which lists the terminal voltages and drain current of every transistor. Now, using the method discussed in Section 2.2 and depicted in Fig. 1, the transistor dimensions are found. Usually, the length of the transistors are chosen and the widths are found. The transistor dimensions are then appended into the database.

Once all the device dimensions are known, the complete schematic is simulated. The node potentials as desired are checked after DC simulation. The AC response of the initial design with $C_L$ = 100 fF is given in Table 4. It can be seen that the bandwidth criteria of the amplifier is not met yet. Ahead in this work, method to fine tune the response of the circuit to meet the desired specification is discussed.

### 3.3 Effect of DC Operating Points

It is well known that the response of any amplifier is significantly affected by the DC operating points which represents the potentials at different nodes and the current levels in differential pair and load branch.

Table 4: Initial response of the amplifier

| Performance Parameter | Response for $C_L = 100$ fF |
|---|---|
| DC Gain | 61.93 dB |
| Bandwidth | 147.9 kHz |
| Unity Gain Frequency (UGF) | 171.8 MHz |
| Phase Margin (PM) | 67.29° |
| ICMR$^-$ | 524 mV |
| ICMR$^+$ | 1.87 V |
| Output Swing$^-$ | 180 mV |
| Output Swing$^+$ | 1.62 V |
| $R_{out}$ | 7.26 MΩ |
| Slew Rate | 100 V/μs |
| $I_{Total}$ | 90 μA |
| Power Dissipation | 162 μW |
| Input Referred Noise | 286.4 $\mu V/\sqrt{Hz}$ |
| CMRR | 300.8 dB |
| PSRR (average) | 259.3 dB |
| Dominant Pole ($P_1$) | 151.1 kHz |
| Non-Dominant Pole 1 ($P_2$) | 417.25 MHz |
| Non-Dominant Pole 2 ($P_3$) | 1.519 GHz |
| Pole Zero Dublet | 2.151 GHz |
| FOM$_1$ (MHzpF/mA) | 190.8 |
| FOM$_2$ ((V/μs)pF/mA) | 111.1 |

A detailed study on the effect of bias by varying these node potentials and currents on the response of the amplifier is carried out by varying one parameter while keeping the other conditions constant. The range of node voltage adjustment is set such that all transistors operate in the saturation region with minimum drain-source drop of $V_{DS,min}$. The currents levels should satisfy the slew rate and UGF requirements and at the same time not exceed the maximum allowed power dissipation. Change in DC bias directly affects the $g_m$ and $r_o$ of transistors thus altering the circuit's response. It is shown that by setting these bias conditions appropriately, the target specifications of the opamp can be met. It is to be mentioned that effect of DC operating point is observed by first altering voltage/current distribution, finding new device dimensions using the method given in 2.2 and then checking the response of the complete circuit.

### 3.3.1 Potential at Node A

As $V_A$ (potential at node A marked in Fig. 4) is varied, the threshold voltage of M6-M7 pair vary due to change in their body bias. Thus, vb2 is adjusted for keeping the overdrive constant at 5% of $V_{DD}$. For allowing a drain to source drop of $V_{DS,min}$ for transistors M4 to M7, the possible range of $V_A$ becomes $V_{DS,min}$ above $V_{out}$ to $V_{DS,min}$ below $V_{DD}$. Thus, the range of $V_A$ can be expressed as

$$V_{out} + V_{DS,min(M6)} \leq V_A \leq V_{DD} - V_{DS,min(M4)} \quad (23)$$

Since $V_{out}$ is assumed at 50% of $V_{DD}$, the limits can be expressed as

$$60\% \text{ of } V_{DD} \leq V_A \leq 90\% \text{ of } V_{DD} \quad (24)$$

$V_A$ is thus varied from 1.1 V to 1.6 V for 1.8 V supply. It is observed that potential at node A significantly affects the UGF, DC gain and the bandwidth of the amplifier.

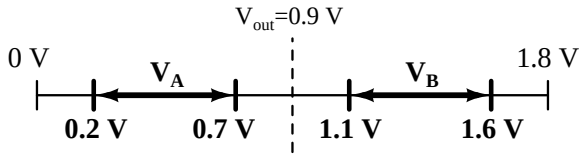



Figure 6: Range of $V_A$ and $V_B$ for UMC 180

### 3.3.2 Potential at Node B

With the change in $V_B$, vb3 must be adjusted to keep overdrive of M8-M9 pair constant. Using the same principle used to decide the range of $V_A$, the possible range for $V_B$ becomes $V_{DS,min}$ above GND to $V_{DS,min}$ below $V_{out}$. Thus, the range of $V_B$ is given by:

$$10\% \text{ of } V_{DD} \leq V_B \leq 40\% \text{ of } V_{DD} \quad (25)$$

$V_B$ is thus varied from 0.2 V to 0.7 V for 1.8 V supply. Similar to $V_A$, $V_B$ is also found to significantly affect the DC gain and the bandwidth of the amplifier. The UGF is independent of the potential at node B. A detailed discussion on their dependency is presented next. The range of $V_A$ and $V_B$ for UMC 180 nm is shown in Fig. 6.

Using the limits set by above equations, the effect of $V_A$ and $V_B$ is illustrated in Fig. 7 to Fig. 12. It is to be noted that the axis labeled *"Potential at node A"* in Fig. 7 and Fig. 12 is reversed to enable clear surface plot view. Fig. 7 shows that the UGF is a function of the potential at node A and is independent of potential at node B. Comparing Fig. 8 and 9 the trade-off between DC gain and bandwidth can be seen. Fig. 10 clearly shows that the phase margin is independent of $V_A$ and $V_B$. The nature of the plot for output resistance is identical to that of voltage gain due to the fact

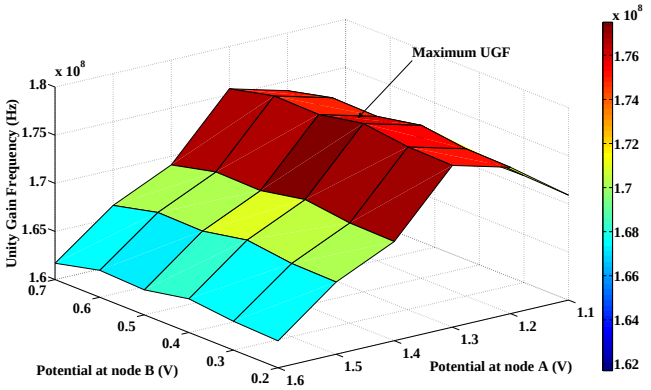



Figure 7: Effect of potential at nodes A and B on unity gain frequency

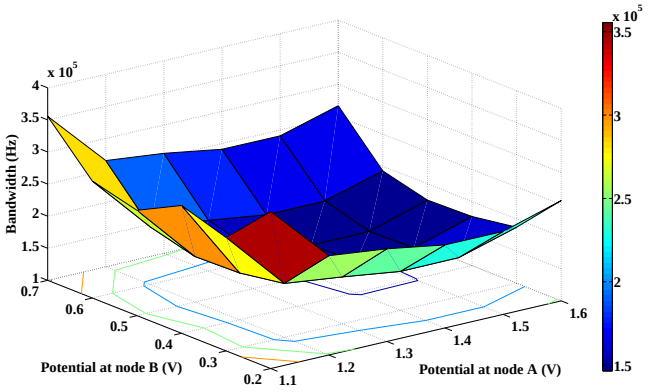



Figure 9: Effect of potential at nodes A and B on 3dB bandwidth

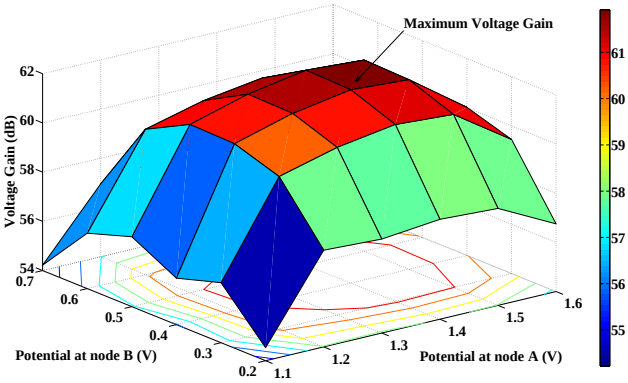



Figure 8: Effect of potential at nodes A and B on voltage gain

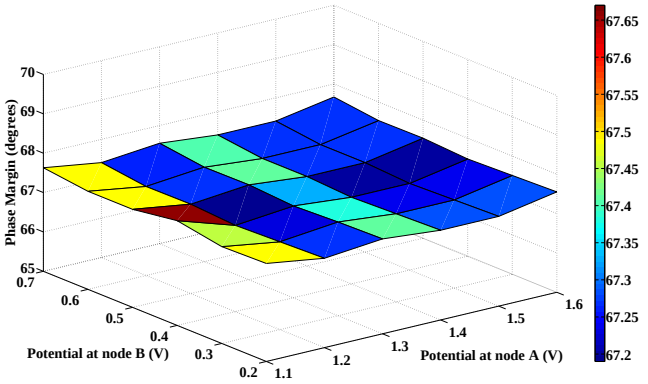



Figure 10: Effect of potential at nodes A and B on phase margin

that $g_m$ of the amplifier is independent of the voltages at node A and B. In this example, output resistance is seen to vary from 3 MΩ to 7 MΩ. The values of $V_A$ and $V_B$ can be read to either maximize $R_{out}$ for large DC gain, minimize $R_{out}$ for large bandwidth or settle for a trade-off. The values $V_A$ and $V_B$ can also be read to achieve given performance parameters. Fig. 11 and 12 shows the dependency of the dominant and non-dominant pole with $V_A$ and $V_B$. The plot for dominant pole and bandwidth are identical with slight level shift. It is also evident that non-dominant pole is independent of potential at node B and takes highest value when node A is at its lowest possible potential. Lowest potential at A allows large drain to source drop for M4-M5 pair leading to their smaller size and hence lower parasitic capacitance.

Table 5 lists the potential at node A and B for maximizing a performance parameter or achieving a trade-off. Table 6 lists the ratio in which drain to source voltages may be distributed to achieve the

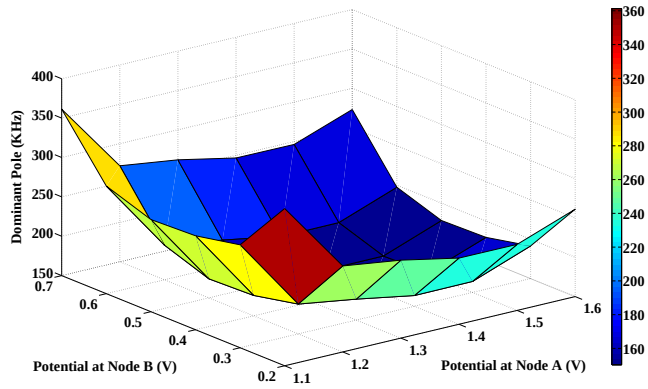



Figure 11: Effect of potential at nodes A and B on Dominant Pole

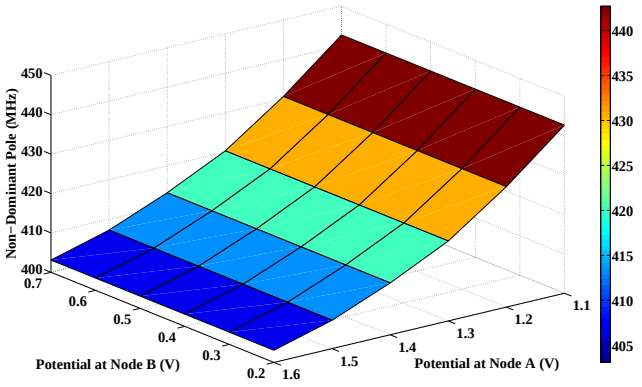



Figure 12: Effect of potential at nodes A and B on non-dominant pole

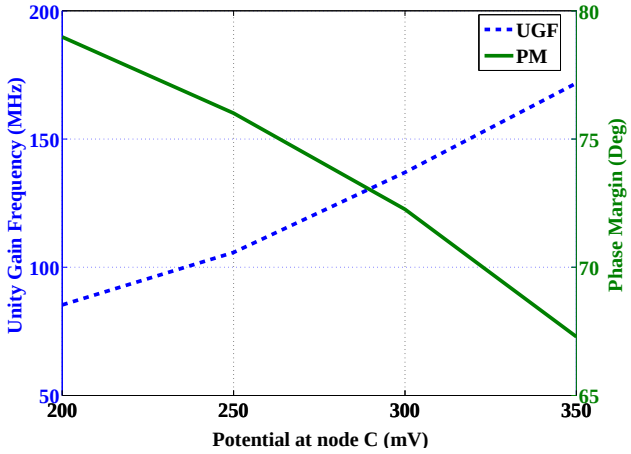



Figure 14: Effect of $V_C$ on unity gain frequency and phase margin

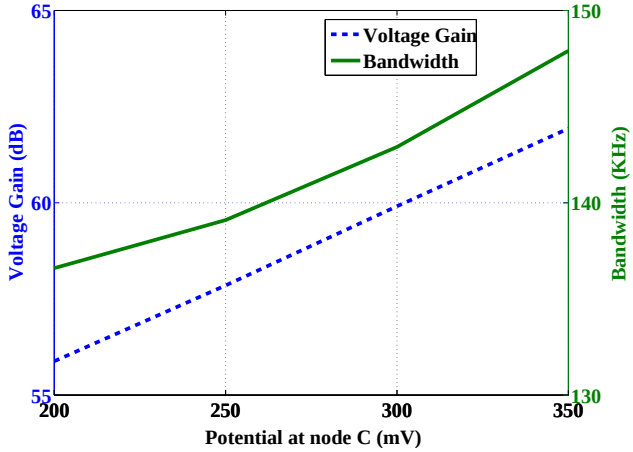



Figure 13: Effect of $V_C$ on voltage gain and bandwidth

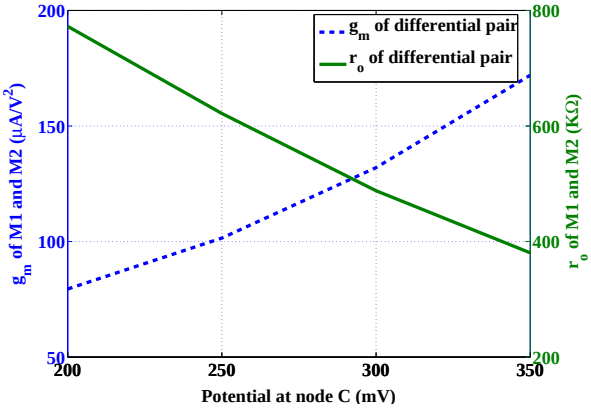



Figure 15: Effect of $V_C$ on $g_m$ and $r_o$ of differential pair M1 and M2

same. It is observed that the bandwidth is maximized when Node A is at lowest possible potential and node B is either at its maximum or minimum possible value.

### 3.3.3 Potential at Node C

The potential at node C is limited on the lower side by $V_{DS,min}$ of transistor M3. As mentioned earlier, for 1.8 V supply, $V_{C,max}$=0.35 V, approximately 20% of $V_{DD}$. Combining this with (14), the limits on $V_C$ can be expressed as

$$10\%\ of\ V_{DD} \leq V_C \leq 20\%\ of\ V_{DD} \qquad (26)$$

The effect of potential at node C on AC response of the opamp is shown in Fig. 13 and 14. It is evident that larger potential at node C fetches larger DC gain, bandwidth and unity gain frequency at the same time, but with little compromise on phase margin. Fig. 15 shows that as the potential at node C is decreased keeping others constant, $r_o$ of differential pair increases. This causes the overall output resistance to increase further. However, with reduction in $V_C$, the transconductance of the amplifier rapidly falls ($g_m \propto 1/(\text{Vin-}V_C)$). This causes a reduction in the overall gain of the amplifier ($A_v = g_m R_{out}$).

### 3.3.4 Selection of Total Current

To examine the effect of total current drawn by the circuit, the total current drawn is varied maintaining the current ratios. In this example, $I_{(M4)} = 1.5I_{Tail}$ and $I_{CMFB}=I_{(M4)}/2$. Combining the conditions given in (7), (10) and (11), the lower limit on total current can be expressed in terms of minimum tail current as

$$I_{Total} \geq 4.5\ I_{Tail,min} \qquad (27)$$

Table 5: Voltage selection of nodes A and B for 1.8 V supply

| $V_A$ (V) | $V_B$ (V) | $V_C$ (V) | Maximized Parameters |
|---|---|---|---|
| 1.35 | 0.45 | 0.35 | DC Gain & $R_{out}$ |
| 1.35 | Independent | 0.35 | UGF |
| 1.1 | 0.7 and 0.2 | 0.35 | Bandwidth & Dominant Pole |
| 1.1 | Independent | 0.35 | Non-Dominant Pole |

Table 6: Drain to Source Voltage Distribution at Nodes A and B keeping $V_C$ = 0.35 V

| $V_{SD(M4)} : V_{SD(M6)}$ | $V_{DS(M8)} : V_{DS(M10)}$ | Maximized Parameters |
|---|---|---|
| 1 : 1 | 1 : 1 | DC Gain & $R_{out}$ |
| 1 : 1 | Independent | UGF |
| 7 : 2 | 7 : 2 or 2 : 7 | Bandwidth & Dominant Pole |
| 7 : 2 | Independent | Non-Dominant Pole |

The upper limit on total current is set by the maximum allowable current. Thus, the range over which the total current can be chosen is given by

$$4.5\ I_{Tail,min} \leq I_{Total} \leq I_{max} \tag{28}$$

For this design, the numerical limits on $I_{Total}$ is

$$90\ \mu A \leq I_{Total} \leq 120\ \mu A \tag{29}$$

The effects of changing total current are shown in Fig. **??** and 18. Fig. 16 suggests that increasing the total current consumed by the opamp increases the UGF significantly, with negligible compromise on the phase margin. Around 30% increase in the total current causes the UGF to increase by around 23%. A 7% compromise on phase margin is also noticed. Fig. 17 however suggests that the DC gain of the opamp is more or less independent of the total current when current ratios are unchanged. An increase in bandwidth is also noticed with increase in total current. From Fig. 18 it may be stated that with the increase in current, the output resistance of the amplifier falls with improvement in transconductance. Their product being constant, the DC gain remains unaffected.

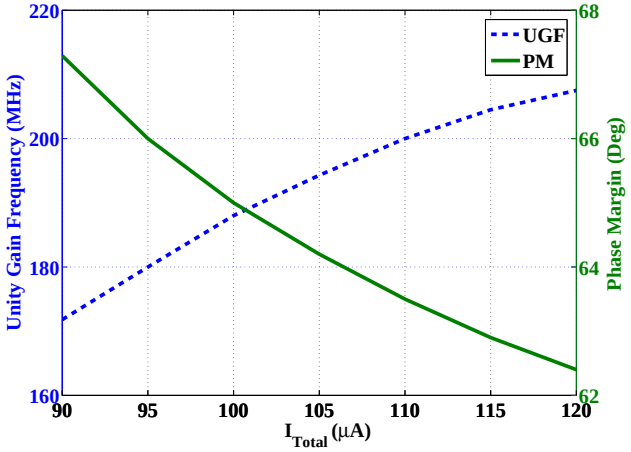



Figure 16: Effect of Changing $I_{Total}$ on unity gain frequency and phase margin

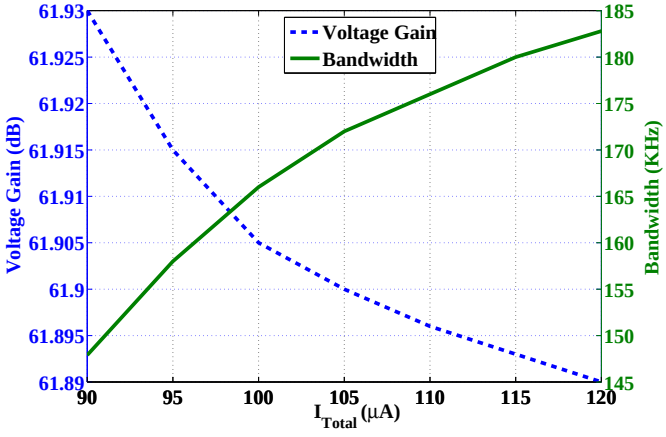



Figure 17: Effect of Changing $I_{Total}$ on voltage gain and bandwidth

### 3.3.5 Selection of Current Through M4

Another scheme for investigating the effect of current on the amplifier's response is to keep the tail current fixed at its minimum level ($I_{Tail,min}$) and vary the current through transistor M4. It should be noted that the current through CMFB transistors also have to be adjusted in order to keep the CMFB loop gain constant.

Combining (10) and (11) the total current drawn by the opamp becomes

$$I_{Total} = 3I_{(M4)} \tag{30}$$

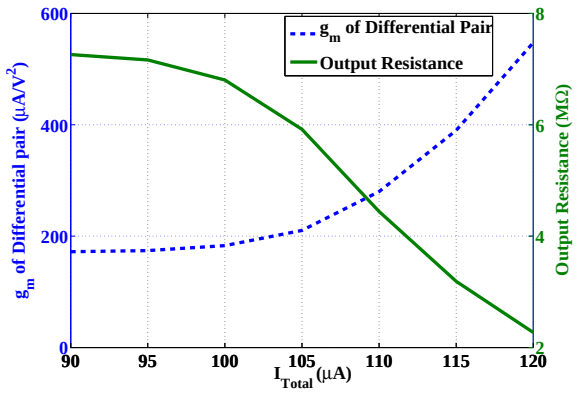



Figure 18: Effect of $I_{Total}$ on $g_{m(M1,M2)}$ and $R_{out}$

When $I_{Total}$ = $I_{max}$, the upper limit on $I_{(M4)}$ is reached.

$$I_{(M4)} \leq \frac{I_{max}}{3} \tag{31}$$

As per [22], the smallest current which should flow through M4 can be expressed in terms of minimum tail current as

$$I_{(M4)} \geq 1.2 I_{Tail,min} \tag{32}$$

Therefore the limits on $I_{(M4)}$ can be summarized as

$$1.2 I_{Tail,min} \leq I_{(M4)} \leq \frac{I_{max}}{3} \tag{33}$$

In this example, with $I_{Tail,min}$ = 20 μA and $I_{max}$ = 120 μA, the numerical limits on $I_{(M4)}$ are

$$24\ \mu A \leq I_{(M4)} \leq 40\ \mu A \tag{34}$$

Fig. 19 shows the effect of changing $I_{(M4)}$ keeping the tail current constant. These graphs may also be seen as portraying the effect of current distribution at node A. Moving left to right on the X-axis of these graphs, cascode load current increase with $I_{Tail}$ fixed. It may be interpreted that a larger fraction of $I_{(M4)}$ diverts into the cascode load as we move left to right on X-axis. Similarly, when we move right to left, the fraction of current flowing into the differential pair increases. It can be concluded that as ratio of current in differential pair to cascode branch increases, the voltage gain and unity gain frequency is improved significantly with compromise on bandwidth and phase margin (PM).

# 4 Performance Tuning

The initial design is carried out by allocating equal drain to source drop across transistors M4 to M11. Node C should be allocated highest possible value for the technology which allows an overdrive of around 5% of $V_{DD}$ for the differential pair. The tail current is set to $I_{Tail,min}$ which satisfies the slew rate and UGF criteria. Current though M4 is set at 1.5 times $I_{Tail}$. All gate biases are allocated such that the overdrive is around 5% of $V_{DD}$. If the initial design does not meet the design specifications, adjustments in node voltages and current have to be carried out. The voltage and current distribution is altered and the devices are re-sized.

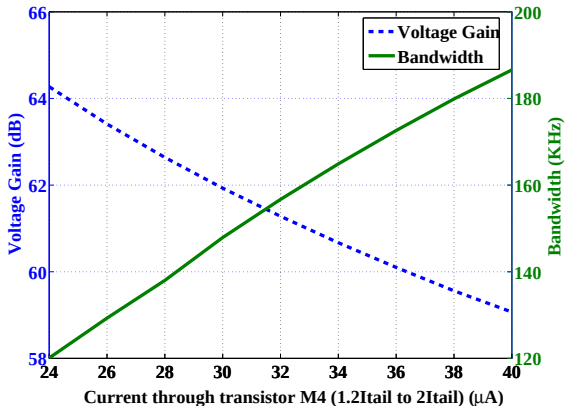
## 4.1 DC Gain and Output Resistance Adjustments

For a given current level, the DC gain is maximized when potentials at node A and B are kept at their mean value, while potential at node C at its maximum possible value which keeps differential pair on. If further increase in DC gain is desired, it may be achieved by increasing the output resistance or amplifier transconductance. At fixed node potentials, output resistance may be increased by reducing the load current keeping tail current fixed ($r_o \propto 1/I_D$). In other words, decreasing $I_{(M4)}$ from $1.5I_{Tail}$ to $1.2I_{Tail}$. This causes significant reduction in power dissipation along with small increase in UGF. Due to reduced current level in the load, transistor widths are reduced. This causes an increase in resistance and decrease in parasitic capacitance, resulting to a simultaneous increase in DC gain ($A_v \propto 1/R_{out}$) and UGF (UGF $\propto 1/C_L$). DC gain however remains constant if the overall current of the opamp is increased proportionally. An increase in transconductance of differential pair can be achieved by either reducing their overdrive (increase $V_C$) or increasing device width (w) by allowing more current in differential pair ($g_m \propto$ W/L ; $g_m \propto 1/V_{ov}$).

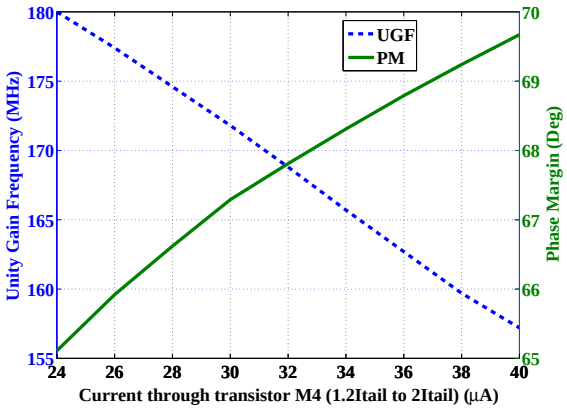
Fine tuning of output resistance can be achieved in a manner similar to that of DC Gain. Voltages at node A and B are kept at their mean values while that of node C is kept at its minimum value. The current levels are also at their minimum level since this supports smaller device width leading to large resistance. The output resistance may also be increased by increasing the lengths of the transistors in the cascode branch. Illustration on device length is presented ahead.

## 4.2 Unity Gain Frequency Adjustments

The mean distribution of potentials at node A with node C at its maximum value, fetches largest UGF for a given current level. UGF is found to be independent of the potential at node B. Current level plays a significant role is deciding the UGF. Diverting a larger




(a)




(b)

Figure 19: Effect of $I_{(M4)}$ on (a) voltage gain and 3dB bandwidth (b) unity gain frequency and phase margin

Table 7: Bias Conditions to Maximize Performance Parameter maintaining $I_{CMFB} = I_{(M4)}/2$ and Overdrive = 5% of $V_{DD}$ for all transistors

| Maximized Parameter | $V_A$ | $V_B$ | $V_C$ | Current Levels |
|---|---|---|---|---|
| DC Gain | mean($V_{DD}$,$V_{out}$) | mean($V_{out}$,GND) | $V_{C,max}$ | $I_{Tail} = I_{Tail,min}$<br>$I_{(M4)} = 1.2\ I_{Tail}$ |
| UGF | mean($V_{DD}$,$V_{out}$) | Independent of $V_B$ | $V_{C,max}$ | $I_{(M4)} = I_{max}/3$<br>$I_{Tail} = I_{(M4)}/1.2$ |
| Bandwidth | $V_{out} + (0.1V_{DD})$ | $0.1V_{DD}$ or<br>$(V_{out} - (0.1V_{DD}))$ | $V_{C,max}$ | $I_{(M4)} = I_{max}/3$<br>$I_{Tail} = I_{(M4)}/2$ |
| Phase Margin | Independent of $V_A$ | Independent of $V_B$ | $V_{C,min}$ | $I_{Tail} = I_{Tail,min}$<br>$I_{(M4)} = 1.2\ I_{Tail}$ |
| Output Resistance | mean($V_{DD}$,$V_{out}$) | mean($V_{out}$,GND) | $V_{C,min}$ | $I_{Tail} = I_{Tail,min}$<br>$I_{(M4)} = 1.2\ I_{Tail}$ |
| Trade-off | mean($V_{DD}$,$V_{out}$) | mean($V_{out}$,GND) | $V_{C,max}$ | $I_{Tail} = I_{Tail,min}$<br>$I_{(M4)} = 1.6\ I_{Tail}$ |

fraction of current from M4 into the differential pair shows an increase in UGF. Increasing the overall current also causes the UGF to increase significantly. It is concluded that UGF can be maximized for a given voltage distribution by allowing the circuit to consume maximum total current and diverting most of the current of M4 into the differential pair. For achieving small increment in UGF, $I_{Tail}$ could be fixed and current through M4 be reduced towards $1.2I_{Tail}$.

### 4.3 Bandwidth and PM Adjustments

Due to opposite dependency on $R_out$, a trade-off between bandwidth and DC gain exists. To increase bandwidth the potential at node B is either increased to decreased from its mean position maintaining all transistors in saturation. This does not affect the UGF since it is independent of $V_B$ (Fig. 7). If this adjustment does not meet the bandwidth requirements, an increase in total current, particularly in the cascode branch, increases bandwidth (Fig. 19(a) and 17).The potential at node C should only be decreased when serious improvement in phase margin is required at the cost of other AC performance parameters. Phase margin can also be improved by increasing $I_{(M4)}$ keeping $I_{Tail}$ constant (Fig. 19(b)).

### 4.4 ICMR and Output Swing Adjustments

The initial design is carried out keeping overdrive at its minimum level. As discussed earlier, this allows maximum ICMR and output swing. If ICMR and output swing results can be relaxed, overdrive of transistors M3, M4, M5, M10 and M11 can be increased. In-

creasing overdrive of M4 and M5 pair should be given higher priority than M6 and M7 pair. This is due to the fact that M4 and M5 pair carry large current and their sizes are usually large. An increase in their overdrive would reduce their dimensions. Similarly, on the negative side, overdrive of M8 and M9 pair is increased first. This causes reduction in their widths and thus in parasitic capacitance at the output node. Although the increased overdrive decreases their $g_m$, parasitic capacitance is reduced due to smaller transistors. Overdrive increase should be such that ICMR and output swing stays within acceptable limits. Moreover, dimension reduction leads to significant area saving.

### 4.5 Achieving Typical Trade-off

Simulation results suggest that a typical trade-off can be achieved when potentials at nodes A and B are kept in their mean positions, node C at its maximum allowable value, tail current at its minimum level and $I_{(M4)}$ at $1.6I_{Tail}$. This leads to an opamp with reasonably good performance with UGF - bandwidth trade-off at moderate power dissipation.

### 4.6 Preferred Method For Performance Tuning

The first attempt to meet target specifications should be by adjusting voltages at nodes A, B and C. Before increasing any current, it should be checked if decreasing $I_{(M4)}$ keeping $I_{Tail}$ meets the target specifications. Only when these two procedures fail to meet the specifications, the current through M4 or overall current may be increased. Increasing the current through transistor M4 increases the power dissipation of the circuit. Thus, any increase in performance parameter should be notably more important and significant than the price paid in terms of increased power dissipation. A suggested flow for designing a fully differential folded cascode amplifier is depicted in Fig. 20.

Table 7 illustrates the node voltages and current levels of a folded cascode opamp for maximizing a performance parameter or settling for a trade-off. It can be noticed that the DC gain and UGF can be maximized at the same time by setting node voltages as per DC gain maximization and current level as per UGF maximization. This is due to two facts observed from the graphs presented earlier. Firstly, node voltage requirement for maximizing DC gain is a special case of maximizing UGF. Secondly, the DC gain of the circuit remains unaffected when currents through the differential pair and load branch is increased proportionally (Fig. 17). This, however, increases the UGF (Fig. 16). Thus, by setting node voltages as per DC gain maximization and increasing current proportionally until maximum power dissipation is reached, both, DC gain and UGF are maximized at the same time. Similar observation can also be made to maximize phase margin and output resistance at the same time.

## 5 Channel Length Selection Guidelines

The amplifier design presented so far used uniform channel length for all transistors. As mentioned earlier, in PDM, the designer is free for choosing any channel length for any transistor. Some guidelines on channel length selection may be found in literature. Fig. 21(a) and 21(b) show the variation of $g_m$ and $g_m r_o$ with channel length. The graphs shown are plotted for NMOS transistor with L=180 $\mathrm{nm}$. Similar plots can be generated for PMOS transistor. It is clearly observed in Fig. 21(a) that $g_m$ is maximized when channel length is around $1.3L_{min}$. The differential pair may thus be sized using $1.3L_{min}$ to extract high $g_m$ from the amplifier. If an increase in output resistance is desired, the length of the load branch transistors, particularly M6 through M9, can be increased. The product $g_m r_o$ of transistors M6 through M9 play a significant role in deciding the amplifiers output resistance.

Another parameter which is significantly affected by channel length is noise. Simulation results reveal that the main contributors of noise in this topology are the NMOS pairs M10-M11 followed by the differential pair M1-M2. It is seen that M10-M11 pair contribute around 75% to 95% of the total noise. With the increase in overdrive of these transistors, the noise contributions are seen to increase. However, a dip in noise contribution is seen when the length of these transistors are increased. It is thus recommended to keep the overdrive of M10-M11 small at large lengths which leads to reduced noise and improved output impedence and swing at the same time (Noise $\propto$ Overdrive/Length). Tabe 8 shows that as the length of M10-M11 pair is increased, their noise contributions decrease and hence total input referred noise also decreases. It can be seen that upto around $3L_{min}$ the noise contributions reduce significantly. When lengths of M10-M11 pair cross $3L_{min}$, differential pair become a significant noise contributor.

## 6 Achieving Desired Response

Comparing Table 1 with 4, it can be seen that bandwidth is the only parameter which is not met. As per

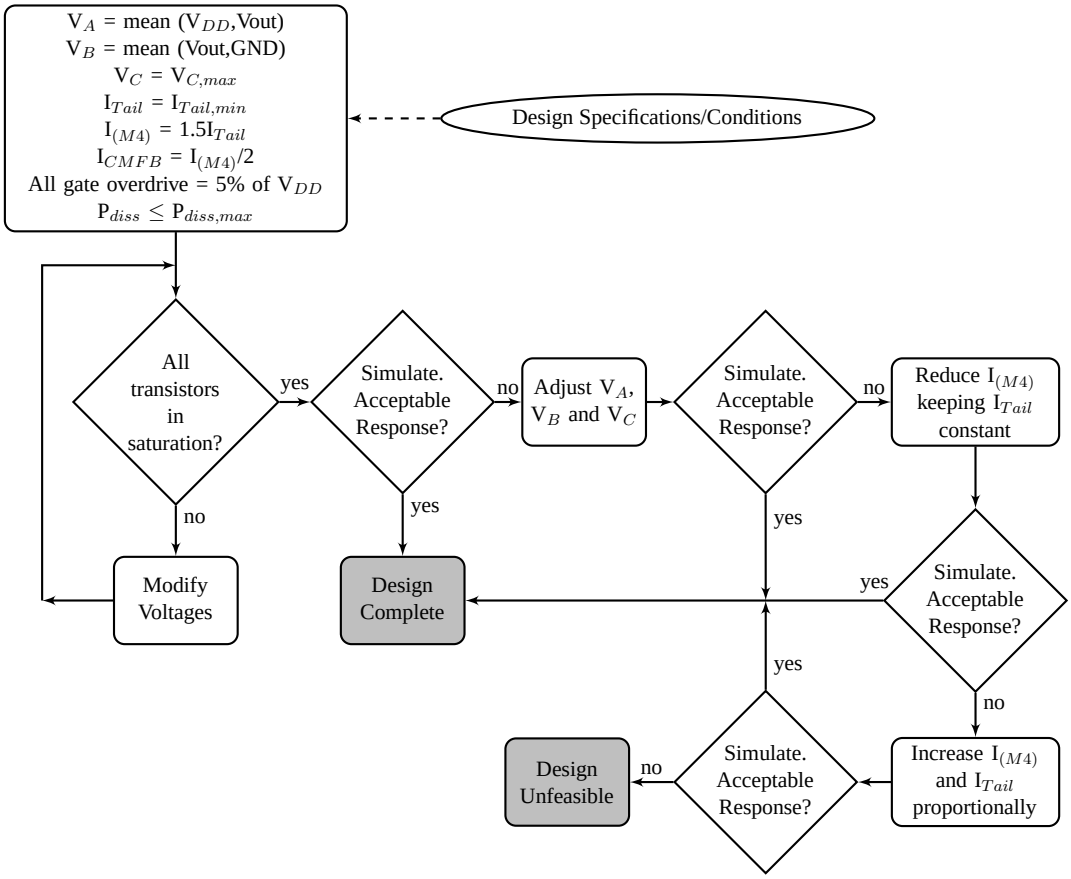
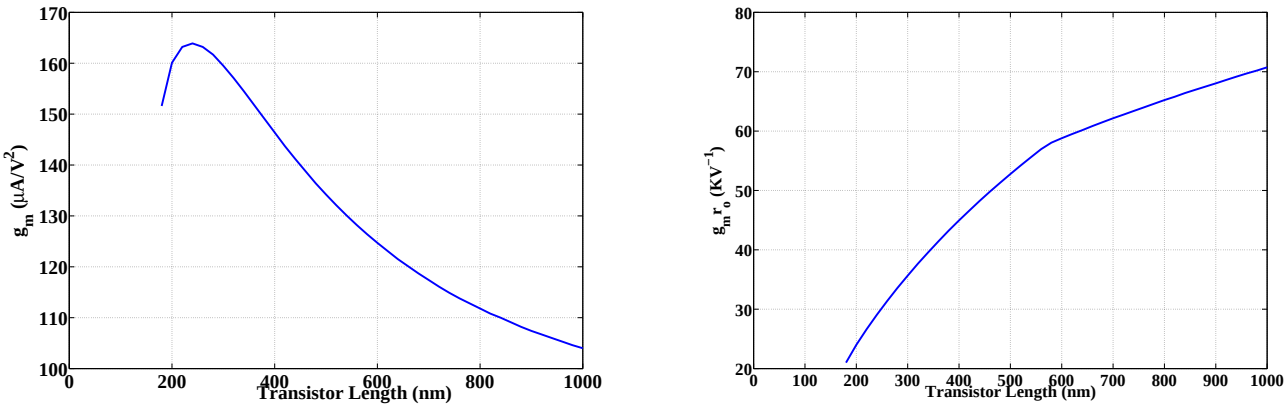



Figure 20: Preferred method for designing a fully differential folded cascode amplifier using Potential Distribution Method




(a) (b)

Figure 21: Effect of channel length on (a) $g_m$ (b) $g_m r_o$ for 180 nm NMOS

Fig. 9, the bandwidth of the amplifier can be increased by moving potentials at node A and B away from their mean position. It is recommended to alter potential at node B since this does not affect the UGF. Also, since sufficient phase margin is noticed, an attempt to lower the current through M4 keeping $I_{Tail}$ constant is considered. Reduction in $I_{(M4)}$ also causes $I_{CMFB}$ to decrease. This leads to valuable power and area saving. The DC bias conditions of the amplifier is thus modified as given in Table 9 and the final specifications achieved is given in Table 10.

It can be seen that all performance parameters of

Table 8: Noise contributions by M10 and M11 at 5% overdrive

| Transistor Length ($\mathrm{nm}$) | Noise Contribution ($\mathrm{mV}$) | Total Input Referred Noise ($\mu\mathrm{V}\sqrt{\mathrm{Hz}}$) |
|---|---|---|
| 180 | 231 | 744 |
| 350 | 119.4 | 343.5 |
| 500 | 83.1 | 286.4 |
| 650 | 62.5 | 270.7 |
| 800 | 48.6 | 265.4 |
| 1000 | 47.6 | 262.8 |

Table 9: Bias Conditions at final design

| Transistor | $V_D$ (V) | $V_G$ (V) | $V_S$ (V) | $V_B$ (V) | $I_D$ ($\mu$A) |
|---|---|---|---|---|---|
| M1, M2 | 1.35 | 0.9 | 0.35 | 0 | 10 |
| M3 | 0.35 | 0.55 | 0 | 0 | 20 |
| M4, M5 | 1.35 | 1.2 | 1.8 | 1.8 | 24 |
| M6, M7 | 0.9 | 0.625 | 1.35 | 1.8 | 14 |
| M8, M9 | 0.9 | 1.075 | 0.45 | 0 | 14 |
| M10, M11 | 0.45 | 0.55 | 0 | 0 | 14 |
| M12, M13 | 1.2 | 1.2 | 1.8 | 1.8 | 12 |
| M14 - M17 | 1.2 | 0.9 | 0.35 | 0 | 6 |
| M18, M19 | 0.35 | 0.55 | 0 | 0 | 12 |

Table 10: Final response of the amplifier

| Performance Parameters | Response for $C_L$=100 fF | | |
|---|---|---|---|
| | Desired | Initial | Final |
| DC Gain ($\mathrm{dB}$) | $\geq 55$ | 61.39 | 65.22 |
| Bandwidth ($\mathrm{kHz}$) | $\geq 200$ | 147.9 | 116.6 |
| UGF ($\mathrm{MHz}$) | $\geq 150$ | 171.8 | 188 |
| Phase Margin ($^\circ$) | $\geq 60$ | 67.29 | 62.09 |
| ICMR$^-$ ($\mathrm{mV}$) | $\leq 600$ | 524 | 524 |
| ICMR$^+$ (V) | $\geq 1.8$ | 1.87 | 1.87 |
| Output Swing$^-$ ($\mathrm{mV}$) | $\leq 200$ | 180 | 180 |
| Output Swing$^+$ (V) | $\geq 1.6$ | 1.62 | 1.62 |
| Slew Rate ($\mathrm{V}/\mu\mathrm{s}$) | $\geq 100$ | 100 | 100 |
| $I_{Total}$ ($\mu$A) | $\leq 135$ | 90 | 72 |
| Power ($\mu$W) | $\leq 250$ | 162 | 129.6 |
| Input Referred Noise ($\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$) | - | 286.4 | 244.6 |
| CMRR ($\mathrm{dB}$) | - | 300.8 | 299 |
| PSRR (average) ($\mathrm{dB}$) | - | 259.3 | 232.8 |
| Dom. Pole ($P_1$) ($\mathrm{kHz}$) | - | 151.1 | 161.1 |
| $P_2$ ($\mathrm{MHz}$) | - | 417.25 | 366.6 |
| $P_3$ ($\mathrm{GHz}$) | - | 1.519 | 1.484 |
| Pole Zero Dublet ($\mathrm{GHz}$) | - | 2.151 | 2.09 |
| $FOM_1$ ($\mathrm{MHzpF/mA}$) | 120 | 190.8 | 261.1 |
| $FOM_2$ (($\mathrm{V}/\mu\mathrm{s}$)pF/mA) | 80 | 111.1 | 138 |

the amplifier is thus met with sufficient margins. It is to be mentioned that the reduction in current level has not only led to reduced power dissipation but also to reduced area due to reduction in transistor widths of transistors M4 through M19.

# 7 Conclusion

Potential Distribution Method (PDM) is a technology independent, simple and quick design methodology for designing analog circuits. Being free from complex mathematical expressions, analog designers with some basic knowledge on operating point (DC bias point) of transistors, can design opamps with moderate performance in a very short time using simulators. PDM also provides a mechanism for performance tuning when specifications of the circuit are precise. For estimation of device geometry, it directly employs a circuit simulator, which uses state-of-the-art MOSFET models like BSIM. The resultant design is guaranteed to work in first attempt. In this work, PDM is applied for designing a fully differential folded cascode opamp using UMC 180 $\mathrm{nm}$ CMOS process. Tuning capabilities and guidelines for meeting target specifications like DC gain, UGF, bandwidth, output resistance etc. are also illustrated. However, PDM may not always result the best and fully optimized design in its present form. But surely, PDM is a fast approach to realize analog circuits with good performance which could be tuned further using traditional methods to get optimum performance.

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