A Digitally Assisted Telescopic Amplifier With Improved ICMR and Programmable Unity Gain Frequency

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Abstract: Telescopic amplifiers are often preferred for their large DC gain, low power dissipation and low flicker noise. On the other side, they suffer from serious problems like poor input common mode range and output swing. In this work, a simple technique to improve the input common mode range of telescopic structure is presented. To achieve this, two telescopic amplifiers using complementary differential pairs are utilized. The proposed design incorporates a digital switching technique which enables to maintain a flat response throughout the extended input common mode range. It also provides a facility to elevate the performance of the circuit over a predefined range of input common mode level, at the cost of extra power. The entire design is verified using UMC 180 nm CMOS technology and the simulation results are presented.

Key–Words: Analog design, CMOS; operational amplifier, telescopic amplifier, input common mode range, complementary amplifier.

1 Introduction

Operational amplifiers are one of the most important building block of analog and mixed signal circuits. Various topologies of amplifiers can be found in literature and research papers differentiated by their characteristic performance parameters. Amplifiers are primarily characterised by parameters like DC gain, output resistance, unity gain frequency (UGF), bandwidth, input common mode range (ICMR), output swing, power dissipation, etc.

It is known that cascoding of transistors increases the output impedance and hence the gain of the amplifier. Telescopic amplifiers are commonly used cascoded architecture that features large DC gain from a single stage but suffers from serious problems like poor input common mode range (ICMR) and output swing [1]. ICMR issues are solved by folded cascode architecture where ICMR extends beyond the supply rail on at least one side [2]. Alternate schemes have also been proposed like the one given in [3] where the folded cascode opamp exhibits rail to rail ICMR by employing complementary input pair and sharing the load branch. However, folded cascode structures offer lesser gain, consume larger current due to presence of two branches and contribute more noise as compared to telescopic structures [4].

Several reports are found to increase the output swing of telescopic structures [5]. However, techniques to improve the ICMR of telescopic structure remains relatively unexplored. In this work, a simple scheme to extend the ICMR of telescopic structure using complementary differential pair is presented. The scheme also includes a provision for enhancing the unity gain frequency of the amplifier over a range of input common mode level.

2 Typical Telescopic Amplifiers

A typical NMOS differential pair based fully differential telescopic amplifier with common mode feedback (CMFB) circuit is shown in Figure 1. Transistors Mn1 to Mn9 form the telescopic amplifier while Mn10 to Mn17 form the common mode feedback (CMFB) circuit. Mathematically, the ICMR (ICMR$^-$ to ICMR$^+$) of this amplifier can be expressed as

$$ICMR^+_{NMOS} = Vout - V_{DS,sat(Mn4)} - V_{DS,sat(Mn2)} + V_{GS(Mn2)} \quad (1)$$

$$ICMR^-_{NMOS} = V_{DS,sat(Mn9)} + V_{GS(Mn2)} \quad (2)$$

Similarly, PMOS differential pair based fully differential telescopic amplifier with CMFB circuit is shown in Figure 2 with transistors Mp1 though Mp9 forming

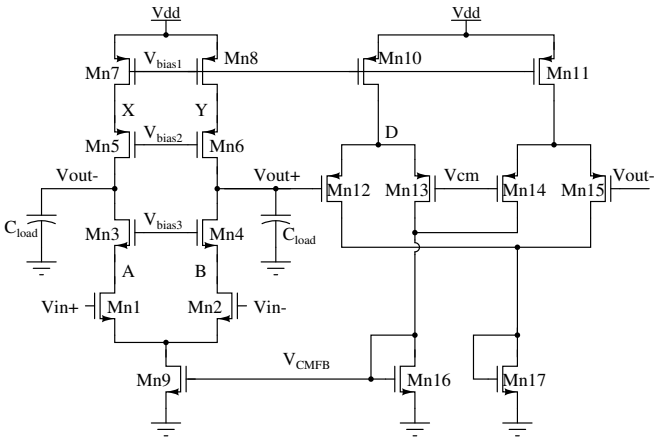


Figure 1: Typical Telescopic Amplfiers with CMFB and NMOS Input Pair

the telescopic amplifier and Mp10 to Mp17 forming the CMFB circuit. The ICMR of this structure can be given by

$$ICMR^{+}_{PMOS} = V_{DD} - |V_{DS,sat(Mp9)}| - |V_{GS(Mp2)}| \quad (3)$$

$$ICMR^{-}_{PMOS} = Vout + |V_{DS,sat(Mp4)}| + |V_{DS,sat(Mp2)}| - |V_{GS(Mp2)}| \quad (4)$$

For a 1.8 V technology, the typical response of amplifiers shown in Fig. 1 and 2 is listed in Table 1. The parameters are measured keeping input and output common mode level at $V_{DD}/2$ = 0.9 V. The two amplifiers are designed using Potential Distribution Method (PDM) [6, 7, 8]. The NMOS input pair based amplifier consumes 20 μA at each tail transistor Mn9,

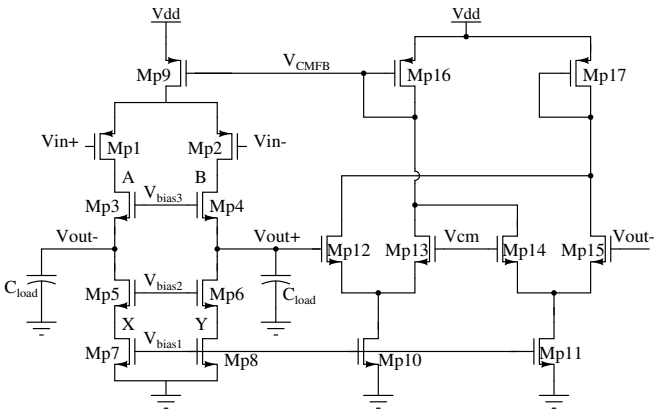


Figure 2: Typical Telescopic Amplfiers with CMFB and PMOS Input Pair

Mn16 and Mn17. For matching the performance of the PMOS based amplifier with that of NMOS based, the source currents of PMOS based amplifier is set to 24 μA at transistors Mp9, Mp16 and Mp17, and its node potentials are adjusted as suggested by PDM [7]. It may be mentioned that designing a PMOS based amplifier matching the AC response of NMOS based amplifier was easily achieved by applying PDM. For achieving large ICMR and for comparative purpose, the overdrive of all transistors in both amplifiers are kept at about 5% of V_{DD}. It is known that both the amplifiers see a dominant pole at the output node and a non-dominant pole at node A (or B) [4]. The dominant pole of the two amplifiers are nearly at the same location. However, the non-dominant pole of the PMOS input pair based amplifier is much lower than its NMOS counterpart. This is due to the fact that in PMOS based amplifier, the capacitance at node A (or B) is accounted by PMOS transistors while in NMOS based amplifier, by NMOS transistors. For carrying the same current, at identical overdrive and channel length, PMOS transistors are around 3 to 4 times wider than NMOS transistors and hence capacitance at node A (or B) of PMOS based amplifier is much larger than that of NMOS based amplifier.

Table 1 clearly shows that the AC response parameters like DC gain, -3 dB bandwidth, unity gain frequency (UGF), transconductance and dominant pole of the two amplifiers closely match. From this table it is evident that telescopic architectures exhibit small ICMR but large DC gain even with a single stage. It is to be noted that NMOS based amplifier has lower $ICMR^{-}$ than PMOS based, while PMOS based amplifier has larger $ICMR^{+}$ than NMOS based. The input common mode response of the amplifiers is now studied.

The AC response of the amplifiers over a wide range of input common mode level are shown in Figure 3 and 4. It is clear that the response of the two amplifiers are comparable over the range of input common mode level. The phase margin of both amplifiers remain around 85° to 90° throughout the range of input common mode. From Figure 3 and 4 it may be concluded that the ICMR of telescopic structure can be improved if we operate NMOS differential pair based amplifier when input common mode level is below $V_{DD}/2$ or 0.9 V and PMOS differential pair based amplifier when input common mode level is above $V_{DD}/2$ or 0.9 V. However, there is a region around 0.9 V where both amplifiers work satisfactorily (from $ICMR^{-}_{PMOS}$ to $ICMR^{+}_{NMOS}$). In this region, both, NMOS and PMOS based amplifiers can be made to work in parallel and we can achieve elevated or improved performance.

Table 1: Response of Typical Telescopic Amplifiers

Performance Parameter @ $V_{in,dc}$ = 0.9 V	NMOS Differential Pair Based Amplifier (Figure 1)	PMOS Differential Pair Based Amplifier (Figure 2)
$ICMR^-$	0.62 V	0.85 V
$ICMR^+$	0.95 V	1.06 V
ICMR	0.33 V	0.21 V
% ICMR	18%	11%
C_{Load}	1 pF	1 pF
DC Gain	62.42 dB	62.41 dB
UGF	21.12 MHz	20.37 MHz
-3 dB Bandwidth	15.67 kHz	15.81 kHz
Phase Margin	89.4°	87.6°
Transconductance (g_m)	140 $\mu A/V^2$	135 $\mu A/V^2$
Tail Current (I_{Tail})	20 μA	24 μA
CMFB Current (I_{CMFB})	20 μA	24 μA
Total Current	60 μA	72 μA
Power Dissipation	108 μW	129.6 μW
Slew Rate	20 $V/\mu s$	24 $V/\mu s$
Dominant Pole	15.98 kHz	15.45 kHz
Non-Dominant Pole	2.09 GHz	519.3 MHz
CMRR	270.5 dB	312.4 dB
PSRR	237.5 dB	242.2 dB
Total Input Referred Noise (1 Hz to 20 MHz)	115.76 $\mu V/\sqrt{Hz}$	151.21 $\mu V/\sqrt{Hz}$

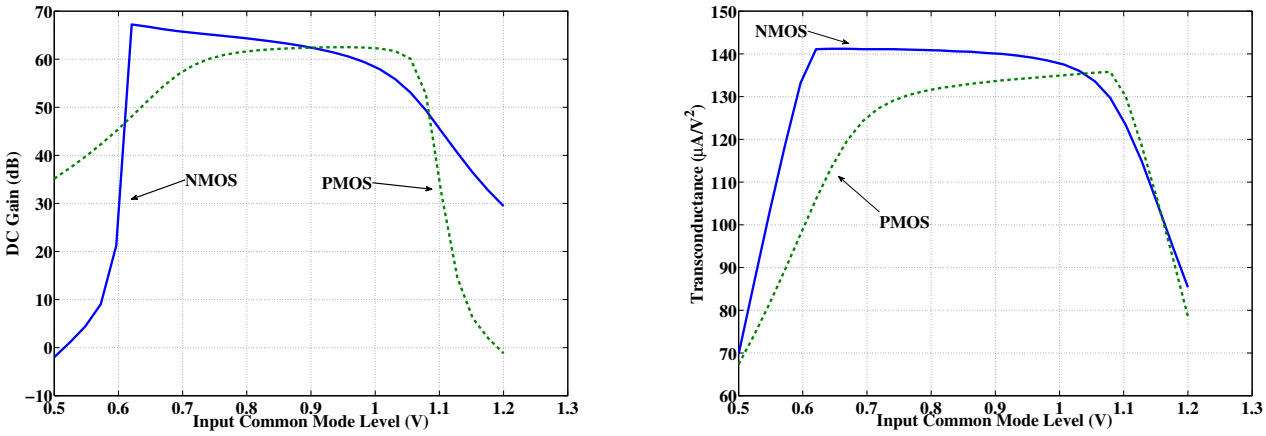
3 Proposed Telescopic Amplifier

The block diagram of the proposed telescopic amplifier structure is shown in Figure 5. It comprises of mainly four parts, the two complementary telescopic amplifiers in parallel, based on NMOS and PMOS input pairs, an amplifier selection and power control circuit and an output selection circuit. Two reference voltages and a low power enable signals are applied externally such that, when the input common mode level is below lower reference voltage, only NMOS input pair based amplifier remains active and when input common mode level is above upper reference, only PMOS input pair based amplifier remains active. When input common mode level is between the two references, both the amplifiers are activated and operate in parallel. The amplifier selection and power control circuit is responsible for generating control signals for activating and deactivating the amplifiers or switching to low power mode when both amplifiers are on. The output selection circuit connects the outputs of the amplifier to the load as per the input common mode level.

3.1 Amplifier Selection And Power Control Circuit

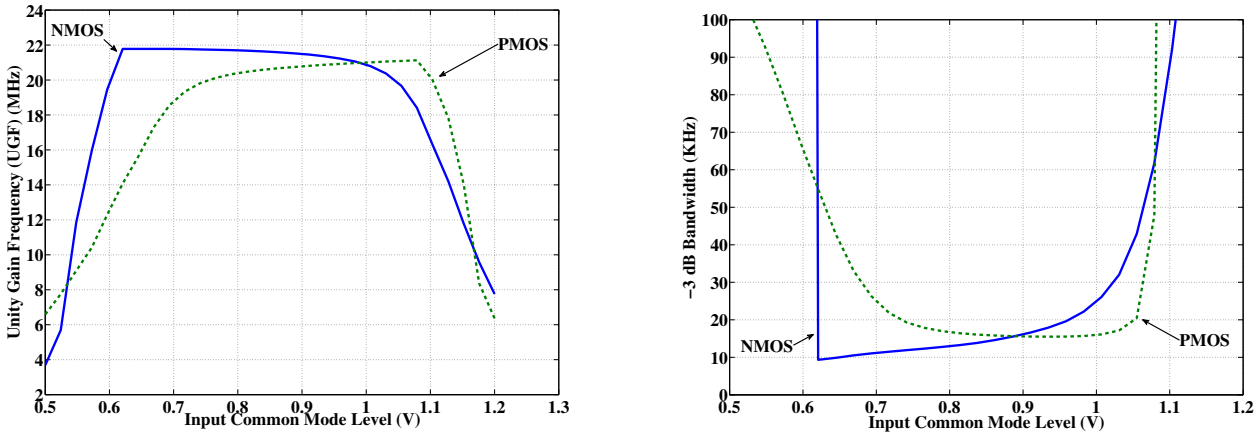
The amplifier selection and power control circuit is responsible for generating digital signals to on/off the amplifiers and control power dissipation when both amplifiers are on.

The inputs to this circuit are the two reference values ($V_{ref}+$ and $V_{ref}-$), along with either of the inputs (Vin+ or Vin−). Let the DC level of the in-



(a) (b)

Figure 3: Response Of Typical Telescopic Amplfiers (a) DC Gain (b) Transconductance (g_m)



(a) (b)

Figure 4: Response Of Typical Telescopic Amplifiers (a) Unity Gain Frequency (UGF) (b) -3 dB Bandwidth

put be denoted by $V_{in,dc}$. The reference voltages are now chosen which marks the switching point of the amplifiers. It also defines the range over which both the amplifiers operate (when input common mode is between the two references). Typically, they are chosen above and below $V_{DD}/2$. Since during this range, both amplifiers operate, $V_{ref}-$ can have a minimum value equal $ICMR^{-}_{PMOS}$ and $V_{ref}+$ can have a maximum value equal $ICMR^{+}_{NMOS}$.

Depending upon the the DC level of the input voltage $V_{in,dc}$, control signals *n_select* and *p_select* are generated. As long as $V_{in,dc} < V_{ref}+$, *n_select* = V_{DD} (logic high), and as long as $V_{in,dc} > V_{ref}-$, *p_select* = V_{DD} (logic high). When the $V_{in,dc}$ is between the two references, *n_select* = *p_select* = V_{DD}. The signals *n_select* and *p_select* are used to turn on the NMOS and PMOS based amplifiers respectively.

This block generates another signal labelled *ctrl* which goes high when *n_select*, *p_select* and *low_power_en* are high at the same time. The signal *low_power_en* is used to activate low power mode when both amplifiers are on. The low power mode makes both the amplifier circuits consume half current, keeping total current more or less flat throughout ICMR. The signals *n_select* and *p_select* can be generated by comparing the input common mode with reference voltages using comparators [9]. The signal *ctrl* is simply the logical AND of *n_select*, *p_select* and *low_power_en*.

Table 2 shows the logical values of signals produced by the amplifier selection and power control circuit under the three cases of input DC level, with low power mode enabled and disabled. It can be seen

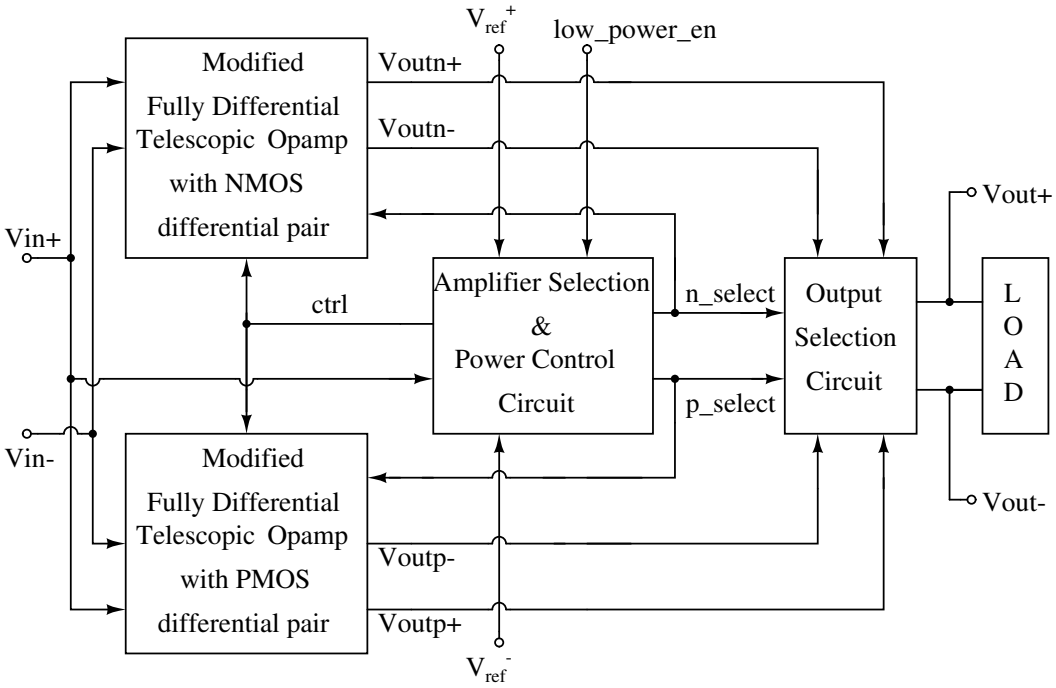


Figure 5: Block Diagram Of Proposed Telescopic Amplifier

Table 2: Amplifier Selection and Power Control Circuit Outputs (H: Logic High (1.8 V); L: Logic Low (0 V))

Case	Input Common Mode ($V_{in,dc}$)	n_select	p_select	low_power_en	ctrl
I	$V_{in,dc} < V_{ref}-$	H	L	H	H
				L	H
II	$V_{ref}- < V_{in,dc} < V_{ref}+$	H	H	H	L
				L	H
III	$V_{in,dc} > V_{ref}+$	L	H	H	H
				L	H

from the table that when both amplifiers are on, as in Case II, and low power mode is enabled (logic high), *ctrl* becomes low. These are used to open the switches in amplifier circuits to cut out half the current and reduce power dissipation. At other times, *ctrl* stays high, switches remain closed and the amplifier circuit draws full current.

3.2 Output Selection Circuit

The output selection circuit can be designed as a simple arrangement of switches implemented using transmission gates which connect the outputs of the two amplifiers across the load. The transmission gates are driven by same signal which activates/deactivates the amplifiers (*n_select* and *p_select*). Whichever amplifier is on, the transmission gate in its path is turned on and amplifier output node is connected across the load. When an amplifier turns off, its output node is disconnected from across the load.

3.3 NMOS Differential Pair Based Amplifier

The NMOS differential pair based telescopic amplifier shown in Figure 6(a) has three modes of operation. First, *full current mode* where tail current is 20 μA. Second, *half current mode* where all currents reduce to half of full current. Third, *turn off mode* where all currents become zero.

In deep sub-micron devices, for reducing currents to half, simply reducing the transistor widths by half while keeping overdrive and channel length constant does not work. To arrive to the transistors widths for Figure 6(a), two amplifiers like shown in Figure 1 are

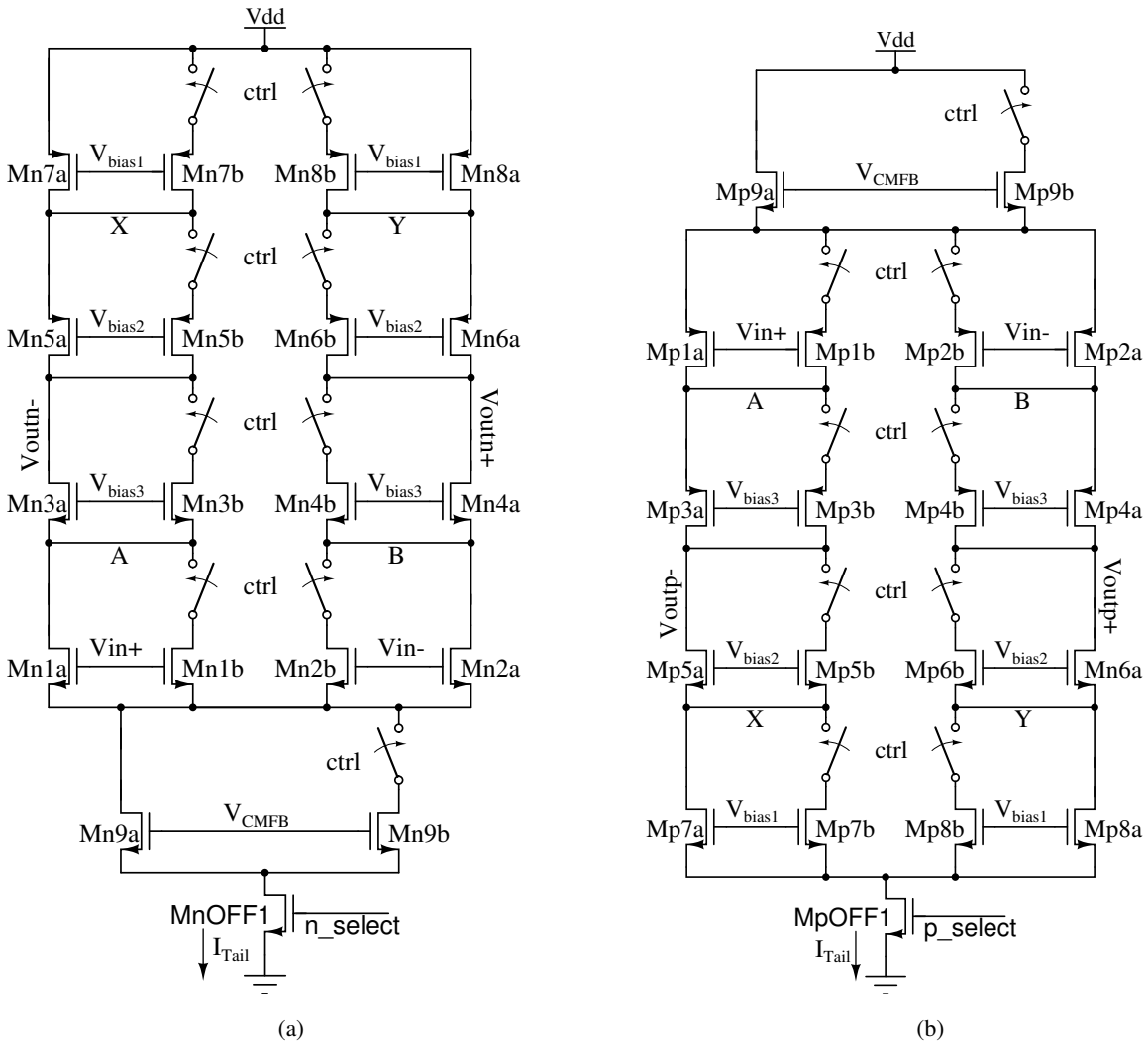


Figure 6: (a) Modified NMOS Based Telescopic Amplifier (b) Modified PMOS Based Telescopic Amplifier

designed, one with full current (20 μA tail current), and one with half current (10 μA tail current). Let the transistor widths be denoted by W_{20} and W_{10} respectively. The two amplifiers must have the same node potential (drain to source drops and gate overdrive) so that ICMR is maintained. The length of all transistors are kept constant and identical for simplicity.

For the amplifier shown in Figure 6(a), all transistors labelled *MnXa*, where *X* takes value from 1 to 9, have widths equal to the corresponding transistor in amplifier carrying half tail current (W_{10}). While all transistors labelled *MnXb* have widths equal to the difference between the widths of transistors carrying full current and half current (W_{20}-W_{10}). As already mentioned, this way of sizing is necessary in deep submicron devices. The CMFB circuit is not shown but is designed in same way as the amplifying branch.

During Case I of Table 2, *ctrl* is always high. As a result, all switches are closed and effective channel width of all transistors is equal to W_{20}. The amplifier circuit thus draws full current. During Case II, as long as low power mode is disabled, circuit still draws full current. When *ctrl* goes low to activate power saving mode, switches open thereby cutting out all transistors labelled *MnXb*. The effective channel width now becomes equal to W_{10} since only transistors labelled *MnXa* conduct. The current consumption thus becomes half. An additional transistors labelled *MnOFF1* is used to turn off this amplifier. It is driven by the *n_select* signal generated by the amplifier selection and power control circuit. Finally, during Case III, this amplifier turns off. The switches can be implemented using transmission gates.

Just like the traditional telescopic amplifier, the dominant pole of this amplifier is located at the output node and the non-dominant pole at node A (or B). The

two poles are given by equations (5) and (6).

$$\text{Dom. Pole} \Rightarrow \omega_{p,Voutn} = \frac{1}{R_{Voutn} \times C_{Voutn}} \quad (5)$$

$$\text{Non-Dom. Pole} \Rightarrow \omega_{p,B(NMOS)} = \frac{g_{m4}}{C_{B(NMOS)}} \quad (6)$$

where,

$$R_{Voutn} \approx (g_{m4}\, r_{o4}\, r_{o2}) \,||\, (g_{m6}\, r_{o6}\, r_{o8}) \quad (7)$$

$$C_{Voutn} \approx C_{db4} + C_{dg4} + C_{db6} + C_{dg6} \quad (8)$$

$$C_{B(NMOS)} \approx C_{db2} + C_{dg2} + C_{sb4} + C_{gs4} \quad (9)$$

The ICMR of the amplifier shown in Figure 6(a) is same as that of the amplifier shown in Figure 1 since all overdrives and channel lengths are kept constant. As already mentioned, the ICMR$^-$ of the proposed structure is decided by NMOS input pair based amplifier. It is expressed as,

$$ICMR^- = V_{DS,sat(Mn9a)} + V_{GS(Mn2a)} \quad (13)$$

3.4 PMOS Differential Pair Based Amplifier

The PMOS differential pair based telescopic amplifier is shown in Figure 6(b). The design procedure and transistor sizing is done in the same way as the NMOS based amplifier. This amplifier consumes a current of 24 μA at tail transistor in full current mode. During half current mode, *ctrl* goes low, all switches open and thus current through all transistors labelled *MpXb* become zero and overall current reduces to half. Transistor labelled *MpOFF1* is responsible for turning off/on the amplifier. It is driven by *p_select* which turns low in Case I of Table 2. During Cases II and III, PMOS based amplifier remains on. The dominant and non-dominant pole of this amplifier are also due to output node and node A (or B) respectively and is given by equations (14) and (15).

$$\text{Dom. Pole} \Rightarrow \omega_{p,Voutp} = \frac{1}{R_{Voutp} \times C_{Voutp}} \quad (14)$$

$$\text{Non-Dom. Pole} \Rightarrow \omega_{p,B(PMOS)} = \frac{g_{m4}}{C_{B(PMOS)}} \quad (15)$$

where,

$$R_{Voutp} \approx (g_{m4}\, r_{o4}\, r_{o2}) \,||\, (g_{m6}\, r_{o6}\, r_{o8}) \quad (16)$$

$$C_{Voutp} \approx C_{db4} + C_{dg4} + C_{db6} + C_{dg6} \quad (17)$$

$$C_{B(PMOS)} \approx C_{db2} + C_{dg2} + C_{sb4} + C_{gs4} \quad (18)$$

The right hand side of equations (15) to (18) have analogous interpretations as discussed earlier in equations (10) to (12). The ICMR$^+$ of the proposed structure is decided by PMOS input pair based amplifier. It is expressed as,

$$ICMR^+ = V_{DD} - |V_{DS,sat(Mp9a)}| - |V_{GS(Mp2a)}| \quad (19)$$

The dominant pole of the complete structure is given by

$$\text{Dominant Pole} \Rightarrow \omega_{p,out} = \frac{1}{R_{out} \times C_{out}} \quad (20)$$

where,

$$R_{out} = R_{Voutn} \,||\, R_{Voutp} \quad (21)$$

$$C_{out} = C_{load} + C_{Voutn} + C_{Voutp} \quad (22)$$

As discussed earlier, the non-dominant pole arises due to node B of both the amplifier circuits. However, since node B of PMOS based amplifier see a larger capacitance than node B of NMOS based amplifier, the non-dominant pole of entire circuit is due to node B of PMOS based amplifier and is given by equation (18).

The voltage gain of the proposed structure can be expressed as

$$A_v = g_m \times R_{out} \quad (23)$$

where, The expression for R_{out} is also derived as per the region of operation and using equations (7), (10), (11), (16) and (21).

During Case II of Table 2, when low power mode is disabled, both amplifiers are on and conduct full current. At this time, the transconductance is double as compared to the other times. This is due to doubling of drain currents. However, due to almost doubled transistor width, the output resistance is halved and the overall DC gain remains the same. At other times, the transconductance and output resistance remain almost constant for the entire ICMR maintaining the DC gain.

4 Simulation

In this section, simulations methods and results are discussed.

4.1 Simulation Methods

The complete design was implemented using UMC 180 nm CMOS technology in Cadence environment. The circuit was first put into low power mode and

$$g_{mi} = \left\{ \begin{array}{ll} g_{m(Mnia)} + g_{m(Mnib)} & \text{if low power disabled} \\ g_{m(Mnia)} & \text{if low power enabled} \end{array} \right\} for\ i = 4, 6 \quad (10)$$

$$r_{oj} = \left\{ \begin{array}{ll} r_{o(Mnja)} \,||\, r_{o(Mnjb)} & \text{if low power disabled} \\ r_{o(Mnja)} & \text{if low power enabled} \end{array} \right\} for\ j = 2, 4, 6, 8 \quad (11)$$

$$C_{Xk} = \left\{ \begin{array}{ll} C_{X(Mnka)} + C_{X(Mnkb)} & \text{if low power disabled} \\ C_{X(Mnka)} & \text{if low power enabled} \end{array} \right\} for\ X = db, dg, sb, gs;\ k = 2, 4, 6 \quad (12)$$

$$g_m = \left\{ \begin{array}{ll} g_{m(Mn2a)} + g_{m(Mn2b)} & \text{Case I} \\ g_{m(Mn2a)} + g_{m(Mn2b)} + g_{m(Mp2a)} + g_{m(Mp2b)} & \text{Case II; low power disabled} \\ g_{m(Mn2a)} + g_{m(Mp2a)} & \text{Case II; low power enabled} \\ g_{m(Mp2a)} + g_{m(Mp2b)} & \text{Case III} \end{array} \right. \quad (24)$$

thorough response was observed. Then low power mode was disabled and the observations are redone. The graphs obtained during the two modes of operation were compared and are presented ahead.

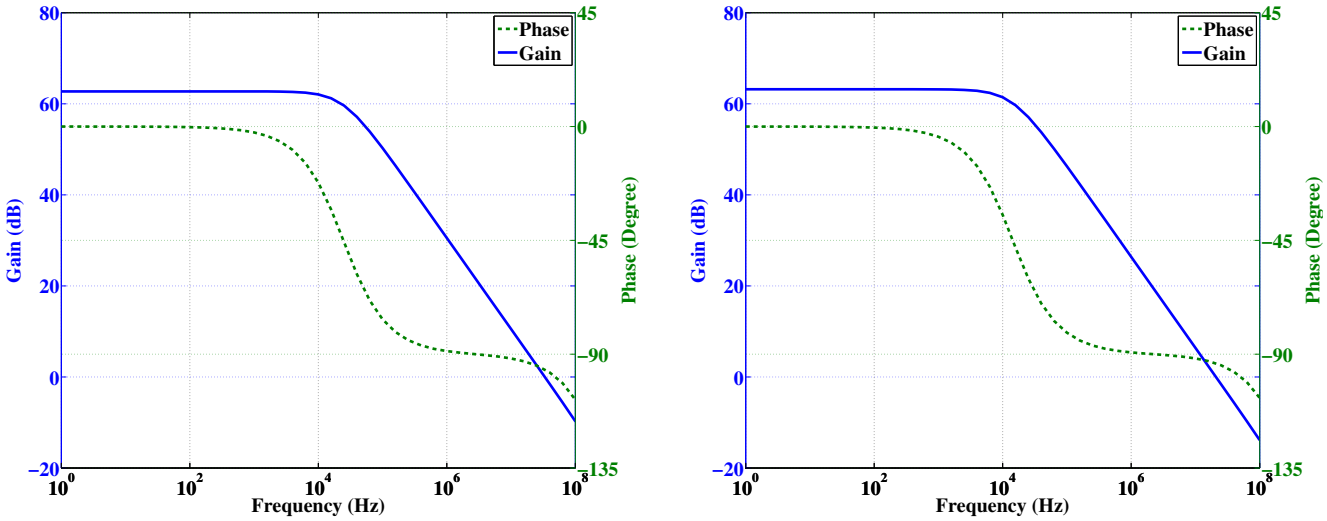
4.2 Simulation Results

The simulation results are presented from Figure 7 to 11 and Table 3. Figure 7(a) and 7(b) show the bode plots for the proposed amplifier circuit with low power mode disabled and enabled respectively, with input and output common mode at $V_{DD}/2$ = 0.9 V and load capacitance of 1 pF. When low power mode is disabled, both amplifiers consume full current. When enabled, they consume half the current. From Figure 7 it is clear that the circuit sees only one pole, the dominant pole, before the unity gain frequency.

The complete response of the proposed circuit is given in Table 3. Since the non-dominant pole appears much beyond the unity gain frequency, the circuit is stable. The DC gain in the two modes of operation is fairly the same. The response of the proposed amplifier in low power mode is almost matching the response of the typical amplifiers from Table 1. When low power mode is disabled, both the amplifier circuits consume full current leading to increased current but twice the bandwidth, transconductance and slew rate. The UGF increases by 1.5 times due to simultaneous increase in capacitance at output node because of increased effective transistor width, along with doubling of transconductance (UGF = g_m/C_{out}) [10]. The ICMR in both the modes remains the same since all node voltages are maintained. Small reduction in input referred noise is also seen when full current is drawn.

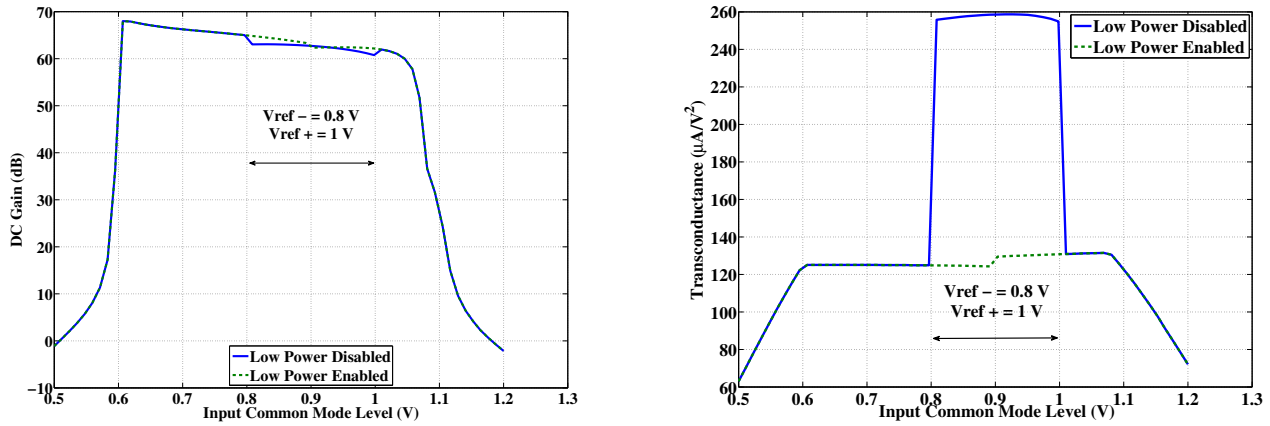
To illustrate the response of the proposed structure over the range of ICMR, Figure 8 to 10 are plotted. The reference voltages for amplifier selection are kept at 0.8 V and 1 V for all the graphs. Figure 8(a) shows that the DC gain of the amplifier remains more or less constant, with or without low power mode enabled. From Figure 8(b) it can seen that the transconductance remains constant throughout the range of ICMR with low power mode enabled. When low power mode is disabled, the transconductance doubles in the range between the two reference voltages. This is due to doubling of drain currents at constant overdrive. In this region, performance elevation is achieved at the expense of increased power dissipation. Consequential effects in the UGF and bandwidth are also seen due to doubling of transconductance and reduction in output resistance. The phase margin, depicted in Figure 10(a), however remains constant throughout the ICMR. Figure 10(b) shows an estimated current consumption over the range of ICMR.

To show the transient behaviour, the proposed amplifier is connected in unity feedback mode and a step input lying within its ICMR is applied. The response is shown in Figure 11. The signal swing is chosen such that the circuit passes through all three regions of operation. The transistor widths of the final design in given in Table 4. The other transistors which are operating with digital inputs can be designed with minimum size or any other size as suitable for the designer such that the drop across them in negligible when on.



(a) (b)

Figure 7: Bode Plot Of Proposed Telescopic Amplifier at Vin, dc = 0.9 V (a) Low Power Disabled (b) Low Power Enabled



(a) (b)

Figure 8: Response Of Proposed Telescopic Amplifiers (a) DC Gain (b) Transconductance (g_m)

5 Conclusion

In this work a digitally assisted complementary telescopic amplifier with improved input common mode range is presented. Digital assistance is employed to turn on/off the amplifiers and to activate or deactivate low power mode as per input DC level to maintain power consumption or elevate circuit performance at the cost of addition power. The proposed design shows an improvement in input common mode range by 33% and 109% over conventional NMOS and PMOS differential pair based telescopic amplifier respectively, while maintaining power dissipation and other performance parameters. The percentage ICMR of V_{DD} has increased from 18% in NMOS and 11% in PMOS to 25% in the proposed design. The complete design is verified using UMC 180 nm CMOS technology and the simulation results are presented.

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Table 3: Response of Proposed Telescopic Structure

Performance Parameters @ $V_{in,dc}$ = 0.9 V	Proposed Structure (Fig. 5)		Typical NMOS Based (Figure 1)	Typical PMOS Based (Figure 2)
	Low Power Disabled	Low Power Enabled		
$ICMR^-$	0.62 V	0.62 V	0.62 V	0.85 V
$ICMR^+$	1.06 V	1.06 V	0.95 V	1.06 V
ICMR	0.44 V	0.44 V	0.33 V	0.21 V
% ICMR of V_{DD}	25%	25%	18%	11%
% Increase in ICMR Over Fig. 1, Fig. 2	33%, 109%	33%, 109%	-	-
C_{Load}	1 pF	1 pF	1 pF	1 pF
DC Gain	62.72 dB	63.19 dB	62.42 dB	62.41
UGF	33.46 MHz	20.85 MHz	21.12 MHz	20.37 MHz
-3 dB Bandwidth	24.36 kHz	13.91 kHz	15.67 kHz	15.81 kHz
Phase Margin	83.2°	86.38°	89.4°	87.6°
Transconductance (g_m)	258.6 $\mu A/V^2$	149.7 $\mu A/V^2$	140 $\mu A/V^2$	135 $\mu A/V^2$
Total Current	132 μA	66 μA	60 μA	72 μA
Power Dissipation	237.6 μW	118.8 μW	108 μW	129.6 μW
Slew Rate	44 $V/\mu s$	22 $V/\mu s$	20 $V/\mu s$	24 $V/\mu s$
Dominant Pole	24.54 kHz	14.2 kHz	15.98 kHz	15.45 kHz
Non-Dominant Pole	371.8 MHz	381.7 MHz	2.09 GHz	519.3 MHz
CMRR	226 dB	223.42 dB	270.5 dB	312.4 dB
PSRR	214.12 dB	211.23 dB	237.5 dB	242.2 dB
Total Input Referred Noise (1 Hz to 20 MHz)	101.05 $\mu V/\sqrt{Hz}$	115.62 $\mu V/\sqrt{Hz}$	115.76 $\mu V/\sqrt{Hz}$	151.21 $\mu V/\sqrt{Hz}$

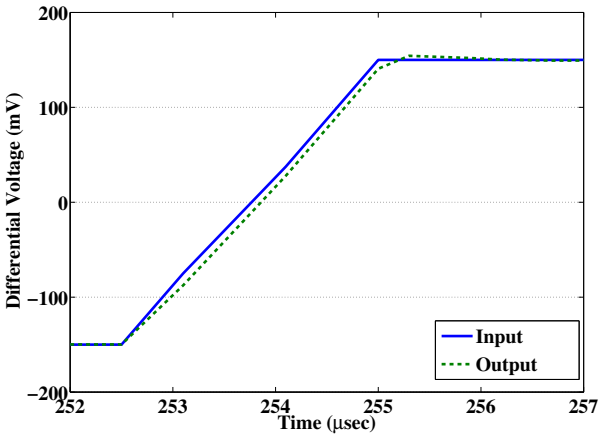
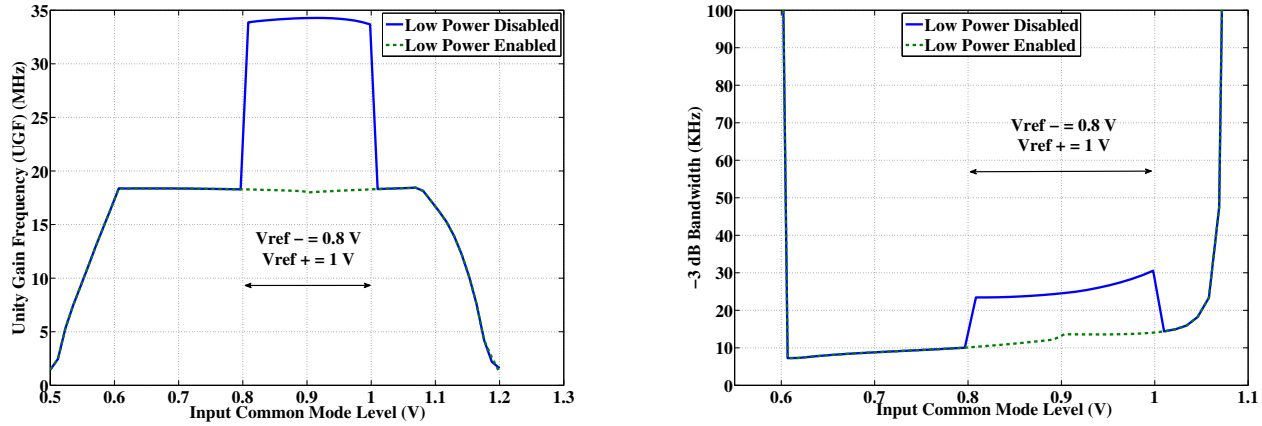
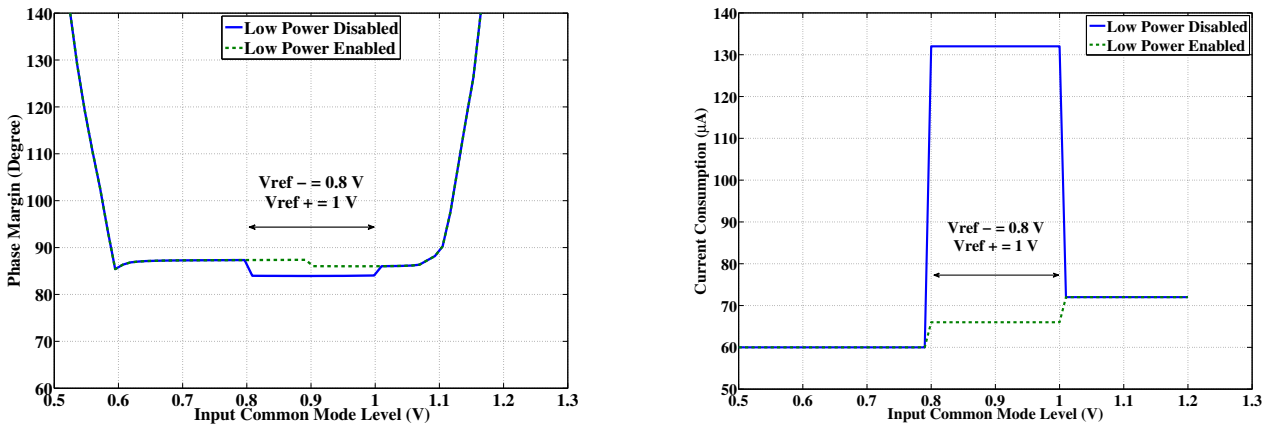


Figure 11: Step Response of Proposed Telescopic Amplifier



(a) (b)

Figure 9: Response Of Proposed Telescopic Amplifiers (a) Unity Gain Frequency (UGF) (b) -3 dB Bandwidth



(a) (b)

Figure 10: Response Of Proposed Telescopic Amplifiers (a) Phase Margin (b) Current Consumption

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Table 4: Transistor width of proposed design (Length = 500 nm)

NMOS Based Amp Figure 6(a)	Transistor Width ($\mu\mathrm{m}$)	PMOS Based Amp Figure 6(b)	Transistor Width ($\mu\mathrm{m}$)
Mn1a, Mn2a	1.36	Mp1a, Mp2a	5.64
Mn1b, Mn2b	1.17	Mp1b, Mp2b	2.59
Mn3a, Mn4a	1.16	Mp3a, Mp4a	6.65
Mn3b, Mn4b	0.85	Mp3b, Mp4b	6.36
Mn5a, Mn6a	4.85	Mp5a, Mp6a	1.67
Mn5b, Mn6b	4.17	Mp5b, Mp6b	1.46
Mn7a, Mn8a	5.63	Mp7a, Mp8a	1.41
Mn7b, Mn8b	4.99	Mp7b, Mp8b	1.21
Mn9a	2.33	Mp9a	13.70
Mn9b	2.09	Mp9b	13.66

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