Sampling Clock Imperfection Analysis for Synthetic Aperture Interferometric Radiometer

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Abstract: - In this paper, a nontrivial sampling clock imperfection analysis is presented for Synthetic Aperture Interferometric Radiometers (SAIR). Sampling clock determines the edges at which analog radiometric demodulated signal are digitized for digital correlation, and its jitter and skew could lead to SAIR performance degradations. Firstly, the jitter and skew contributions to visibility uncertainty degradation is analyzed by SAIR correlation principles. Secondly, clock jitter effects on Analog-to-Digital Converter (ADC) SNR is demonstrated, and this effect is quantitatively evaluated by Time Interval Error (TIE) jitter. The jitter simulation method by Phase Noise Integration (PNI) is also proposed. Thirdly, the Phase Synchronization Method (PCM) is presented to decrease the clock skews between correlation channel pairs to improve decorrelation effects. The experimental verifications for clock jitter and skews are conducted on the BHU-2D-U SAIR instrument, and the contributions of this paper are concluded. This paper has proposed nontrivial imperfection analysis for SAIR sampling clock, and the conclusions could be used for SAIR and polarimetric radiometer digital correlation designs.

Key-Words: - Samping Clock, Jitter, Skew, SAIR, Visibility Uncertainty, SNR, TIE Jitter

1 Introduction

Synthetic Aperture Interferometric Radiometer (SAIR) offers a way of realizing the full potential of microwave remote sensing from space by overcoming the antenna size and on-board weight limitations, and the system configuration is highly flexible [1]. Several SAIR imaging systems have been in operation, and visibility uncertainty is vital for radiometric correlation performance [2-9]. 1bit/2level digital correlations are applied [10], for analog correlations have unavoidable defects such as temperature drift and unacceptable size. Therefore, IF signal must be digitized by ADCs before digital correlation, but this operation leads to visibility degradations [11,12].

Sampling clock determines the edges at which sampling operations are conducted. Clock imperfections such as jitter and skew, the difference of edges between channel pairs, could both lead to SAIR performance degradations. This paper analyzes these two effects in detail.

The analysis begins with SAIR imaging principle, then focuses on the analysis of sampling clock jitter and skew. Firstly, the jitter and skew effects on visibility uncertainties and in the Fringe-Washing-Function (FWF) are shown [3]. Secondly, the sampling clock jitter effects on ADC Signal-to-Noise Ratio (SNR) are shown, and they are quantitatively evaluated by Time Interval Error (TIE) jitter, which is commonly applied in communication industries. Also, the Phase Noise Integration (PNI) method is proposed to simulate TIE jitter. Thirdly, the Phase Synchronization Method (PSM) is illustrated and applied in reducing sampling clock skews between channel pairs, and systematic FWF errors are greatly reduced. Finally, experimental verifications are conducted on BHU-2D-U SAIR instrument, and the contributions of this paper are summarized. This paper has proposed nontrivial imperfection analysis for SAIR sampling clock, and could be applied in the digital correlation design for SAIR and polarimetric radiometers.

2 Clock Imperfection Effects on SAIR Performance

2.1 SAIR Imaging Principle

SAIR measures spectral components of the brightness temperature distribution in the Field Of View (FOV) by correlating received signals, as given in Fig.1 [1]. Visibility is obtained by correlating signal pairs as [3]:

$$V_{ij}(u,v)=\frac{1}{2}E\left[b_i(t)b_j^*(t)\right] \quad (1)$$

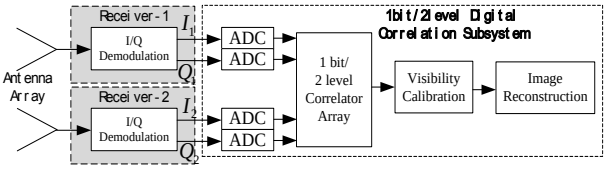

Figure 1: Configuration of a Two Channel Demonstrator Model of SAIR.

Where $E[\bullet]$ is the expectation operator, and * denotes conjugated signal. V_{ij} is the visibility, $b_{i,j}(t)$ is the I/Q demodulated signals, and (u,v) is the baseline. By the Van-Cittert-Zernike Theorem, the relationship between visibility and brightness temperature is [1]:

$$V_{ij}(u,v)=\iint_{\xi^2+\eta^2\le 1} T_M(\xi,\eta)r_{ij}(\tau)e^{-j2\pi(u\xi+v\eta)}d\xi d\eta \quad (2)$$

Which is the integral form of visibility, and $T_M(\xi,\eta)$ is the modified brightness temperature consisting of the target brightness temperature and antenna radiation patterns, $r_{ij}(\tau)$ is FWF, $\xi=\sin\theta\cos\varphi$ and $\eta=\sin\theta\sin\varphi$ are directional cosines. To avoid FOV aliasing and systematic bias, visibility background cancellation method is applied as [13,14]:

$$V_{NORM}=\frac{V_T(u,v)-V_B(u,v)}{V_C(u,v)-V_B(u,v)} \quad (3)$$

Where, $V_T(u,v)$, $V_B(u,v)$ and $V_C(u,v)$ are the target, background and calibrated visibility. Image reconstruction is obtained by the IFT of this pre-processed visibility [13]. Hence, visibility uncertainties could lead to imaging errors, and sampling clock imperfection analysis should be focused on their impacts on visibility functions.

2.2 Clock Jitter and Skew in FWF

From Eq.2, clock jitter and skew are present in the FWF of visibility function, and the timing difference is an independent variable. The FWF in visibility function can be given by [3]:

$$r_{12}(\tau)=\frac{1}{\sqrt{B_1B_2}}\int_0^\infty H_{n1}(f)H_{n2}^*(f)e^{j2\pi f\tau}df \quad (4)$$

Where $B_{1,2}$ and $H_{n1,2}$ are the bandwidth and normalized frequency response of receiver 1 and 2, respectively. τ is the timing difference between channel pairs, including baseline delay, timing jitter and group delay between receiver pairs. The FWF gain factor can be further expressed by [15]:

$$FWF_{Gain}=e^{-\pi[2\pi(f_c\sigma_{clk})^2+(B\tau_s)^2]} \quad (5)$$

Where σ_{clk} is the root-mean-square (rms) sampling clock jitter, τ_s is the sampling clock skew error, f_c is the cutoff frequency of input analog signal. In general, sampling clock jitter can be designed to be less than 10% of group delay, hence its impact on FWF gain is not prominent, but it proposes significant contribution in ADC SNR degradation [11,15]. Sampling clock skew, on the other hand, is a more significant contributor in FWF gain factor and must be carefully controlled.

3 Clock Jitter Characterization and Simulation

As stated above, clock jitter could lead to ADC SNR degradations, and this part analyzes this effect in detail, and a nontrivial simulation method of clock jitter by phase noise integration is proposed.

3.1 Clock Jitter Impact on ADC SNR

If input signal is assumed to be sinusoidal, the widely accepted ADC SNR equation is given by [16]:

$$SNR_{Sine}=-20\lg[(2\pi f_c\sigma_{clk})^2+\frac{2}{3}(\frac{1+\varepsilon}{2^N})^2+(\frac{2\sqrt{2}V_{n,rms}}{2^N})^2]^{\frac{1}{2}} \quad (6)$$

Where the first term inside the square bracket is SNR degradation by clock jitter, the second and third term are caused by quantization and input noise, respectively. For high-bit quantization (more than 4 bit) in SAIR digital correlation, quantization and input noise can be neglected, and clock jitter becomes the dominant contributor of ADC SNR, which can be proposed for sinusoidal input analog signal by [16,17]:

$$SNR_{CLKjitter,Sine}=-20\lg(2\pi f_c\sigma_{clk}) \quad (7)$$

However, SAIR IF signal cannot be regarded as sinusoidal. A more appropriate approximation is given by a Gaussian narrow-band noise, which is represented by a rectangular in Double Side-Band (DSB) power spectrum shown in Fig.2 as:

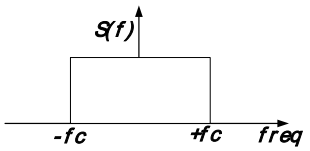

Figure 2: Power Spectrum of IF signal before ADC sampling.

The corresponding SNR equation for this kind of analog signal incurred by sampling clock jitter is proposed by [18]:

$$SNR_{CLKjitter,Gauss} = -20\lg(2\pi f_c \sigma_{clk} / \sqrt{3}) \quad (8)$$

Therefore, the sampling clock jitter requirement is $\sqrt{3}$ times less strict than sinusoidal input SNR. The ADC SNR requirement for SAIR system can be proposed by [19]:

$$SNR_{ADC} = SQNR_{ADC,Gauss} + 20\lg(\frac{V_{p-p,gauss}}{V_{p-p,sine}}) + DR_{\max} + DL \quad (9)$$

In which the second term is the peak-to-average ratio between Gaussian and sinusoidal signal, and maximum receiver Dynamic Range ($DR_{\max}$)and Distortion Loss (DL) should also be considered. The first term is the quantization noise for Gaussian input signal limited by [20]:

$$SQNR_{ADC,Gauss} \geq 10\lg(\frac{T_A + T_R}{\Delta T}) \quad (10)$$

In which $T_A + T_R$ is the SAIR system noise temperature, ΔT is the radiometric temperature sensitivity. A 5 dB margin is selected to avoid clock jitter impact on ADC SNR, then the jitter limit is quantitatively defined as:

$$SNR_{CLKjitter} \geq SNR_{ADC} + 5dB \quad (11)$$

3.2 Clock Jitter Characterization and Simulation

Several characterizations have been proposed for clock stability evaluation [21]. As clock jitter is a long-term effect whose probability density always follows Gaussian distribution, a statistical jitter evaluation is required [22].

Time Interval Error (TIE) jitter is a widely accepted statistical jitter evaluation in communication industries, and as will be demonstrated, this jitter could be simulated by Phase Noise Integration (PNI) [23]. Since most suppliers do not provide jitter measurement results, but only phase noise profiles, it is attractive to use TIE jitter to evaluate sampling clock instability. The real-time TIE is given as [21]:

$$TIE(t) = T(t) - T_{ref}(t) \quad (12)$$

Where $T(t)$ is the actual transition time of the clock edge, and $T_{ref}(t)$ is the ideal transition time. the long-term instability effects of timing jitter is represented by the rms TIE jitter, which can be given by [21,23]:

$$TIE_{rms} = \lim_{N\to\infty} \sqrt{\frac{1}{N-1}\sum_{n=1}^{N} TIE(t_n)^2}, n = 1,2,...,N-1 \quad (13)$$

Phase noise profile in frequency-domain can be given by [24]:

$$L(f - f_c) = 10\lg\left[S_c(f)/S_c(f_c)\right](dBc) \quad (14)$$

The square-wave clock could be given by the sum of odd number Fourier Series as:

$$f(t) = \sum_{i=1}^{2N+1} A_i \sin(2\pi i f_c(t + \frac{\theta_i(t)}{2\pi f_c})), i = 1,3,...,2N+1, N \geq 3 \quad (15)$$

Where A_i is the harmonic amplitude, and the time-domain effect of phase noise is the overall effect of phase instability $\theta(t)$, whose power spectrum is presented by:

$$S_{\theta(t)}(f) = \frac{4}{A^2}\int_{-\infty}^{+\infty} n_\theta(t) e^{-2\pi ft} dt = 10^{\frac{L(f)}{10}} \quad (16)$$

Where $n_\theta(t)$ is the time-domain phase noise term. Since the TIE Jitter could be given by phase instability as:

$$TIE(t_n) = \frac{\theta(t_n)}{2\pi f_c} \quad (17)$$

Where t_n is the nth clock cycle, hence the rms TIE jitter could be simulated by Double Side-Band (DSB) PNI as:

$$J_{TIE,rms} = \frac{\sqrt{\sigma(\theta^2(t))}}{2\pi f_c} = \frac{1}{2\pi f_c}\sqrt{2\int_0^{+\infty} 10^{\frac{L(f)}{10}} df} \quad (18)$$

This conclusioon is useful in TIE jitter evaluations, and will be verified in the results and discussions section.

4 Clock Skew Requirement and Control

4.1 Clock Skew Requirement

Clock skew requirement is analyzed by FWF approximations. If channel frequency response is assumed to be rectangular, phase difference between channel pairs can be expressed as [20]:

$$H_{1,2}(f) = Ae^{j(\phi + \Delta\phi_{1,2})} \quad (19)$$

Where $\Delta\phi_{1,2}$ is the phase difference between channel 1 and 2. Phase difference is often assumed to be uniformly distributed within the limit $\Delta\psi$:

$$p(\Delta\phi)=\begin{cases}\dfrac{1}{2\Delta\psi} & , \ |\Delta\phi|\le\Delta\psi \\ 0 & , \ |\Delta\phi|>\Delta\psi\end{cases} \quad (20)$$

And the FWF can be simplified to:

$$r_{12}(\tau)=\sin(\Delta\phi)/\Delta\phi=Sinc(\Delta\phi) \quad (21)$$

It is found that a 10 deg phase difference could lead to 0.5% visibility degradation, as shown in Fig.3. Sampling clock skew contributes to this difference, and must be decreased as low as possible.

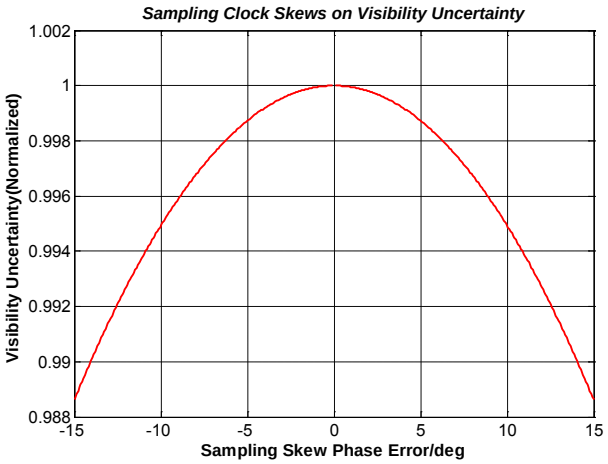

Figure 3: Sampling Clock Skew Errors on Visibility Uncertainty.

4.2 Phase Synchronization Method (PSM)

In SAIR 1 bit/2 level digital correlation architecture, the sampling clock is distributed several times before it is fed to ADC module. If the last stage before being fed to ADC is designed as a Phase Locked Loop (PLL) clock conditioner, then Phase Synchronization Method (PSM) can be applied, whose block diagram is shown in Fig.4:

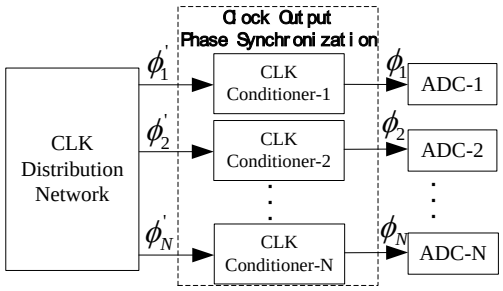

Figure 4: Clock Ouput Phase Synchronization.

The PSM is applied with on-board phase adjustments of the i and j th CLK conditioner as:

$$|\phi_i-\phi_j|\le\Delta\phi_{\max},\ i,j=1,2...N, i\ne j \quad (22)$$

In which an upper limit $\Delta\phi_{\max}$ is defined for sampling clock skew requirement. With the adjusted phase in each clock conditioner, the FWF decorrelation effect caused by sampling clock skews can be reduced. Although this method is tedious, it has to be conducted for a lower sampling skew to reduce FWF gain error.

5 Results and Discussions

Based on the discussions above, the sampling clock jitter, skew and FWF decorrelation effects are demonstrated by the BHU-2D-U SAIR instrument [25-27]. The related systematic parameters are given in Tab.1 below [26]:

Table 1: BHU-2D-U Related Specifications.

Parameter	Specification
Working Distance	2.5-5 m
range Resolution	6.5 cm@3 m
Imaging Rates	2~20 images/sec
Center Frequency	34 GHz
Antenna Temperature	300 K
Temperature Sensitivity	~3K@50ms Integration Time
Calibration Method	External Point Source with Background Cancellation
Receiver Type	Dual Conversion (DSB for I/Q Demodulator)
Receiver Noise Figure	4.5 dB
Receiver Bandwidth	200 MHz DSB
Receiver Dynamic Range	4 dB Max
Power Measurement Sub-System	8 bit ADC (200 MSPS) and 1bit/2level auto Correlator
ADC Distortion Loss	4 dB Max
ADC SNR Requirement	32.2 dB
FWF Gain Error	1.5% Max

5.1 Sampling Clock Jitter and ADC SNR

As the I/Q demodulated radiometric signal covers a $\pm 200MHz$ DSB for BHU-2D-U, the PNI is performed in DSB mode for the sampling clock. Fig.4 gives the single side-band (SSB) RMS jitter of 1.52 ps (100 Hz~200 MHz offset frequency range, which covers flicker noise, in-band PLL noise and wideband thermal noise ranges), and a DSB RMS jitter yields 2.15 ps clock jitter.

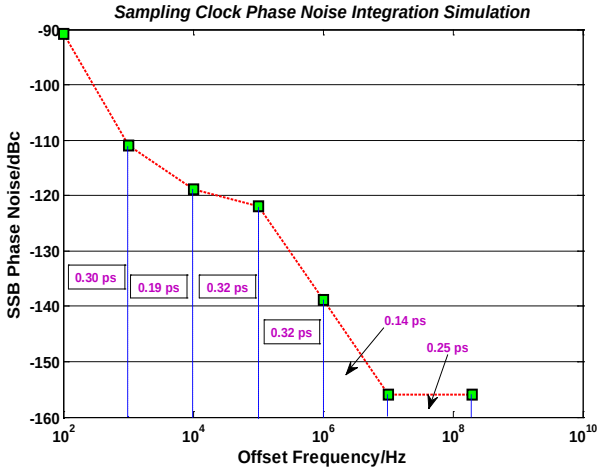

Figure 5: TIE Jitter Simulation by Phase Noise Profile Integration.

TIE jitter measurements are conducted by high sampling rate digital oscilloscopes, and the simplified sampling clock distribution network in BHU-2D-U is given in Fig. 6, in which clock TIE jitter is measured at 3 positions.

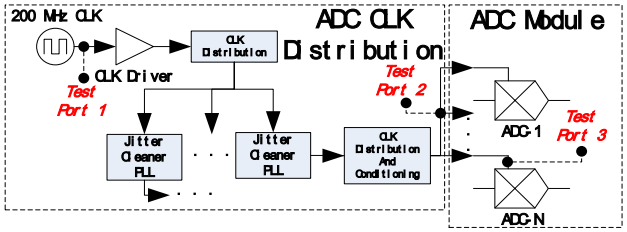

Figure 6: TIE Jitter Measurement Setup.

Test results are shown in Fig. 7, and clock driving and distribution impacts on jitter degradation are clearly observed. The worst clock TIE jitter is 2.44 ps at clock output (2.15 ps from PNI simulation), and 3.92 ps at ADC clock port.

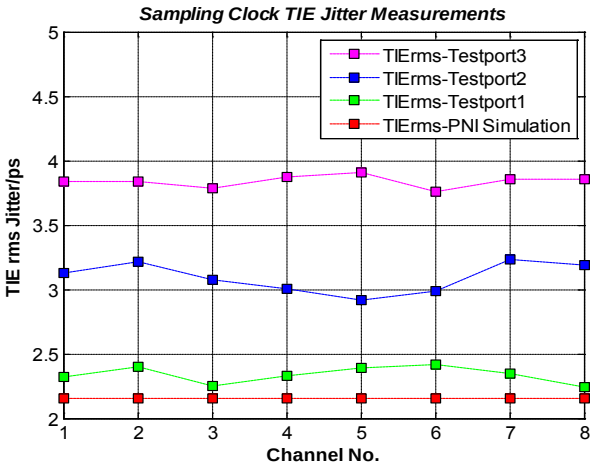

Figure 7: Sampling Clock TIE Jitter Measurements.

The realized jitter-incurred SNR by Eq.8 is 50.92 dB, which is larger than the 47.93 dB requirement. The Effective Number of Bits (ENOB) is used to evaluate the realized SNR [28] as:

$$ENOB = \frac{SNR_{ADC} - 1.76}{6.02} \tag{23}$$

The realized ENOB at various input frequencies are proposed in Fig.8. The worst ENOB of 6.97 bit ENOB occurs at 200.1 MHz, and the realized ADC SNR is 43.60 dB, which is more than the 42.93 dB requirement.

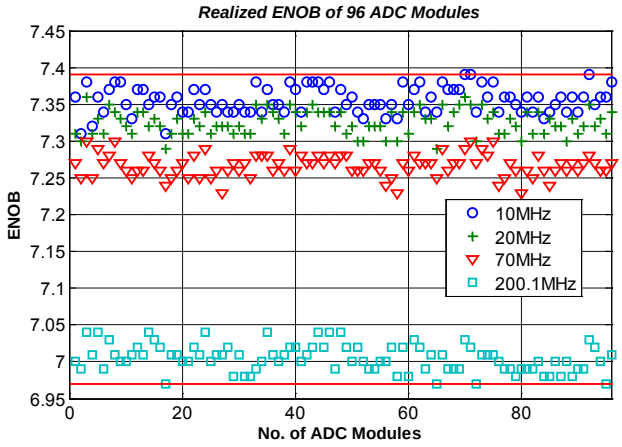

Figure 8: Realized ENOB of 96 ADC Modules.

5.2 Sampling Clock Skew

The raw skew without phase synchronization is given is Fig.9, and the calibrated skew by phase synchronization method is proposed in Fig.10.

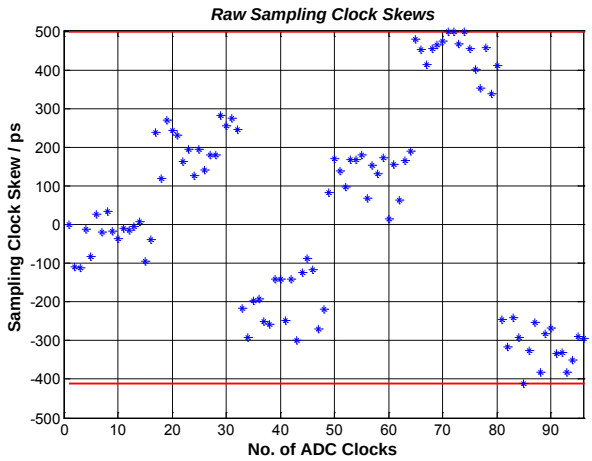

Figure 9: Raw Sampling Clock Skews.

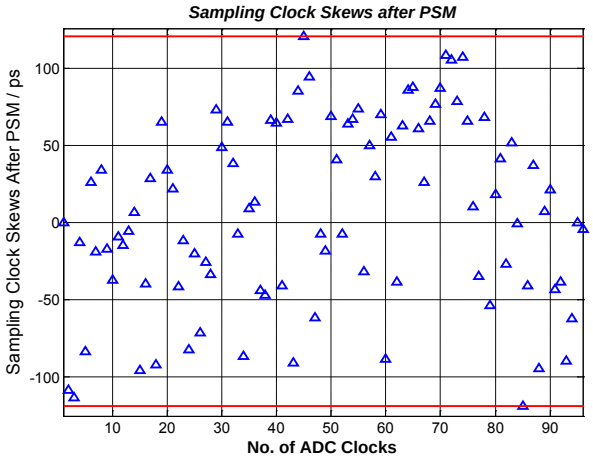

Figure 10: Improved Sampling Clock Skews by PSM

As shown in Fig.9 and 10, sampling clock skew maximum values are improved from $\pm 500\,ps$ to $\pm 120\,ps$, hence the FWF gain error effect is improved from 95.16% to 99.62% to meet the systematic requirement of 1.5%. The 6-channel FWF gain measurement is given in Fig.11 as:

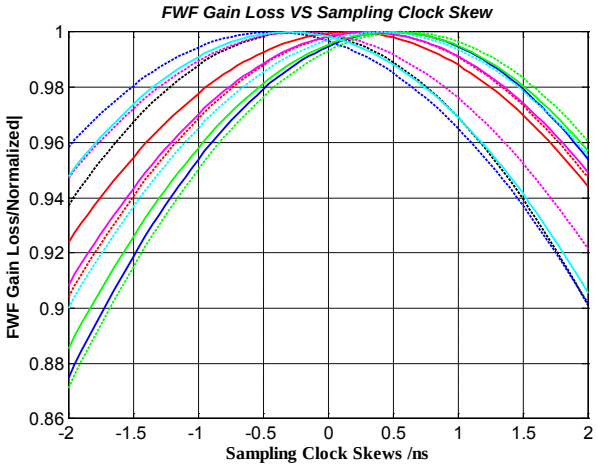

Figure 11: Phase Synchronized Sampling Clock Skews

It can be clearly observed from Fig.10 that FWF correlation loss is within 1%, which satisfies the 1.5% systematic requirement. The overall group delay, including all receiver group delays, is about $\pm 450\,ps$.

6 Conclusion

In this paper, a nontrivial sampling clock imperfection analysis for SAIR systems is proposed. It is first demonstrated that clock jitter and skew both impact FWF, for which clock jitter is a less significant contributor. Secondly, as clock jitter can degrade ADC SNR, for which a rigorous SNR limit is set for jitter control. TIE jitter is proposed as the most appropriate chacterization for clock jitter, and it is simulated by phase noise integration. Thirdly, clock skew reduction by phase synchronization method is proposed. Finally, the clock TIE jitter simulation and tests, the clock skew reductions and the improved FWF results are shown. The contributions of this paper can be summarized as:

1, Although clock jitter has less impact on FWF, its degradation on ADC SNR is clearly shown. A 5 dB SNR margin is imposed on the raw ADC SNR limit to guarantee that jitter has no degradation on SNR. TIE jitter is demonstrated to be the most appropriate parameter to evlauate long-term statistical clock jitter, and can be simulated by phase noise profiles to estimate SNR in advance.

2, As clock skews can degrade FWF correlation efficiency, the PSM is proposed with on-board phase calibrations, and the improved FWF results are shown. PSM is therefore obligatory in SAIR ADC clock chain design.

Compared with previous reports, the sampling clock imperfection analysis method proposed in this paper are nontrivial, and can be applied in the ADC clock design for SAIR or polarimetric systems.

References:

[1] C. S. Ruf, C. T. Swift, A. B. Tanner, et. al. Interferometric Synthetic Aperture Microwave Radiometry for the Remote Sensing of the Earth, *IEEE Transactions on Geoscience and Remote Sensing*, Vol.26, No.5, 1988, pp. 597-611.

[2] C. T. Swift, D. M. Le Vine and C. S. Ruf, Aperture Synthesis Concepts in Microwave Remote Sensing of the Earth, *IEEE Transactions on Microwave Theory and Techniques*, Vol.39, No.12, 1991, pp. 1931-1935.

[3] A. Camps, *Application of interferometric radiometry to earth observation*, Ph.D. Dissertation, Department of Electrical Engineering, Polytechnic University of Catalonia, Spain, 1996.

[4] A. B. Tanner, W. J. Wilson, B. H. Lambrigsten, et.al. Initial Results of the Geostationary Synthetic Thinned Array Radiometer (GeoSTAR) Demonstrator Instrument, *IEEE Transactions on Geoscience and Remote Sensing*, Vol.45, No.7, 2007, pp. 1947-1957.

[5] K. Rautiainen, J. Kainulainen, T. Auer, et.al. Helsinki University of Technology L-Band

Airborne Synthetic Aperture Radiometer, *IEEE Transactions on Geoscience and Remote Sensing*, Vol.46, No.3, 2008, pp. 717-726.

[6] H. J. Lee, H. Park, S. H. Kim, et.al. Evaluation of Imaging Performance for Sub-Y-type Interferometric Synthetic Aperture Radiometer, *PIERS Online*, Vol. 1, No. 5, 2005, pp. 543-546.

[7] C. Zheng, X. Yao, A. Hu and J. Miao, A Passive Millimeter-Wave Imager Used for Concealed Weapon Detection, *Progress In Electromagnetic Research B*, Vol. 46, 2013, pp. 379-397.

[8] C. Zhang, J. Wu, H. Liu, et. al. Near Field Imaging of Synthetic Aperture Radiometer, *PIERS ONLINE*, Vol.4, No.8, 2008, pp. 886-890.

[9] J. Chen, Y. Li, J. Wang, et. al. An Accurate Imaging Algorithm for Millimeter Wave Synthetic Aperture Imaging Radiometer in Near-Field, *Progress In Elegtromagnetic Research*, Vol.141, 2013, pp. 517-535.

[10] J. B. Hagen, Digital-Correlation Techniques in Radio Science, *Radio Science*, Vol.8, No.9, 1973, pp. 775-784.

[11] R. H. Walden, Analog-to-Digital Converter Survey and Analysis, *IEEE Journal of Selected Areas in Communications*, Vol. 17, No.4, 1999, pp. 539-550.

[12] S. M. Hamed, A. H. Khalil, M. B. Abdelhalim, et. al. Testing of N-Stage 1 Bit Per Stage Pipelined ADC Using Test Input Regeneration, *WSEAS Transactions on Circuits and Systems*, Issue 11, Vol.12, Nov.2013, pp. 331-340.

[13] A. B. Tanner and C. T. Swift, Calibration of a Synthetic Aperture Radiometer, *IEEE Transactions on Geoscience and Remote Sensing*, Vol.31, No.1, 1993, pp. 257-267.

[14] C. Zheng, X. Yao, A. Hu, et.al, Closed form Calibration of 1bit/2level Correlator Used for Synthetic Aperture Interferometric Radiometer, *Progress In Electromagnetic Research M*, Vol. 29, 2013, pp. 193-205.

[15] A. Campus, F. Torres, I. Corbella, et.al. Threshold and timing errors of 1bit/2level digital correlators in Earth observation synthec aperture radiometry, *Electronic Letter*, Vol.33, No.9, 1997, pp. 812-814.

[16] W. Kester, *The Data Conversion Handbook (3rd Edition)*, Analog Devices Inc., 2004.

[17] M. A. Fischman and A. W. England, Sensitivity of a 1.4 GHz Direct-Sampling Digital Radiometer, *IEEE Transactions on Geoscience and Remote Sensing*, Vol.37, No.5, 1999, pp. 2172-2180.

[18] N. D. Dalt, M. Harteneck, C. Sandner, et.al. On the Jitter Requirements of the Sampling Clock for Analog-to-Digital Converters, *IEEE Trans. Circuits and Systems-1: Fundamental Theory and Applications*, Vol.49, No.9, 2002. pp. 1354-1360.

[19] J. H. Reed, Software Radio: *A Modern Approach to Radio Engineering (1st Edition)*, NJ: Prentice Hall, 2002.

[20] X. Yao, Z. Li, C. Zheng, et.al. Analysis and Correction of the Inter-channel Mismatch in Synthetic Aperture Radiometer, *TELKOMNIKA Indonesian Journal of Electrical Engineering*, Vol.11, No.12, 2013, pp. 7190-7196.

[21] S. Bregni, Clock Stability Characterization and Measurement in Telecommunications, *IEEE Transactions on Instrumentation and Measurements*, Vol.46, No.6, 1997, pp. 1284-1294.

[22] M. Shinagawa, Y. Akazawa and T. Wakimoto, Jitter Analysis of High-Speed Sampling Systems, *IEEE Journal of Solid-State Circuits*, Vol.25, No.1, 1990, pp. 220-224.

[23] S. Bregni, Measurement of Maximum Time Interval Error for Telecommunications Clock Stability Characterization, *IEEE Transactions on Instrumentation and Measurements*, Vol.45, No.5, 1996, pp. 900-906.

[24] A. Hajimiri, A General Theory of Phase Noise in Electrical Oscillators, *IEEE Journal of Solid-State Circuits*, Vol.33, No.2, 1998, pp. 179-194.

[25] X. Yao, C. Zheng, J. Zhang, et.al. Near-Field Image Reconstruction Algorithm for Passive Millimeter-Wave Imager BHU-2D-U, *Progress In Electromagnetic Research C*, Vol. 45, 2013, pp. 57-71.

[26] C. Zheng, X. Yao, A. Hu, and J. Miao, Initial Results of a Passive Millimeter-Wave Imager Used for Concelaed Weapon Detection BHU-2D, *Progress In Electromagnetic Research C*, Vol.43, 2013, pp. 151-163,

[27] J. Zhang, Z. Li, C. Zheng, et.al. Local Oscillator Uncorrelated Phase Noise Analysis for Millimeter-Wave Passive Imager BHU-2D Frequency Synthesizer, *Progress In Electromagnetic Research B*, Vol.54, 2013, pp. 89-106.

[28] J. R. Piepmeier, A. J. Gasiewski and J. E. Almodovar, Advances in Microwave Digital Radiometry, in *Proc. IGASS 2000*, pp. 2830-2833.