Design of 4-Bit Reversible Shift Registers

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Abstract: - In recent years, Reversible logic has emerged as a major area of research due to its ability to reduce the power dissipation which is the main requirement in the low power digital circuit design. It has wide applications like low power CMOS design, Nano-technology, Digital signal processing, Communication, DNA computing and Optical computing. In this paper, we have proposed a new 4x4 reversible gate and it is being used to realize the D-latch and D-flip-flop in the reversible domain. The transistor representation of the proposed reversible D-flip-flop is implemented using adiabatic logic. Also a 4-bit reversible SISO, SIPO, PISO and PIPO shift registers has been designed using the proposed reversible d-flip-flop. Proposed circuits have been simulated using Modelsim and synthesized using Xilinx Virtex5vlx30tff665-3.

Key-Words: - Reversible D-Latch, Reversible D-Flip-Flop, Reversible Shift Registers, FPGA.

1 Introduction

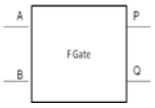
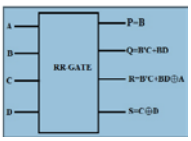
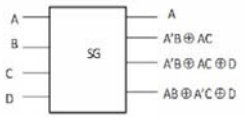
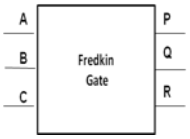
Reduction of the power dissipation remains as an important goal in the VLSI circuit design for many years.. Conventionally digital circuits have been implemented using the basic logic gates which were irreversible in nature. These irreversible gates produce energy loss due to the information bits lost during the operation. Information loss occurs because total number of output signals generated is less than total number of input signals applied. Thus, conventional combinational logic circuits dissipate heat for every bit of information that is lost during their operation. In 1961, R.Landauer, proved that a single bit of information loss dissipates KTlni2 joules of energy where K is the Boltzmann's constant and T is the temperature at which the computation is performed. In 1973, Bennett showed that in order to avoid energy loss it is necessary that all the computations have to be performed in a reversible way [2]. Thus to avoid power dissipation, circuits must be constructed from reversible logic gates. Thus every future technology has to use reversible gates in order to reduce power dissipation. Perkowski et .al.'s states [3] " every future technology will have to use reversible gates in order to reduce power" This has led many people to pursue research in the area of reversible logic. A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and if there is a one – to –one correspondence between its input and out put assignment. A reversible circuit maps each input vector, into a unique output vector and vice versa. Thus reversible logic has application in various research areas such as digital signal processing, quantum computing, low power CMOS design, communication, bioinformatics and nanotechnology-based systems [4]. A reversible logic circuit should be designed using minimum number of reversible logic gates, with minimum number of garbage outputs and with minimum number of constant inputs [5-7]. The output which cannot be used further for computation process is known as garbage output. The input that is added to an n xk function to make it reversible is called constant input [8]. The quantum cost of a reversible or quantum circuit is defined as the number of 1×1 or 2×2 gates used to implement the circuit. The major objective of a reversible logic design is to minimize the quantum cost and the number of garbage outputs [9]. Hence, one of the major issues in reversible circuit design is garbage minimization to minimise the power dissipation. Another significant criterion in designing a reversible logic circuit is to minimize the number of reversible gates used [10]. It has been shown that both the combinational as well as the sequential circuits can be designed using reversible logic gates. However the design of sequential circuits is more complex than that of a combinational circuit. In this paper we are presenting a new 4x4 reversible logic gate and the realization of reversible D-latch and reversible D-flip-flop using the proposed gate. The transistor representation of the proposed circuit is better in terms of transistor count. The proposed work is then

compared with the existing reversible sequential circuits. Also, a 4-bit reversible Serial in Serial out, 4-bit Reversible Serial in Parallel out, 4-bit Reversible Parallel in Serial out and a 4-bit Reversible Parallel in Parallel out shift registers are designed using the proposed D-flip-flop. All the proposed circuits have been implemented using VHDL and simulated using Modelsim. The paper is organized as follows: Section 2 is an overview of the reversible gates. Section 3 deals with the survey of the existing work. Section 4 represents the design of the proposed reversible gate. Section 5 represents the transistor implementation of the proposed gate using adiabatic logic. Section 6 describes the proposed design of a D-Latch and a D-flip-flop. Section 7 describes the design of all the four types of 4-bit reversible shift register. Simulation results of the proposed design are presented in section 9 and conclusions are contained in section 10.

2 Reversible Logic Gates

Some of the important reversible logic gates are Feynman gate, RR gate, and SG gate. Brief introduction of these gates are as shown in Table 1.

Table 1. Reversible Logic Gates

SI.No	Gate	Block Diagram	Function
1.	Feynman		P = A Q = A⊕B
2.	RR		P = B Q = B'C+BD R = B'C+BD⊕A S = C ⊕D
3.	SG		P =A Q = A'B ⊕C R = A'B⊕AC⊕D R = AB⊕A'C⊕D
4.	Toffoli		P = A Q = B R = AB⊕C
5.	Fredkin		P = A Q = A'B + AC R = AB + A'C

3 Literature Survey

H.Thapliyal, M.B.Srinivas and Mark Zwolinski [11]proposed a reversible D-flip-flop using New gate and Feynman gate. The drawback of this work is that it requires more number of reversible gates and produces more number of garage outputs. As the number of reversible gates required is more, it also increases the quantum cost of their flip-flop. H.Thapliyal and M.B.Srinivas [12] proposed a reversible D-latch using two Fredkin gates. The drawback of their work is the quantum cost to realize a reversible D-latch with both the outputs Q and Q' is 10. However, to realize a reversible master-slave D-flip-flop 5 Fredkin gates are used which increases the quantum cost. Rice [13] proposed a reversible SR latch and all the other latches were designed as the sub-units from reversible RS latch as a part of master-slave flip-flops. Thapliyal and Vinod [14] proposed the designs of reversible latches and flip flops. The proposed designs were shown to be better than the designs presented in Rice [13] in terms of the number of reversible gates and garbage outputs. The quantum cost of the reversible D-latch proposed by Thapliyal and Vinod is 10. H.Thapliyal and N. Ranganathan [15] proposed a negative enabled reversible D - Latch using Fredkin gate. The advantage of this work is that it does not require the inversion of CLK pulse to realize the master-slave D-flip-flop. To realize both the outputs Q and Q', it requires 1 Fredkin gate and 2 Feynman gates and the quantum cost of their implementation is 7. The transistor implementation is not addressed in this work. Md. Selim Al Mamun, Indrani Mandal, Md. Hasanuzzaman [16] proposed a reversible D-latch using MG-1 gate. In this work the number of XOR operations involved in realizing a MG-1 gate is more which will increase the transistor count. S.Ranjith, T.Ravi and E. Logashanmugam [17] proposed a reversible RR gate using which a reversible D-Flip-flop has been realized. The drawback of their work is that to realize a master slave flip-flop an additional reversible gate is required to produce the complement of the clock signal and further to realize the flip-flop with both the outputs Q and Q' one more reversible gate is in need to produce Q'. Thus, the number of reversible gates required is more which in addition will

increase the transistor count. Prashant R. Yelekar and Prof. Sujata S. Chiwande [18] proposed a reversible D-Latch and T-flip-flop using SG gate. Again in this work to implement a master-slave D-flip flop an additional reversible gate is required to complement the clock pulse and also the number of XOR operations involved in realizing a SG gate is more which will increase the transistor count. To minimize the transistor count, we have proposed a new reversible gate which is a modified form of the reversible R R gate which can be used for the realization D -Latch and D -flip-flop with less number of transistor count.

4 Proposed Work

4.1 Proposed Reversible gate AS

The logic diagram of the proposed reversible gate AS is as shown in figure. The proposed reversible gate AS is a 4 x4 reversible gate with inputs(A,B,C,D) and with outputs A', AB + A'C, D⊕(AB + A'C) and B ⊕C.

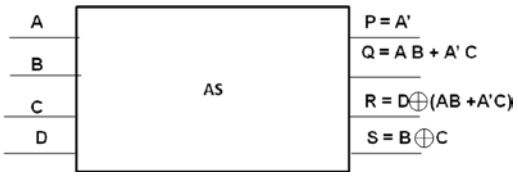


Fig.1 Proposed 4x4 AS Reversible Gate.

The truth table for the corresponding gate is as shown in Table 2.

Table 2. Truth Table of AS Reversible Gate

A	B	C	D	P	Q	R	S
0	0	0	0	1	0	0	0
0	0	0	1	1	0	1	0
0	0	1	0	1	1	1	1
0	0	1	1	1	1	0	1
0	1	0	0	1	0	0	1
0	1	0	1	1	0	1	1
0	1	1	0	1	1	1	0
0	1	1	1	1	1	0	0
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	1	1
1	0	1	1	0	1	0	1
1	1	0	0	0	0	0	1
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	0	1	0	0

A closer look at the Truth Table reveals that the input pattern corresponding to a specific output pattern can be uniquely determined and thereby maintaining that there is a one-to-one correspondence between the input vector and the output vector. In this gate the input vector is given by IV=(A,B,C,D) and the corresponding output vector is OV=(P,Q,R,S). The quantum cost of the proposed reversible gate AS is 6. The quantum cost represents the number of 1x1 and 2x2 primitive gates used in the realization of the proposed reversible gate AS.

4.1.1 Realization of the Classical Operations using the Proposed Reversible Gate AS

The proposed reversible gate AS can implement OR, AND, XOR, NOT and COPY operation. Also since AND, OR and NOT operation can be implemented justifies the aforesaid because any boolean function can be materialized in product – of – sum or sum – of – products form. Also the COPY operation is an important operation which can be realized using the proposed reversible gate AS.

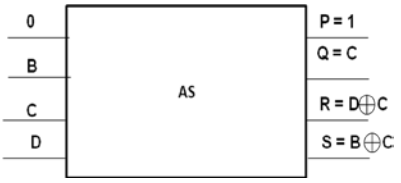


Fig. 2 Reversible Gate AS implementing reversible XOR and COPY operation.

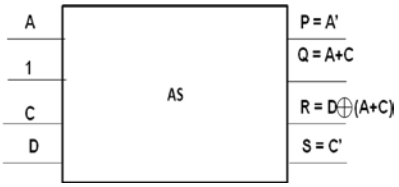


Fig. 3 Reversible Gate AS implementing reversible OR, NOT and XOR operation.

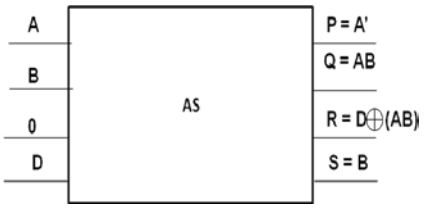


Fig. 4 Reversible Gate AS implementing reversible AND, NOT and COPY operation.

5 Transistor Implementation of the Proposed Reversible Gate using Adiabatic Method

Conventional CMOS logic circuits operate at a constant voltage Vdd and the amount of energy dissipated per transition due to pull-up and pull-down is $CVdd^2/2$. ---------- (1)

Energy is used only once in CMOS logic circuits. Whereas adiabatic logic circuits are powered by a power clock pulse and the amount of energy per transition over the time period T is $i^2(t)$ R T,----- (2) where i(t) – current through the capacitor, C.

From an RC circuit, the current through the capacitor can be expressed as i(t) = C dv/dt. Let the input signal v(t) makes a transition from logic 0 to Vdd over the time T. Thus, $i^2(t) = C^2 Vdd^2 / T^2$

Thus, the amount of energy per transition is RC^2Vdd^2/T. In CMOS logic circuits, the amount of energy dissipated depends only on C and Vdd while in adiabatic circuits it depends on the size of transistor as well as on the time T. To dissipate less energy T > 2RC in adiabatic circuits. Thus, adiabatic circuits are low power circuits which use reversible logic to conserve energy.

Adiabatic logic families can be implemented either using efficient charge recovery logic (ECRL)or by positive feedback adiabatic logic(PFAL). ECRL implements the logic function with less number of transistors when compared to PFAL technique. PFAL technique implements the function with less power dissipation at the expense of transistor count. In both the techniques, the input signal must be phase shifted by 90° with respect to the power clock. In adiabatic systems, more than one power clock is required. We have proposed the transistor representation of the proposed gate AS using ECRL technique. In our work, four phases of power clock is used to achieve the synchronization and the input signal is phase shifted by 90° with respect to the power clock.

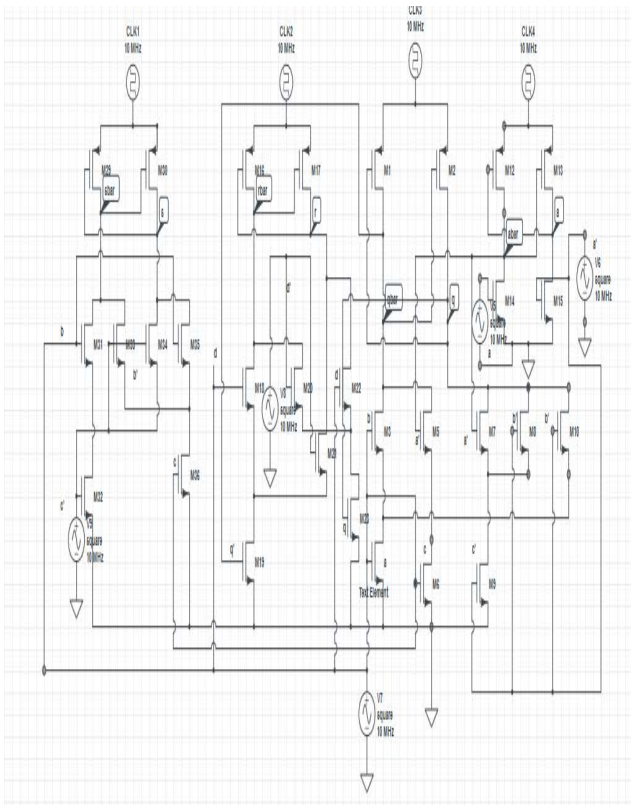


Fig. 5 Transistor Representation of Proposed Reversible Gate AS.

The transistor representation of proposed reversible gate AS is shown in figure 5. When the input a is 0 and a' is 1, the transistor M15 conducts and pull down the node a to 0. Thus, the node a represents the function pbar. Since node a is 0, the transistor M12 conducts and the node abar follows the signal clock CLK4 which represents the function p. Thus, the transistors M12, M13, M14 and M15 represent an inverter. The transistors M3, M4, M5 and M6 represent the function ab + a'c i.e the function q. While the transistors M7, M8, M9 and M10 represent the function (ab + a'c)' i.e qbar. The transistors M18, M19 and M20 represent the function dqbar + d'q i.e the function s. While the transistors M21, M22 and M23 represent the function dq + d'qbar i.e sbar. The transistors M31, M32 and M33 represent the function bc' + b'c i.e

the function r. While the transistors M34, M35 and M36 represent its complement i.e bc + b'c'. Thus, a total of 30 transistors are required to implement the reversible gate AS. Adiabatic logic introduces more number of transistors but it produces both the signal and its complement. The average power consumed by the circuit at a frequency of 10MHz is 72mW with an operating voltage of 2V.

6 Proposed Design of Reversible D-Latch and Reversible D-Flip-Flop

6.1 Proposed Reversible D-Latch

To minimise the transistor count, we have implemented a reversible D-Latch using the proposed reversible gate AS. The symbolic representation of the proposed reversible D-Latch with the un-complemented output is shown in figure 6.

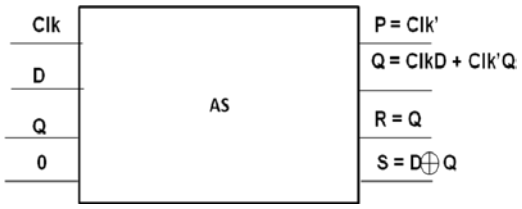


Fig. 6 Symbolic Representation of Proposed Reversible D-Latch with the output Q Using Reversible Gate AS.

From reversible gate AS, when D is 0, A= Clk, B = D(Data Input), and C = Q(Previous Output) P = Clk', R = Q, S = D XOR Q and Q = ClkD + Clk'Q which represents the Boolean Expression of D-Latch. The output P = Clk' can be used to realize the master-slave D-flip-flop and S = D XOR Q represent the garbage output. Thus, the proposed Reversible D-Latch requires 1 reversible gate. The circuit accepts1 constant input and produces one garbage output which is an optimized circuit. The number of transistors required to implement the proposed circuit is 30.

The symbolic representation of the proposed reversible D-Latch with both un-complemented and complemented outputs is shown in figure 7.

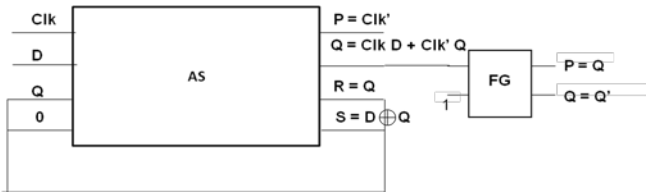


Fig. 7 Symbolic Representation of Proposed Reversible D-Latch with both the outputs Q and Q' Using Reversible Gate AS and Feynman Gate.

To realize both the outputs Q and Q', two reversible gates are required. To produce the complemented value of the signal Q, Feynman gate is used. The circuit accepts two constant inputs and produces one garbage output. The number of transistors required to realize the proposed reversible gate3 is 30 and to realize the Feynman gate eight transistors are required. Thus, a total of 38 transistors are required to realize the reversible D-Latch with both the outputs Q and Q'. Table 3 shows the number of gates required to realize the reversible D-Latch with both Q and Q' using Reversible Gate AS and Feynman gate.

The reversible D-latch in [17] is a partially reversible design that uses complimentary pass transistor logic, which is an acceptable approach

SI.No	Number of Gates Required	Quantum Cost	Number of Transistors Required	Number of garbage outputs produced
1.Existing Work[12]	2	10	Not given	1
2.Existing Work[14]	2	10	Not given	2
3.Existing Work[15]	2	7	Not given	2
5..Existing Work[16]	1	10	Not given	1
6..Existing Work[17]	2	Not given	30 (uses conventional CMOS inverters)	1
7..Existing Work[18]	2	Not given	28 (using non-adiabatic)	1
8. Proposed Work	2	6	38 (using adiabatic logic)	2

Table 3. Number of gates required to realize the Reversible D-Latch with both the outputs Q and Q'.

(although they do use conventional inverters at points). The circuits in [18] use DeVos pass transistor logic (but are not still completely adiabatic). From table 3, it is inferred that the number of transistors required to implement the D-latch[18] with both the outputs Q and Q' using non-adiabatic logic is 28. However, if the same is implemented using adiabatic logic, the number of transistors required is 44 which is more when compared with our proposed work.

6.2 Proposed D-Flip-Flop

The symbolic representation of the master-slave D-flip-flop with both the outputs Q and Q' is shown in figure 8.

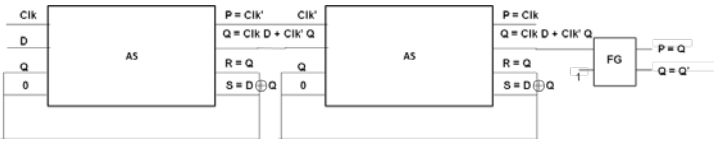


Fig. 8 Symbolic Representation of Proposed Reversible D-Flip-Flop with both the outputs Q and Q' Using Reversible Gate AS and Feynman Gate.

Thus two reversible Gates AS are required to realize the master-slave D-flip-Flop. One Feynman gate is used to produce the true and the complement value of the signal Q. The circuit operation is straight forward. The first reversible gate AS functions as master. The second reversible gate AS functions as slave. Master is activated when the clock makes a transition from low to high and slave gets activated when the clock goes from high to low. When the Clock pulse makes a transition from low to high, master passes the D value to the signal Q on the first gate AS. The output produced by the master is given as the data input to the slave. Since the slave is triggered by the signal clk', when clock goes from 0 to 1, the slave retains the previous value. When the clock makes a transition from high to low, master retains the previous value while the slave passes the data passed by the master to the signal Q on the signal Q of the second reversible gate AS. One input for the Feynman gate is Q and the second input is 1. Thus it produces a copy of the signal Q and its complement Q'. The output P from the second reversible gate AS can be used to realize the shift register. However, the output S from both the reversible gates AS is unused and hence the number of garbage outputs is 2. The circuit accepts three constant inputs. The symbolic representation of the reversible D-Flip-Flop is as shown in figure 9.

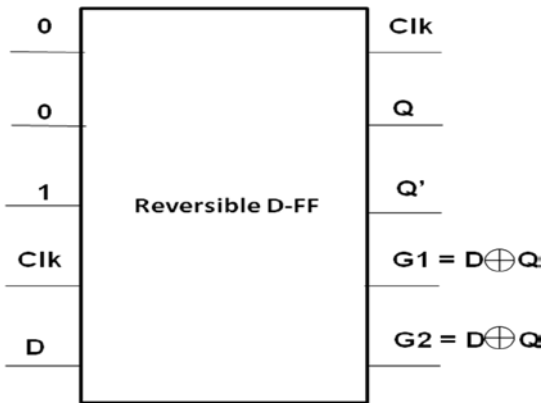


Fig. 9 Symbolic Representation of Proposed Reversible D-Flip-Flop with both the outputs Q and Q' Using Reversible Gate AS and Feynman Gate.

Table 4 shows the number of gates required to implement the proposed Reversible D-Flip-Flop.

Table 4. Number of gates required to implement the proposed Reversible D-Flip-Flop.

SI.No	Number of Gates Required	Number of Transistors Required	Number of garbage outputs produced
1.Existing Work[18]	4	48(using non-adiabatic logic)	2
2.Proposed Work	3	68 (using adiabatic logic)	2

From table 4, it is inferred with respect to the existing work[18] the number of transistors required to realize the reversible D-Flip-flop using Sayem Gate is 80 i.e., using adiabatic logic which is more when compared with the proposed reversible D-Flip-Flop using modified RR gate. However, the number of garbage outputs produced remains the same in both the existing and the proposed work.

7 Realization of Shift Registers

A shift register is a cascade of flipflop, sharing the same clock, in which the output of each flip-flop is connected to the "data" input of the next flip-flop in the chain, resulting in a circuit that shifts by one position the "bit array" stored in it, shifting in the data present at its input and shifting out the last bit in the array, at each transition of the clock input. More generally, Shift registers can have both parallel and serial inputs and outputs. These are often configured as serial-in, parallel-out (SIPO) or as parallel-in, serial-out (PISO). There are also types that have both serial and parallel input and types with serial and parallel output.

7.1 Realization of Serial In Serial Out Shift Register

The serial in /serial out shift register accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. The input data is then applied sequentially to the D input of the first flip-flop on the left .During each clock pulse, one bit is transmitted from left to right. A basic four-bit shift register can be constructed using four D flip-flops. The operation of the circuit is as follows. The input data is then applied sequentially to the D input of the first flip-flop on the left. During each clock pulse, one bit is transmitted from left to right.

A 4 -Bit Reversible Serial in Serial out Shift Register is realized using the proposed D-Flip-Flop. Thus, 4 Reversible D-Flip-Flops are connected in cascade in series to implement the 4-bit reversible shift register as shown in figure 10.

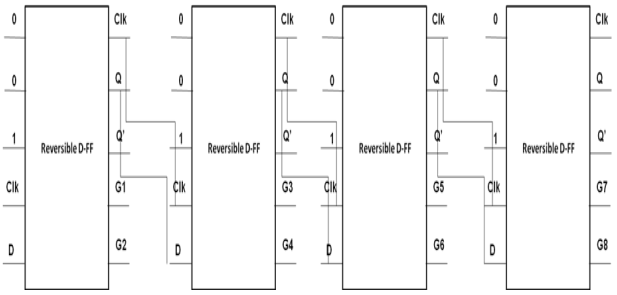


Fig. 10 Symbolic Representation of Proposed Reversible4-Bit Serial In Serial Out Shift Register.

Table 5 shows the number of reversible gates required to implement the reversible 4-bit serial in serial out shift register.

Table 5. Number of gates required to implement a 4-bit Reversible Serial in Serial out Shift Register.

SI.No	Number of Gates Required	Number of garbage outputs produced
1.Proposed Work	12	8

7.2 Realization of Serial In Parallel Out Shift Register

In this type of shift register, data bits are entered serially that is, one bit at a time on a single line. It produces the stored information on its output in parallel form. The input data is then applied sequentially to the D input of the first flip-flop on the left .During each clock pulse, one bit is transmitted from left to right. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. A construction of a four-bit serial in - parallel out register is shown in figure 11.

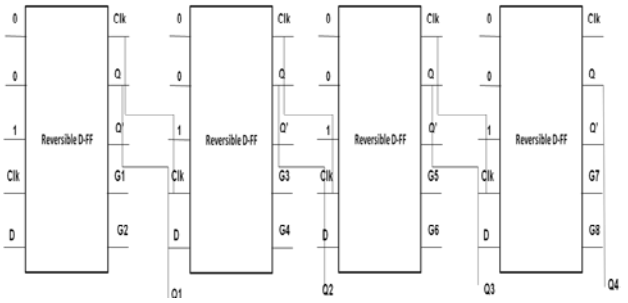


Fig. 11 Symbolic Representation of Proposed Reversible4-Bit Serial In Parallel Out Shift Register.

Table 6 shows the number of reversible gates required to implement the reversible 4-bit Serial in Parallel out shift register.

Table 6. Number of gates required to implement a 4-bit Reversible Serial in Parallel out Shift Register.

SI.No	Number of Gates Required	Number of garbage out puts produced
1.Proposed Work	12	8

7.3 Realization of Parallel In Parallel Out Shift Register

For parallel in - parallel out shift registers, all data bits appear on the parallel outputs immediately following the simultaneous entry of the data bits. Figure 12 shows the 4-bit Reversible Parallel In Parallel Out Shift Register.

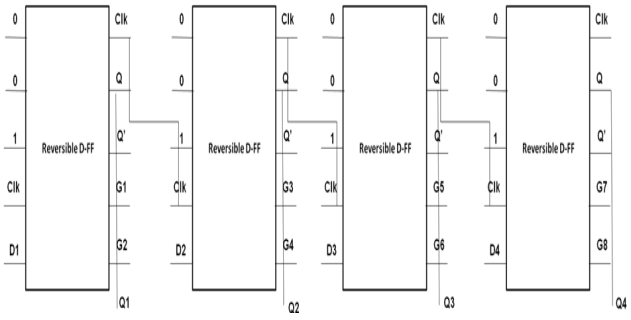


Fig. 12 Symbolic Representation of Proposed Reversible4-Bit Parallel In Parallel Out Shift Register.

Table 7 shows the number of reversible gates required to implement the reversible 4-bit Parallel in Parallel out shift register.

Table 7. Number of gates required to implement a 4-bit Reversible Parallel in Parallel out Shift Register.

SI.No	Number of Gates Required	Number of garbage outputs produced
1.Proposed Work	12	8

7.4 Realization of Parallel In Serial Out Shift Register

Figure 13 shows the realization of the reversible 4 – bit Parallel in Serial Out Shift Register. To write the new data to the register, W/S line must be held high. To shift the data, W/S line should be low. Fredkin gate is used as the multiplexer to select whether to shift the data or to load a new data.

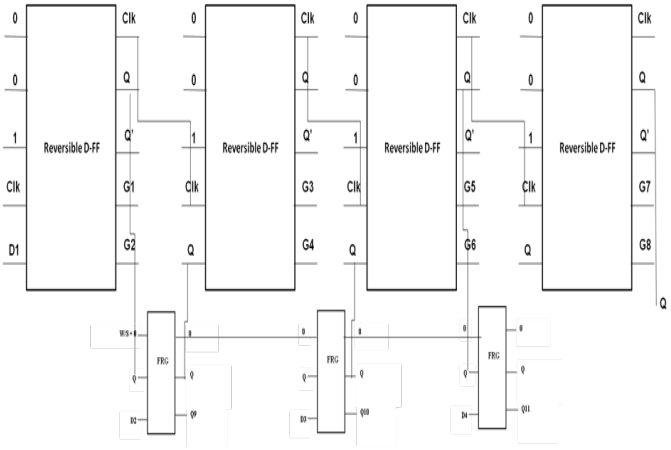


Fig. 13 Symbolic Representation of Proposed Reversible4-Bit Parallel In Serial Out Shift Register.

Table 8 shows the number of reversible gates required to implement the reversible 4-bit Parallel in Serial out shift register.

Table 8. Number of gates required to implement a 4-bit Reversible Parallel in Serial out Shift Register.

SI.No	Number of Gates Required	Number of garbage out puts produced
1.Proposed Work	15	11

9 Simulation Results

The entire unit was functionally verified. A test-bench is used to generate the stimulus and applies it to the implemented reversible d-flip-flop, Serial in Serial out Shift Register, Serial in Parallel Out Shift Register, Parallel in Parallel out Shift Register. The design was simulated using Modelsim and synthesized using Xilinx Virtex5 and the power is estimated using Xilinx Power Estimator tool.

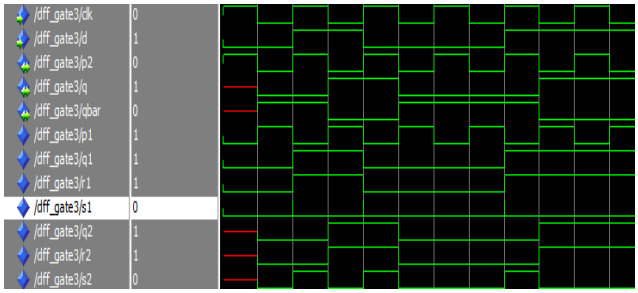


Fig. 14 Simulation Result of the Proposed D-Flip-Flop Using Reversible Gate AS.

In figure 14, clk, d represents the input signals and q, qbar represents the output signals. From the figure whenever clk makes a transition from logic 1 to logic 0, whatever is the d value that is reflected in the output signal q.

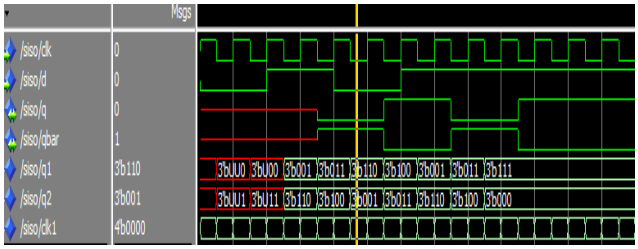


Fig. 15 Simulation Result of the Proposed Reversible 4-Bit Serial In Serial Out Shift Register.

Figure 15 shows the simulation result of the Reversible 4-bit Serial in Serial out Shift Register where clk, dr epresents the input and q, qbar represents the output. From the figure, the first input is available on the output signal q during the fourth clk transition from logic1 to logic 0.

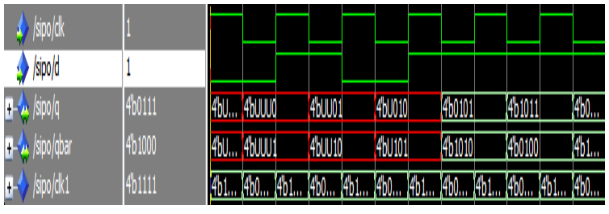


Fig. 16 Simulation Result of the Proposed Reversible 4-Bit Serial In Parallel Out Shift Register.

Figure 16 shows the simulation result of the Reversible 4-bit Serial in Parallel out Shift Register where clk, dr epresents the input and q, qbar represents the output. From the figure, the first input is available on the output signal q during the first clk transition from logic1 to logic 0. The 4-bit input 0101 is a vailable on the output during the fourth clk transition from logic 1 to logic 0.

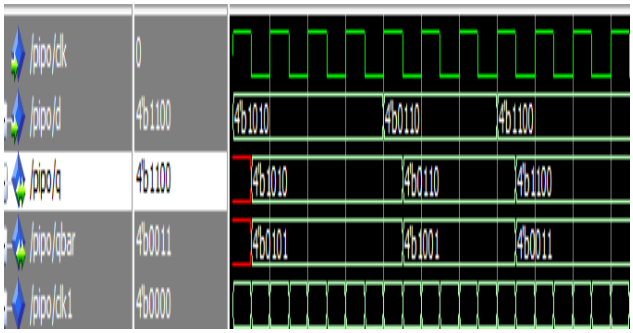


Fig. 17 Simulation Result of the Proposed Reversible 4-Bit Parallel In Parallel Out Shift Register.

Figure 17 shows the simulation result of the Reversible 4-bit Parallel in Parallel out Shift Register where clk, d represents the input and q, qbar represents the output. From the figure, the 4-bit input 1010 is available on the output during the first clk transition from logic 1 to logic 0.

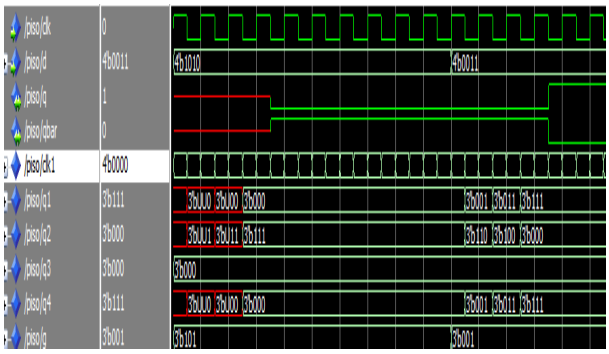


Fig. 18 Simulation Result of the Proposed Reversible 4-Bit Parallel In Serial Out Shift Register.

Figure 18 shows the simulation result of the Reversible 4-bit Parallel in Serial out Shift Register where clk, dr epresents the input and q, qbar represents the output. From the figure, for the 4-bit input 1010 the first bit is available on the output

signal during the fourth clk transition from logic 1 to logic 0. In the realization of the proposed shift register, the previous bit is loaded as the input to the next flip-flop and hence the first bit is shifted serially.

10 Conclusion

In this paper an optimized reversible d-latch and a d-flip-flop is presented with the proposed new Reversible Gate AS with lesser number of transistors. The proposed D-flip-flop can generate both the outputs Q and Q'. Then a 4-bit reversible serial in serial out, serial in parallel out, parallel in serial out and parallel in parallel out shift register is designed using the proposed reversible d-flip-flop. The design is very useful for the future computing techniques like ultra low power digital circuits and quantum computers. The proposed d-flip-flop is highly optimized in terms of number of transistors.

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