Stabilization of DC Link Voltage Using Redundant Vectors for Five-Level Diode Clamped Shunt Active Power Filter

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Abstract: - In this paper, the control of DC link capacitor voltages of five-level diode clamped Active Power Filter (APF) using simplified Space Vector Pulse Width Modulation (SVPWM) associated with the redundant vectors of this topology is proposed. The space vector diagram of the five-level inverter is simplified into that of three-level inverter. In turn, the three-level inverter space vector diagram is simplified into that of two-level inverter. Thus, the algorithm of five-level SVPWM becomes very similar to that of conventional two-level inverter SVPWM. Concerning the self stabilization of dc link capacitor voltages, on the base of position of reference voltage vector in space vector diagram, we explain how to choose switching states that will be used to generate the output voltages. The redundancies of some switching states are thoughtfully used to cancel imbalance of dc link capacitor voltages, on the base of a closed loop that use measurements of input and output currents of the APF. The performance of the proposed redundant vector algorithm associated with sliding regulator used to control the shunt APF is illustrated through the compensation of harmonic currents and reactive power produced by a non-linear load in medium voltage network.

Key-Words: - Active Power Filter, Harmonic current, Five-level inverter, Space Vector Pulse Width Modulation (SVPWM), DC source balancing, Redundant vectors

1 Introduction

The application of power electronics devices such as arc furnaces, adjustable speed drives, computer power supplies etc. are some typical non-linear characteristic loads used in most of the industrial applications and are increasing rapidly due to technical improvements of semiconductor devices, digital controller and flexibility in controlling the power usage. The use of the above power electronic devices in power distribution system gives rise to harmonics and reactive power disturbances. The harmonics and reactive power cause a number of undesirable effects like heating, equipment damage and electromagnetic interference effects in the power system.

In high power applications, the multilevel inverters are more adequate compared to the conventional two-level structure. The many inherent benefits of these structures have led to their recent increased interest amongst both industry and utilities.

The unbalance of the different DC voltage sources of the multi levels inverters constitutes the major limitation for the use of these power converters. Several methods are proposed to suppress the unbalance of neutral point potential. Some of these methods are based on adding a zero sequence or a dc-offset to output voltage [1,2]. In [3,4], power electronics circuitry is added to redistribute charges between capacitors. A method based on minimizing a quadratic parameter that depends on capacitor voltages is presented in [5]. This quadratic parameter is positively defined and reach zero when the two capacitors have the same voltage. Some other works use a converter-inverter cascade, and apply automatic control methods, such as fuzzy logic control [6] or sliding mode control [7] to this cascade. In this work we use a simple closed loop method which makes a continuous measurement of output current and difference between capacitors

voltages, and choose the redundant vector on the basis of these measurements.

In this paper, first part is dedicated to the presentation of the model of the three phases five-level diode clamped voltage source inverter (VSI) with its space vector diagram. In the second part, the proposed simplified SVPWM control method is presented [8]. After that the multi DC bus voltages balancing method using redundant vectors is detailed. This APF is applied for the enhancement of medium voltage network power quality by compensation of harmonic currents produced by an unbalanced nonlinear load (Figure 1). At the end the simulation results of sliding mode controlled APF are presented.

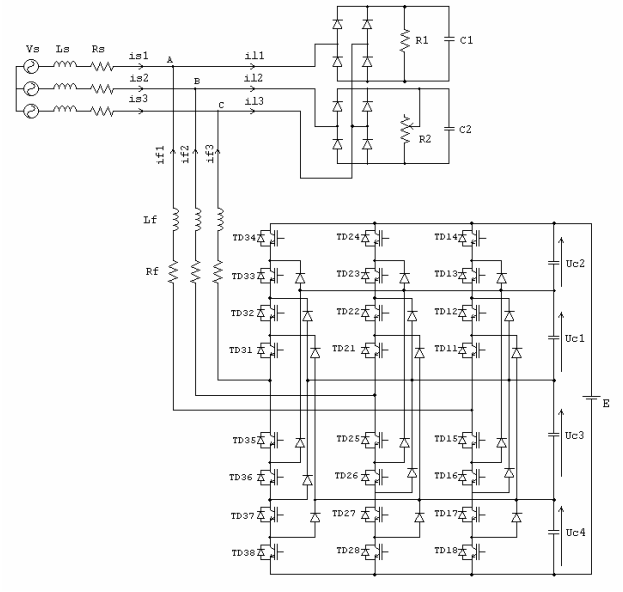

Fig.1 Synoptic diagram of application of shunt APF on power supply fed a non-linear load

2. Modelling and control of five-level Diode Clamped VSI

2. 1. Modelling of five-level Diode Clamped VSI

Structure of five-level diode clamped inverter is shown in Figure 2. Each leg is composed of four upper and lower switches with anti-parallel diodes. Four series dc-link capacitors split the dc-bus voltage in half. The necessary conditions for the switching states for the five-level inverter are that the dc-link capacitors should not be shorted, and the output current should be continuous [9].

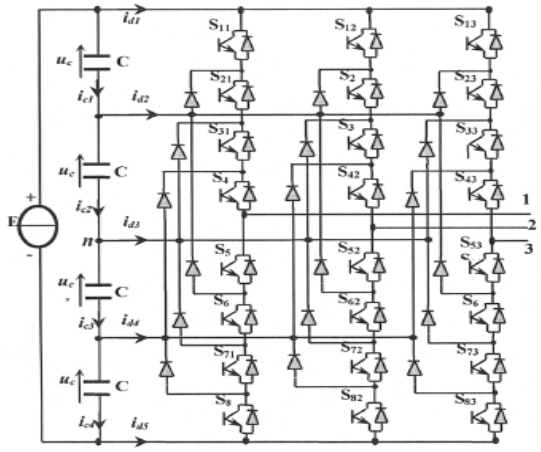

Fig.2 Five-level diode clamped voltage source inverter

Each leg of the inverter has five possible switching states (Tab.1):

State P2: The upper switching devices S1x, S2x, S3x and S4x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = E/2.

State P1: The switching devices S2x, S3x, S4x and S5x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = E/4.

State 0: The switching devices S3x, S4x, S5x and S6x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = 0.

State N1: The switching devices S4x, S5x, S6x and S7x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = -E/4.

State N2: The lower switching devices S5x, S6x, S7x and S8x (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage Vxn = -E/2.

For each switching device Sij (i = 1- 8, j = 1,2 or 3), we define a Boolean function Fij as:

Table 1 States of five-level inverter

Switching Symbols	Switching States								Output Voltage
	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	S_{i7}	S_{i8}	
P2	ON	ON	ON	ON	OFF	OFF	OFF	OFF	E/2
P1	OFF	ON	ON	ON	ON	OFF	OFF	OFF	E/4
O	OFF	OFF	ON	ON	ON	ON	OFF	OFF	0
N1	OFF	OFF	OFF	ON	ON	ON	ON	OFF	-E/4
N2	OFF	OFF	OFF	OFF	ON	ON	ON	ON	-E/2

$$F_{ij}=\begin{cases}1 & \text{if } S_{ij} \text{ is ON}\\ 0 & \text{if } S_{ij} \text{ is OFF}\end{cases} \quad (1)$$

The complementarities between upper and lower switching devices of each leg impose the following equations:

$$F_{ij}=1-F_{(i-4)j} \quad i=5 \text{ to } 8 \quad (2)$$

For each leg of the inverter, we define five connection functions (one for each switching state) as:

$$\begin{cases} F_{c1j}=F_{1j}F_{2j}F_{3j}F_{4j} \\ F_{c2j}=F_{2j}F_{3j}F_{4j}F_{5j} \\ F_{c3j}=F_{3j}F_{4j}F_{5j}F_{6j} \quad j=1,2 \text{ or } 3 \\ F_{c4j}=F_{4j}F_{5j}F_{6j}F_{7j} \\ F_{c5j}=F_{5j}F_{6j}F_{7j}F_{8j} \end{cases} \quad (3)$$

The output phase voltages with reference to neutral point (n) of DC bus voltage are:

$$\begin{pmatrix} V_{1n} \\ V_{2n} \\ V_{3n} \end{pmatrix} = \begin{pmatrix} F_{c11} & F_{c21} & F_{c31} & F_{c41} & F_{c51} \\ F_{c12} & F_{c22} & F_{c32} & F_{c42} & F_{c52} \\ F_{c13} & F_{c23} & F_{c33} & F_{c43} & F_{c53} \end{pmatrix} \begin{pmatrix} E/2 \\ E/4 \\ 0 \\ -E/4 \\ -E/2 \end{pmatrix} \quad (4)$$

Figure 3 shows the space vector diagram for five-level inverter.

Since five kinds of switching states exist in each leg, this converter has 125 switching states. The output voltage vector can take only 61 discrete positions in the diagram because some switches state are redundant and create the same space vector.

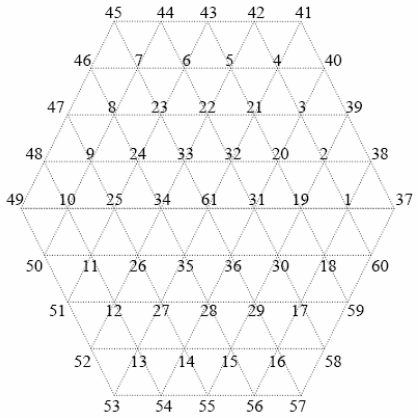

Fig.3 Space vector diagram of a five-level inverter

2. 2. Simplified SVPWM for five-level inverter

The space vector diagram of a five-level inverter can be thought that is composed of six hexagons that are the space vector diagrams of the three-level inverters [10]. Each of these six hexagons, constituting the space vector diagram of a three level inverter, centers on the six apexes of the medium hexagon as shown in Figure 4.

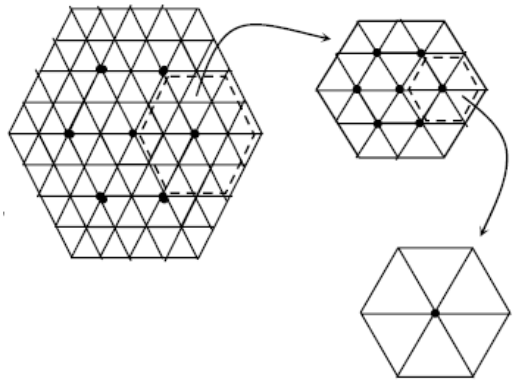

Fig.4 Simplification of a five-level space vector diagram into two-level space vector diagram

To simplify into the space vector diagram of a three-level inverter, two steps have to be taken.

Firstly, from the location of a given reference voltage, one hexagon has to be selected among the six hexagons. There exist some regions that are overlapped by two adjacent hexagons. These regions will be divided in equality between the two hexagons as shown in Figure 5. Each hexagon is identified by a number S defined in equation (5).

$$s=\begin{cases} 1 & if \quad -\pi/6<\theta<\pi/6 \\ 2 & if \quad \pi/6<\theta<\pi/2 \\ 3 & if \quad \pi/2<\theta<5\pi/6 \\ 4 & if \quad 5\pi/6<\theta<7\pi/6 \\ 5 & if \quad 7\pi/6<\theta<3\pi/2 \\ 6 & if \quad 3\pi/2<\theta<11\pi/6 \end{cases} \quad (5)$$

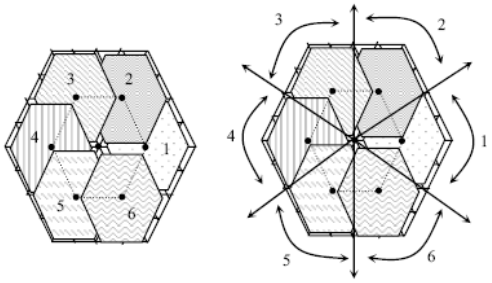

Fig.5 Division of overlapped regions

Secondly, we translate the origin of the reference voltage vector towards the center of the selected hexagon as indicated in Figure 6. This translation is done by subtracting the center vector of selected hexagon from the original reference vector. Table 2

gives the components d and q of the reference voltage V^{3*} after translation, for all the six hexagons. The index (^{5}) or (^{3}) above the components indicate five or three-level cases respectively.

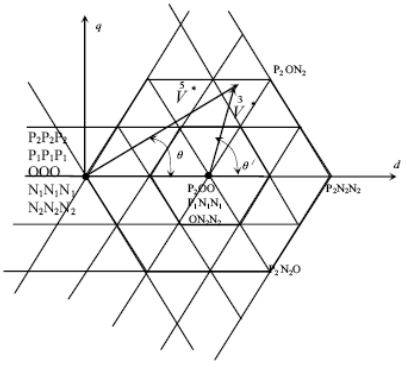

Fig.6 Translation of five-level reference voltage vector

Table 2 Correction of five-level reference voltage vector

s	v_d^{3*}	v_q^{3*}
1	$v_d^{5*}-1/2$	v_q^{5*}
2	$v_d^{5*}-1/4$	$v_q^{5*}-\sqrt{3}/4$
3	$v_d^{5*}+1/4$	$v_q^{5*}-\sqrt{3}/4$
4	$v_d^{5*}+1/2$	v_q^{5*}
5	$v_d^{5*}+1/4$	$v_q^{5*}+\sqrt{3}/4$
6	$v_d^{5*}-1/4$	$v_q^{5*}+\sqrt{3}/4$

To simplify into the space vector diagram of a two-level inverter, we have to take the two steps mentioned above. Figure 7 shows the translation of three-level reference voltage vector. The correction of its reference voltage vector is presented in Table 3.

At the end, one applied the pulse width modulation based on voltage space vectors of H. W. Van Der Broeck [11]:

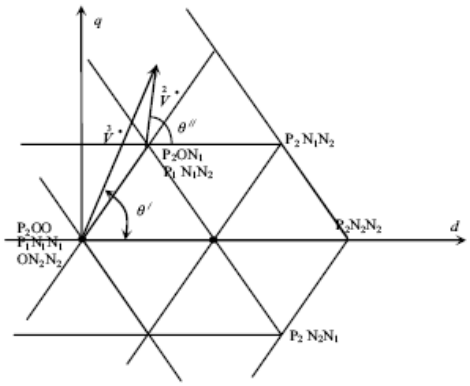

Fig.7 Translation of three-level reference voltage vector

Table 3 Correction of three-level reference voltage vector

s	v_d^{2*}	v_q^{2*}
1	$v_d^{3*}-1/4$	v_q^{3*}
2	$v_d^{3*}-1/8$	$v_q^{3*}-\sqrt{3}/8$
3	$v_d^{3*}+1/8$	$v_q^{3*}-\sqrt{3}/8$
4	$v_d^{3*}+1/4$	v_q^{3*}
5	$v_d^{3*}+1/8$	$v_q^{3*}+\sqrt{3}/8$
6	$v_d^{3*}-1/8$	$v_q^{3*}+\sqrt{3}/8$

3. Redundant vectors algorithm for five-level APF

In this part, one proposes to remedy to the instability problem of the input DC voltages of five-level APF, by using the redundant vectors of this topology. To know the impact of each vector on capacitors voltages, four steps must be followed:

First one consists in definition of equations representing capacitors currents as a function of load currents for each vector with redundant states. Tables 4,5,6 resume relationships between load currents and capacitor currents for all the redundant vectors of the space vector diagram.

To reduce the size of control algorithm, the second step consists in constituting vectors groups that have the same disposition in the table of states D1, D2 and D3. Table 7 shows six possible cases of disposition of states D1, D2 and D3. The different groups are listed bellow:

Group 1 : V1, V4, V7, V10, V13, V16
Group 2 : V2, V6, V8, V12, V14, V18
Group 3 : V3, V5, V9, V11, V15, V17
Group 4 : V19, V21, V23, V25, V27, V29
Group 5 : V20, V22, V24, V26, V28, V30
Group 6 : V31, V32, V33, V34, V35, V36

Third step consists in analyzing the influence of different groups of redundant vectors on capacitors voltages, under different conditions of load currents. From Table 7, it can be noticed that some vectors depend on state D1 (groups 1, 4 and 6) and others depend on states D1, D2 and D3 (groups 2, 3 and 5).

For vectors depending on state D1, there are two possibilities of polarity according to load currents. Each possibility is associated to logic function in the following manner:

$$\begin{cases} P_1 = 1 \ \ if \ \ D1 \geq 0 \ \ else \ \ P_1 = 0 \\ P_2 = 1 \ \ if \ \ D1 < 0 \ \ else \ \ P_2 = 0 \end{cases} \quad (6)$$

For vectors depending on states D1, D2 and D3, there are six possible combinations, according to load currents, associated to six logic functions defined as follows:

Table 4 Relationship between load currents and capacitor currents for the vectors with two redundant states

Vectors			$4\,i_{c1}$	$4\,i_{c2}$	$4\,i_{c3}$	$4\,i_{c4}$	D1=	D2=	D3=
V1	a	P2N1N1	D1	D1	D1	-3D1	-i1		
	b	P1N2N2	D1	3D1	D1	D1			
V2	a	P2ON1	D1	D1	D2	D3	-i1+i2	-i1-3i2	3i1+i2
	b	P1N1N2	D1	D3	D1	D2			
V3	a	P2P1N1	D1	D2	D1	D3	-i1-2i2	-i1+2i2	3i1+2i2
	b	P1ON2	D2	D3	D1	D1			
V4	a	P2P2N1	D1	D1	D1	-3D1	-i1-i2		
	b	P1P1N2	D1	-3D1	D1	D1			
V5	a	P1P2N1	D1	D2	D1	D3	-2i1-i2	2i1-i2	2i1+3i2
	b	OP1N2	D2	D3	D1	D1			
V6	a	OP2N1	D1	D1	D2	D3	i1-i2	-3i1-i2	i1+3i2
	b	N1P1N2	D1	D3	D1	D2			
V7	a	N1P2N1	D1	D1	D1	-3D1	-i2		
	b	N2P1N2	D1	-3D1	D1	D1			
V8	a	N1P2O	D1	D1	D2	D3	-i1-2i2	3i1+2i2	-i1+2i2
	b	N2P1N1	D1	D3	D1	D2			
V9	a	N1P2P1	D1	D2	D1	D3	2i1+i2	-2i1-3i2	-2i1+i2
	b	N2P1O	D2	D3	D1	D1			
V10	a	N1P2P2	D1	D1	D1	-3D1	i1		
	b	N2P1P1	D1	-3D1	D1	D1			
V11	a	N1P1P2	D1	D2	D1	D3	i1-i2	i1+3i2	-3i1-i2
	b	N2OP1	D2	D3	D1	D1			
V12	a	N1OP2	D1	D1	D2	D3	i1+2i2	i1-2i2	-3i1-2i2
	b	N2N1P1	D1	D3	D1	D2			
V13	a	N1N1P2	D1	D1	D1	-3D1	i1+i2		
	b	N2N2P1	D1	-3D1	D1	D1			
V14	a	ON1P2	D1	D1	D2	D3	2i1+i2	-2i1+i2	-2i1-3i2
	b	N1N2P1	D1	D3	D1	D2			
V15	a	P1N1P2	D1	D2	D1	D3	-i1+i2	3i1+i2	-i1-3i2
	b	ON2P1	D2	D3	D1	D1			
V16	a	P2N1P2	D1	D1	D1	-3D1	i2		
	b	P1N2P1	D1	-3D1	D1	D1			
V17	a	P2N1P1	D1	D2	D1	D3	i1+2i2	-3i1-2i2	i1-2i2
	b	P1N2O	D2	D3	D1	D1			
V18	a	P2N1O	D1	D1	D2	D3	-2i1-i2	2i1+3i2	2i1-i2
	b	P1N2N1	D1	D3	D1	D2			

Table 5 Relationship between load currents and capacitor currents for vectors with three redundant states

Vectors			$4\,i_{c1}$	$4\,i_{c2}$	$4\,i_{c3}$	$4\,i_{c4}$	D1=	D2=	D3=
V19	a	P2OO	D1	D1	-D1	-D1	-2i1		
	b	P1N1N1	D1	-D1	D1	-D1			
	c	ON2N2	-D1	-D1	D1	D1			
V20	a	P2P1O	D1	D2	D3	D3	-2i1-3i2	-2i1+i2	2i1+i2
	b	P1ON1	D2	D3	D1	D3			
	c	ON1N2	D3	D3	D2	D1			
V21	a	P2P2O	D1	D1	-D1	-D1	-2i1-2i2		
	b	P1P1N1	D1	-D1	D1	-D1			
	c	OON2	-D1	-D1	D1	D1			
V22	a	P1P2O	D1	D2	D3	D3	-3i1-2i2	i1-2i2	i1+2i2
	b	OP1N1	D2	D3	D1	D3			
	c	N1ON2	D3	D3	D2	D1			
V23	a	OP2O	D1	D1	-D1	-D1	-2i2		
	b	N1P1N1	D1	-D1	D1	-D1			
	c	N2ON2	-D1	-D1	D1	D1			
V24	a	OP2P1	D1	D2	D3	D3	3i1+i2	-i1-3i2	-i1+i2
	b	N1P1O	D2	D3	D1	D3			
	c	N2ON1	D3	D3	D2	D1			
V25	a	OP2P2	D1	D1	-D1	-D1	2i1		
	b	N1P1P1	D1	-D1	D1	-D1			
	c	N2OO	-D1	-D1	D1	D1			
V26	a	OP1P2	D1	D2	D3	D3	2i1-i2	2i1+3i2	-2i1-i2
	b	N1OP1	D2	D3	D1	D3			
	c	N2N1O	D3	D3	D2	D1			
V27	a	OOP2	D1	D1	-D1	-D1	2i1+2i2		
	b	N1N1P1	D1	-D1	D1	-D1			
	c	N2N2O	-D1	-D1	D1	D1			
V28	a	P1OP2	D1	D2	D3	D3	-i1+2i2	3i1+2i2	-i1-2i2
	b	ON1P1	D2	D3	D1	D3			
	c	N1N2O	D3	D3	D2	D1			
V29	a	P2OP2	D1	D1	-D1	-D1	2i2		
	b	P1N1P1	D1	-D1	D1	-D1			
	c	ON2O	-D1	-D1	D1	D1			
V30	a	P2OP1	D1	D2	D3	D3	i1+3i2	-3i1-i2	i1-i2
	b	P1N1O	D2	D3	D1	D3			
	c	ON2N1	D3	D3	D2	D1			

$$\begin{cases} P_1 = 1 \; if \; D1 < 0, D2 < 0, D3 \geq 0 \; else \; P_1 = 0 \\ P_2 = 1 \; if \; D1 < 0, D2 \geq 0, D3 < 0 \; else \; P_2 = 0 \\ P_3 = 1 \; if \; D1 < 0, D2 \geq 0, D3 \geq 0 \; else \; P_3 = 0 \\ P_4 = 1 \; if \; D1 \geq 0, D2 < 0, D3 < 0 \; else \; P_4 = 0 \\ P_5 = 1 \; if \; D1 \geq 0, D2 < 0, D3 \geq 0 \; else \; P_5 = 0 \\ P_6 = 1 \; if \; D1 \geq 0, D2 \geq 0, D3 < 0 \; else \; P_6 = 0 \end{cases} \quad (7)$$

The influence of different groups of redundant vectors on capacitors voltages depends on the logic function Pi like shown on Table 8. In this table, (+) indicates that the redundant vectors of the concerned group charge the capacitors and consequently increases the capacitor voltage. On the other hand, (-) indicates that the redundant vectors of the concerned group discharge the capacitor and consequently decreases its voltage.

Table 6 Relationship between load currents and capacitor currents for vectors with four redundant states

Vectors			4 i_{c1}	4 i_{c2}	4 i_{c3}	4 i_{c4}	D1=	D2=	D3=
V31	a	P2P1P1	D1	-3D1	D1	D1	i1		
	b	P1OO	-3D1	D1	D1	D1			
	c	ON1N1	D1	D1	-3D1	D1			
	d	N1N2N2	D1	D1	D1	-3D1			
V32	a	P2P2P1	D1	-3D1	D1	D1	i1+i2		
	b	P1P1O	-3D1	D1	D1	D1			
	c	OON1	D1	D1	-3D1	D1			
	d	N1N1N2	D1	D1	D1	-3D1			
V33	a	P1P2P1	D1	-3D1	D1	D1	i2		
	b	OP1O	-3D1	D1	D1	D1			
	c	N1ON1	D1	D1	-3D1	D1			
	d	N2N1N2	D1	D1	D1	-3D1			
V34	a	P1P2P2	D1	-3D1	D1	D1	-i1		
	b	OP1P1	-3D1	D1	D1	D1			
	c	N1OO	D1	D1	-3D1	D1			
	d	N2N1N1	D1	D1	D1	-3D1			
V35	a	P1P1P2	D1	-3D1	D1	D1	-i1-i2		
	b	OOP1	-3D1	D1	D1	D1			
	c	N1N1O	D1	D1	-3D1	D1			
	d	N2N2N1	D1	D1	D1	-3D1			
V36	a	P2P1P2	D1	-3D1	D1	D1	-i2		
	b	P1OP1	-3D1	D1	D1	D1			
	c	ON1O	D1	D1	-3D1	D1			
	d	N1N2N1	D1	D1	D1	-3D1			

Table 7 Disposition of states D1, D2 and D3

Vectors		4i_{c1}	4i_{c2}	4i_{c3}	4i_{c4}	D1	D2	D3
V1	(a)P2N1N1	D1	D1	D1	-3D1	-i1		
	(b)P1N2N2	D1	-3D1	D1	D1			
V2	(a)P2ON1	D1	D1	D2	D3	-i1 +i2	-i1 -3i2	3i1 +i2
	(b)P1N1N2	D1	D3	D1	D2			
V3	(a)P2P1N1	D1	D2	D1	D3	-i1-2i2	-i1 +2i2	3i1 +2i2
	(b)P1ON2	D2	D3	D1	D1			
V19	(a)P2OO	D1	D1	-D1	-D1	-2i1		
	(b)P1N1N1	D1	-D1	D1	-D1			
	(c)ON2N2	-D1	-D1	D1	D1			
V20	(a)P2P1O	D1	D2	D3	D3	-2i1 -3i2	-2i1 +i2	2i1 +i2
	(b)P1ON1	D2	D3	D1	D3			
	(c)ON1N2	D3	D3	D2	D1			
V31	(a)P2P1P1	D1	-3D1	D1	D1	i1		
	(b)P1OO	-3D1	D1	D1	D1			
	(c)ON1N1	D1	D1	-3D1	D1			
	(d)N1N2N2	D1	D1	D1	-3D1			

Fourth step consists to choice the redundancies. For each case of redundancy, the vector which tends to cancel the unbalance in capacitor voltages will be selected. In other words, we select the vector which charge the undercharged capacitors, and discharge the overcharged ones.

To do so, we most measure capacitor voltages and their derivation case. We get 24 cases. For each selected vector, the redundancy that will decrease the largest capacitor voltage and increase the smallest capacitor voltage is selected (Table 9).

4. Sliding mode control of APF

Active power filter is controlled using sliding mode regulator [12,13]. From the model of active filter associated to supply network (8) and by considering the error between harmonic current reference and the active filter current as sliding surface (9), and the smooth continuous function as attractive control function (10), one gets the control law (11).

$$V_{frefK} - V_K = R_f \cdot i_{fK} + L_f \cdot (di_{fK} / dt) \quad (8)$$

with:

$V_K = V_{sK} - R_s \cdot i_{SK} - L_s \cdot (di_{sK} / dt)$; K = 1,2 and 3

$$S = i_{frefK} - i_{fK} \quad (9)$$

$$U_n = k \cdot (S / (|S| + \lambda)) \quad (10)$$

$$V_{frefK} = R_f \cdot i_{fK} + L_f \cdot (di_{frefK} / dt) + V_K + k \cdot (S / (|S| + \lambda)) \quad (11)$$

Table 8 Effect of redundant vectors on capacitors voltages

Groups		Redundancy (a)				Redundancy (b)				Redundancy (c)				Redundancy (d)			
		U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}	U_{c1}	U_{c2}	U_{c3}	U_{c4}
6	P_1	+	-	+	+	-	+	+	+	+	+	-	+	+	+	+	-
	P_2	-	+	-	-	+	-	-	-	-	-	+	-	-	-	-	+
5	P_1	-	-	+	+	-	+	-	+	+	+	-	-				
	P_2	-	+	-	-	+	-	-	-	-	-	+	-				
	P_3	-	+	+	+	+	+	-	+	+	+	+	-				
	P_4	+	-	-	-	-	-	+	-	-	-	-	+				
	P_5	+	-	+	+	-	+	+	+	+	+	-	+				
	P_6	+	+	-	-	+	-	+	-	-	-	+	+				
4	P_1	+	+	-	-	+	-	+	-	-	-	+	+				
	P_2	-	-	+	+	-	+	-	+	+	+	-	-				
3	P_1	-	-	-	+	-	+	-	-								
	P_2	-	+	-	-	+	-	-	-								
	P_3	-	-	-	+	+	+	-	-								
	P_4	+	-	+	-	-	-	+	+								
	P_5	+	-	+	+	-	+	+	+								
	P_6	+	+	+	-	+	-	+	+								
2	P_1	-	-	-	+	-	+	-	-								
	P_2	-	-	+	-	-	-	-	+								
	P_3	-	-	+	+	-	+	-	+								
	P_4	+	+	-	-	+	-	+	-								
	P_5	+	+	-	+	+	+	+	-								
	P_6	+	+	+	-	+	-	+	+								
1	P_1	+	+	+	-	+	-	+	+								
	P_2	-	-	-	+	-	+	-	-								

5. Simulation Results

A medium voltage source of 5.5kV, 50Hz feeds a non-linear load as illustrated in Figure 1. This load produces distorted phases currents with total harmonic distortion (THD) of respectively 120%, 129% and 83% which is above the tolerated THD limit standard. These currents with there spectral analysis are presented in Figure 8.

The first part of this simulation is dedicated to investigating the performance of the Redundant Vectors Control Algorithm (RVCA). For that, active power filtering is introduced at t=2s without applied RVCA. One remarks that capacitors voltages diverge (Figure 9). Application of the proposed RVCA based SVPWM at t=5s, push capacitors voltages towards the reference value of 3 kV keeping them constant.

The second part is devoted to testing the performance of the APF. As shown in Figure 10, at t= 7s, the resistor value changes from R2 = 300Ω to R2 = 100Ω. This resistor variation implies the increase of the non-linear load current amplitude. The capacitors voltages are not disturbed by this load variation (Figure 9).

Figure. 11.a,b,c presents main source voltages and currents after harmonic currents compensation. Spectral analysis of each current is illustrated in Figure. 11.d,e,f. It is shown that source currents are almost sinusoidal with THD low than 3%.

Simulation Parameters:

Main source:
$V_{(ph\text{-}ph)}$ = 5.5k V, f = 50 Hz, R_s = 0.0001Ω, L_s = 0.001H.
Load:
C1=C2 = 0.05 F, R1=200, R2 = 300Ω (t = 2s), R2 = 100Ω (t = 7s).
Active power filter:
R_f = 0.0001 Ω, L_f = 0.0035 H, C= 0.01F, f_c = 2kHz.

Table 9 Selection of redundancies

Groups	1		2						3						4		5						6	
Possibility / Derivation case	P1	P2	P1	P2	P3	P4	P5	P6	P1	P2	P3	P4	P5	P6	P1	P2	P1	P2	P3	P4	P5	P6	P1	P2
Uc1<Uc2<Uc3<Uc4	a	b	b	a	b	a	b	a	b	b	b	a	a	a	a	c	c	b	c	a	c	a	d	b
Uc1<Uc2<Uc4<Uc3	a	b	b	a	b	a	a	a	b	b	b	a	a	a	a	c	c	b	b	a	c	a	c	b
Uc1<Uc3<Uc2<Uc4	a	b	b	a	a	b	b	a	b	b	b	a	a	a	b	c	c	b	c	a	a	b	d	b
Uc1<Uc3<Uc4<Uc2	b	a	a	a	a	b	b	b	a	b	b	a	a	b	b	a	a	b	c	a	a	b	a	b
Uc1<Uc4<Uc2<Uc3	b	a	a	a	b	a	a	b	a	b	b	a	a	b	a	c	c	b	b	a	c	a	c	b
Uc1<Uc4<Uc3<Uc2	b	a	a	b	a	b	a	b	a	b	b	a	a	b	b	a	a	b	b	a	a	b	a	b
Uc2<Uc1<Uc3<Uc4	a	b	b	a	b	a	b	a	b	a	b	a	b	a	a	c	c	a	c	a	c	a	d	a
Uc2<Uc1<Uc4<Uc3	a	b	b	a	b	a	a	a	b	a	b	a	b	a	a	c	c	a	b	a	c	a	c	a
Uc2<Uc3<Uc1<Uc4	a	b	b	a	b	a	b	a	b	a	b	a	b	a	a	c	c	a	c	b	b	a	d	a
Uc2<Uc3<Uc4<Uc1	a	b	b	a	b	a	b	a	b	a	a	b	b	a	c	c	b	a	a	b	b	c	b	a
Uc2<Uc4<Uc1<Uc3	a	b	b	a	b	a	a	a	b	a	a	b	b	a	a	b	b	a	b	c	c	a	c	a
Uc2<Uc4<Uc3<Uc1	a	b	b	b	b	a	a	a	b	a	a	b	b	a	c	b	b	a	a	c	b	c	b	a
Uc3<Uc1<Uc2<Uc4	a	b	b	a	a	b	b	a	b	b	b	a	a	a	b	c	c	c	c	b	a	b	d	c
Uc3<Uc1<Uc4<Uc2	b	a	a	a	a	b	b	b	a	b	b	a	a	b	b	a	a	c	c	b	a	b	a	c
Uc3<Uc2<Uc1<Uc4	a	b	b	a	a	b	b	a	b	a	b	a	b	a	b	c	c	c	c	b	b	b	d	c
Uc3<Uc2<Uc4<Uc1	a	b	b	a	a	b	b	a	b	a	a	b	b	a	c	a	a	c	a	b	b	c	b	c
Uc3<Uc4<Uc1<Uc2	b	a	a	a	a	b	b	b	a	b	a	b	a	b	c	a	a	c	a	b	a	c	a	c
Uc3<Uc4<Uc2<Uc1	b	a	a	a	a	b	b	b	a	a	a	b	b	b	c	a	a	c	a	b	b	c	b	c
Uc4<Uc1<Uc2<Uc3	b	a	a	b	b	a	a	b	a	b	a	b	a	b	a	b	b	b	b	c	c	a	c	d
Uc4<Uc1<Uc3<Uc2	b	a	a	b	a	b	a	b	a	b	a	b	a	b	c	a	a	b	b	c	a	c	a	d
Uc4<Uc2<Uc1<Uc3	b	a	a	b	b	a	a	b	a	a	a	b	b	b	a	b	b	a	b	c	c	a	c	d
Uc4<Uc2<Uc3<Uc1	b	a	a	b	b	a	a	b	a	a	a	b	b	b	c	b	b	a	a	c	b	c	b	d
Uc4<Uc3<Uc1<Uc2	b	a	a	b	a	b	a	b	a	b	a	b	a	b	c	a	a	c	a	c	a	c	a	d
Uc4<Uc3<Uc2<Uc1	b	a	a	b	a	b	a	b	a	a	a	b	b	b	c	a	a	c	a	c	b	c	b	d

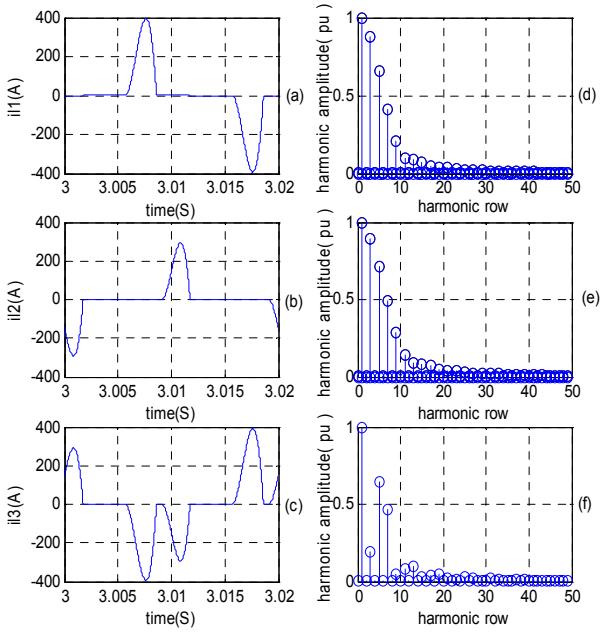

Fig.8 Current drawn by the non-linear load

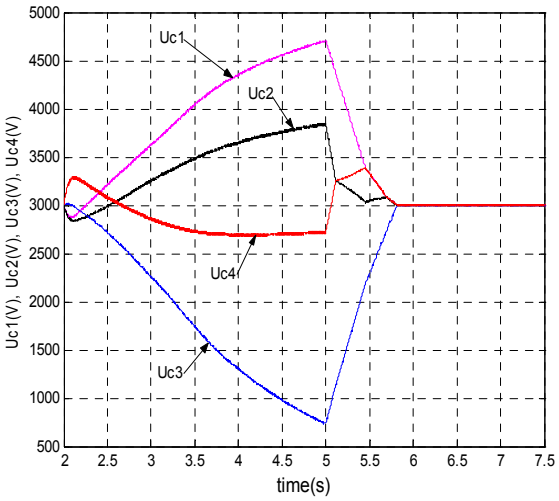

Fig.9 DC bus capacitors voltages of five-level APF

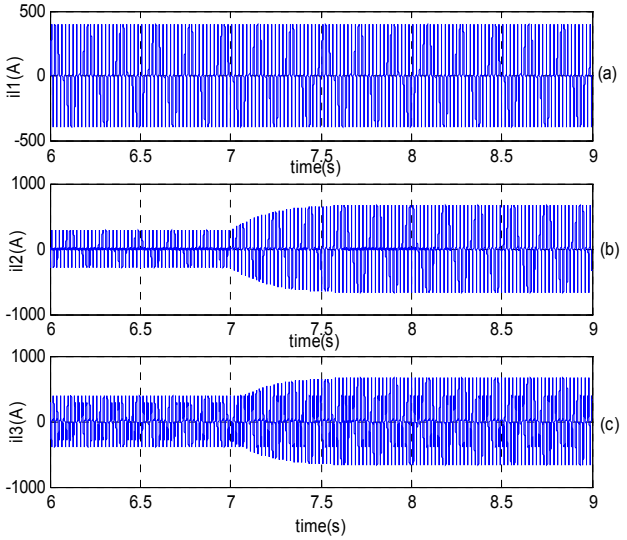

Fig.10 Load currents

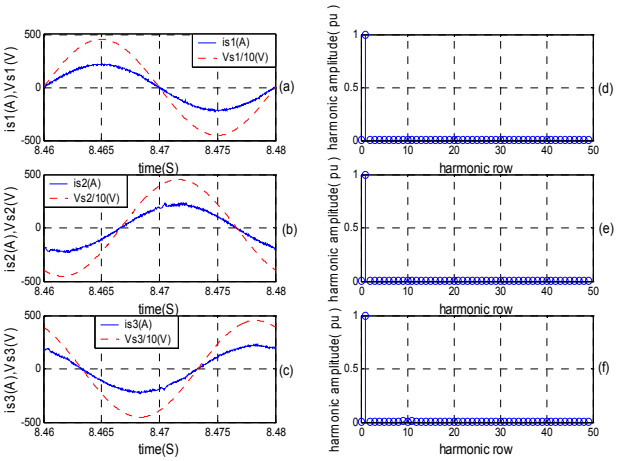

Fig.11 Main source voltages and currents with their spectral analysis

6. Conclusion

This paper presents an algorithm for self stabilization of dc link capacitors voltages using redundant vectors of five-level diode clamped shunt active power filter. A comprehensive analysis of the dc link capacitor voltages balancing is presented. Based on the measurement of load currents and determination of capacitor currents signs, the desirable redundant vector is selected. Also, a simplified space vector pulse width modulation algorithm has been described and applied to five-level inverter. Through the decomposition of the space vector diagram the complicated five-level space vector modulation algorithm is simplified into two-level cases.

This simplified SVPWM method has the advantages to reduce the execution time of the five-level inverter modulation and allows saving memory of the controller in case of experimental realization.

With a low switching frequency the proposed redundant vectors control makes possible:

- Stable multi DC link voltages without using additional power electronics circuitry;
- Active power filtering in medium voltage without using transformer.
- Low total harmonic distortion of main source currents.
- Compensation of reactive power.

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