Switched-Current Techniques: An Overview of Cumulative SI-Related Errors on Dynamic and Static Performances of 2nd Order LP-ΣΔMs

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Abstract — We present in this work a systematic analysis to identify Sigma Delta Modulators (ΣΔMs) non-idealities, such as charge injection error, I/O conductance ratio error and settling time error. A physical mechanism behind Switched Current (SI) errors is proposed. In the first time, errors mentioned above are treated separately and a behavioural model of SI cell is derived for each non-ideality. In the second time, we propose a behavioural model of Non-inverting Lossless Integrator. For typical variations of SI-related errors, simulations have been made using Matlab/Simulink. Finally we present their influences on both dynamic and static performances of the 2nd order SI Low Pass ΣΔMs (SI-LPΣΔMs).

Key-words: ADC converter, Switched Current technique, Sigma-Delta Modulator, error mechanisms, Dynamic and Static Performances.

1 Introduction

The staggering scaling-down of Complementary Metal Oxide Semiconductor (CMOS) Very-Large-Scale Integration (VLSI) technologies and the tendency towards Systems On Chip (SOC) are prompting the development of new digital telecommunication devices spanning the portable gadgets of nowadays (cellular phone, smart phone, tablet computer...). SI technique has been adopted in many applications (e.g. filtering [1, 2], current differentiation [3], Sigma Delta modulation [4], Digital to Analog Converters (DACs) and Analog to Digital Converters (ADCs) [5, 6, 7]). ΣΔMs are very suited to implement high-resolution and robust (lower sensitivity to circuitry imperfections) ADCs, not only by increasing the oversampling ratio (a sampling frequency much larger than the Nyquist frequency) but also by pushing the quantization noise out of the band of interest. Furthermore, oversampled SI ΣΔMs have gained much popularity for their high-speed, low consumption and low supply voltage compared to the Switched-Capacitor (SC) technique [8, 9, 10, 11]. The use of such technique facilitates the integration of a whole system into a mixed signal chip. The analog portion of these chips must feature the required analog performance level in VLSI standard, what has motivated exploring analog design technique compatible with CMOS process [12, 13, 14].

Several works have been focused on identifying and modeling non-idealities in both SI and SC techniques in order to get a behavioural model of these cells. The non-ideal behavioural model has been made only at memory cell level [2, 8, 21, 22, 23]. M.Loulou et al. and N. Khitouni et al, respectively [15] and [16], have developed a mathematical model of charge injection phenomena. By using a continuous and physical formulation based on the EKV model, A. Dei et al. [17] have developed a compact behavioural model of the MOS analogue switch for charge injection analysis. According to W.Ming Koe et al. [18], a better understanding of non-idealities in switched-capacitor circuits on sigma-delta modulators can be achieved if each of these non-idealities is studied separately.

In this work, we will study the cumulative effect of SI-related error on dynamic and static SI-LPΣΔM performances. The analysis will be focused on 1-bit 2nd-LPΣΔM. This modulator is easy to understand and simple to design. Nevertheless, this study can be extended to other architectures such as multi-stage cascade modulators [7], since the integrator represent the main block in this kind of architectures.

The paper is organized as follows; A briefly review of ΣΔM principle is presented in section 2. In section 3, we analyse the effect of isolated non-idealities on transfer function of SI memory cell. Section 4 describes the cumulative error effect on the transfer function of the Non-Inverting Lossless Integrator. The impact on the dynamic and static performances on LP-SIΣΔM is carried out in

Section 5. Lastly, we conclude this paper in section 6.

2 Modulator Architecture Overview

Fig. 1 shows the Z-domain of 1-bit 2nd-LPΣΔM block diagram. The output modulator is given by Equ. 1 if we assume that the quantized error is modeled as a white noise [7]:

$$S(z) = STF(z) \cdot X(z) + NTF(z) \cdot E(z) \quad (1)$$

Where, X*(z)* and *E(z)* are respectively the z-transform of the input signal and the quantization noise source. The Signal Transfer Function (STF) and the Noise Transfer Function (NTF) are given by:

$$STF(z) = z^{-2} \quad (2)$$

$$NTF(z) = \left(1 - z^{-1}\right)^2 \quad (3)$$

For physical frequencies, $z = e^{j\omega T}$, and ωT much smaller than unity to correspond to the highly oversampled situation, the magnitude response of *NTF* can be very well approximated by ω. Thus at low frequencies, the quantization noise is made insignificant, whereas at high frequencies it is greatly increased. We can therefore conclude that the *NTF* is a high-pass function and the noise power is shaped to frequency region where the input signal is not located. Subsequent filtering can then separate the input signal from the quantization noise as illustrated in Fig. 2(a).

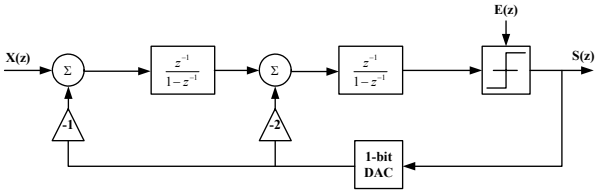


Fig. 1. 1-bit 2nd-LPΣΔM Architecture under study.

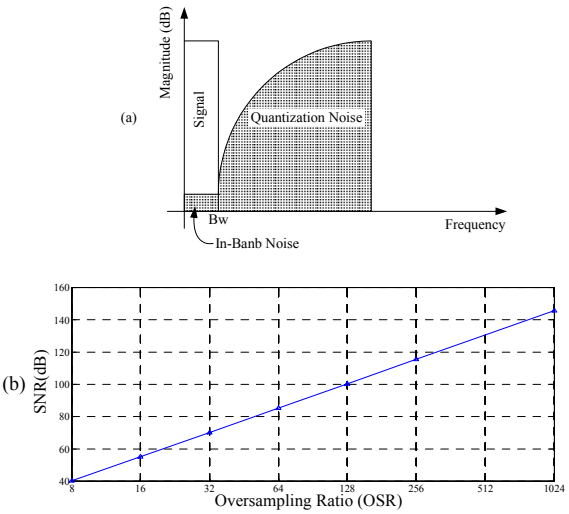


Fig. 2. (a) Filtering function of 2nd-LPSDMs, (b) SNR(dB) vs. oversampling ratio OSR

The in band quantization noise power is given by Equ. 4:

$$P_Q = \int_0^{Bw} 2 \cdot E \cdot \left|NTF(f)\right|^2 df = \frac{\Delta^2}{12 \cdot \pi \cdot OSR} \sin\left(\frac{2\pi}{OSR}\right) \cdot OSR + 6\pi - 8 \cdot \sin\left(\frac{\pi}{OSR}\right) \cdot OSR \quad (4)$$

Where, *Bw* is the signal band, Δ is the quantization noise step, and $OSR = \frac{f_s}{2 \cdot Bw}$ is the oversampling ratio with f_s is the sampling frequency.

Consider a sinewave input signal and *N* is the quantizer resolution, the maximum full-scale input signal power is found to be,

$$P_s = \frac{\left(\frac{\Delta \cdot 2^N}{2}\right)^2}{2} \quad (5)$$

And then the Signal to Noise Ratio (SNR) is given as below:

$$SNR_{dB} = 10 \cdot \log_{10}\left(\frac{P_s}{P_Q}\right) = 10 \cdot \log_{10}\left(\frac{6\pi M}{\sin\left(\frac{2\pi}{OSR}\right) \cdot OSR + 6\pi - 8 \cdot \sin\left(\frac{\pi}{OSR}\right) \cdot OSR}\right) \quad (6)$$

Equ. 7 gives the output Effective Number Of Bit (ENOB).

$$ENOB = \frac{SNR_{dB} - 1.7}{6.02} \quad (7)$$

In this scenario presented by equations (6) and (7), the resolution increases with *OSR* at rate of $\approx 2.5bit/octave$ as illustrated in Fig. 2(b).

3 Study Of Isolated Error Mechanism Of SI Cell

Several alternatives to analyse the non-idealities behaviour have been described in the literature [13, 24, 25]. These errors are responsible for SNR degradation of ΣΔMs. The main errors related on the SI memory cell are: output-input conductance ratio, charge injection and settling time errors. A switched current memory cell performs the function of a current copier, and it is ideally modeled by a delay line of a half clock period as shown in Fig. 3(a). In this paper, the study is based on 2nd generation memory cell presented in Fig. 3(b). In this kind of cell, the same transistor is used to implement both the sink and source currents. Thus, it does not exhibit mismatch errors [23].

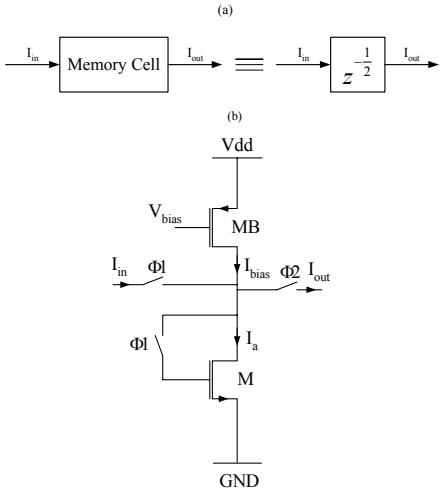


Fig. 3. Ideal 2nd generation SI memory cell, (a) z-domain building bloc, (b) transistor level.

3.1 Output-input conductance ratio error

As it shown in Fig.4 (a), the memory cell can be modeled as an ideal memory transistor *M* in parallel with a conductance g_0 given by Equ. 8. [8, 13, 24].

$$g_0 = g_{ds}\frac{C_{gd}}{C + C_{gd}}g_m \quad (8)$$

Where g_{ds} is the output conductance of memory transistor, *C* is the memory capacitor, g_m is the transconductance of the memory transistor *M* and C_{gd} is the drain gate parasitic capacitance.

This conductance is due to two main effects:

- Firstly, the channel length modulation effect of both memory transistor *M* and the bias one *MB*.
- Secondly, the charge injected into the memory capacitance *C* when the gate of the memory transistor held open. This leads to a disturbance of the gate-source voltage and therefore an error in the drain current I_a.

We consider cascaded memory cell shown in Fig. 4(b) and taken the equivalent small signal model shown in Fig. 4(c). On phase *Φ1*, memory transistor *M1* is diode connected, therefore for small signal $V_{ds} = V_{gs} + \frac{I_{in}(n-1)}{g_m}$ and $I_{a1}$is given by Equ. 9.

$$I_{a1} = I_{bias} + I_{in}(n-1) - I_{g_{01}} = I_{bias} + I_{in}(n-1)\left(1 - \frac{g0}{gm}\right) - V_{gs}\cdot g_0 \quad (9)$$

On phase *Φ2*, the drain voltage of *M1* is determined by the gate voltage of *M2* i.e. $V_{ds1} = V_{gs2} = V_{gs} + \frac{I_{out1}\left(n-\frac{1}{2}\right)}{g_m}$ and Equ. 10 gives the output current $I_{out1}\left(n-\frac{1}{2}\right)$.

$$I_{out1}\left(n-\frac{1}{2}\right) = I_{bias} - I_{a1} - I_{g_{02}} = -I_{in}(n-1)\left(1 - \frac{2g_0}{g_m}\right) \approx -\frac{I_{in}(n-1)}{1+\frac{2g_0}{g_m}} \quad (10)$$

We notice, after making z-transformation, that the transfer function of the memory cell can be written by Equ. 11:

$$H_{\varepsilon_g}(z) = \frac{I_{out1}(z)}{I_{in}(z)} = \frac{-z^{-\frac{1}{2}}}{1+\frac{2g_0}{g_m}} = \frac{H_i(z)}{1+\varepsilon_g} \quad (11)$$

Where $H_i(z)$ is the ideal transfer function of the SI memory cell and $\varepsilon_g = \frac{2g_0}{g_m}$

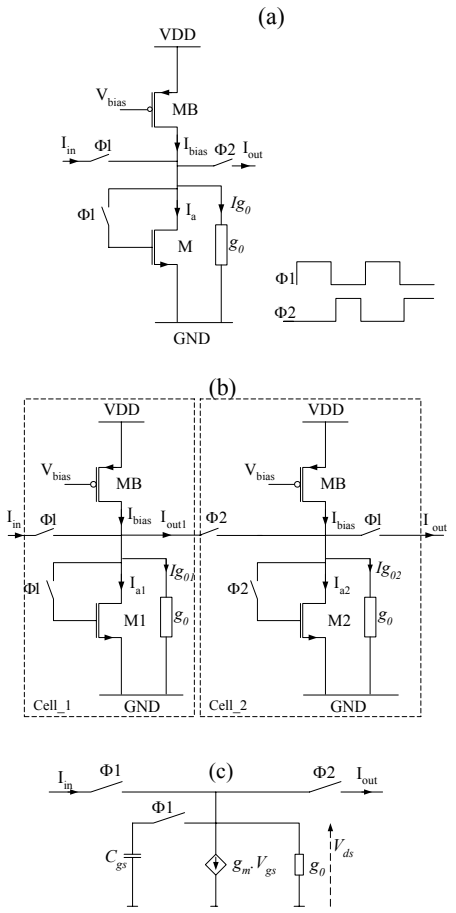


Fig. 4. 2nd generation SI memory cell. (a) With output-input conductance error. (b) Cascaded memory cells. (c) Small signal model.

3.2 Settling time error

SI circuits are based on charging and discharging the gate capacitance of the memory transistor. During the sampling phase, the input current witch is applied to the memory cell charges or discharges the gate-source capacitance C_{gs}. If at the end of the sampling period, C_{gs} has not been charged or discharged to the final value, errors occur in the memorized current I_a. This error is represented by ε_s in SI context.

In this analysis, we consider the linear model of SI memory cell presented in Fig. 3(b) with only ε_s error. During the clock phase *Φ1* the memory transistor is diode-connected and the drain current I_a increases from its previous level $I_a(n-1)$ towards a new level given by Equ. 12.

$$\widehat{I_a}\left(n\right) = I_{bias} + I_{in}\left(n-\frac{1}{2}\right) \qquad (12)$$

Assuming the cell is linear and so I_a reaches a final value $I_a(n)$ given by

$$I_a\left(n\right) = I_a\left(n-1\right) + \left[\widehat{I_a}\left(n\right) - I_a\left(n-1\right)\right]\left(1-\varepsilon_s\right) \qquad (13)$$

Where $\varepsilon_s = e^{\frac{T}{2\tau}}$ is the settling time error. The time-constant $\tau=C/g_m$ represents the effective time constant of the memory cell occur on clock phase *Φ1* [26].

During the next phase *Φ2*, $I_{out}(n)$ is given by Equ. 14. And during previous phase *Φ2*, the output current is given by Equ. 15.

$$I_{out}\left(n\right) = I_{bias} - I_a\left(n\right) \qquad (14)$$

$$I_{out}\left(n-1\right) = I_{bias} - I_a\left(n-1\right) \qquad (15)$$

The output SI cell current is expressed from Equ.12 to Equ 15 by:

$$I_{out}\left(n\right) = \varepsilon_s I_{out}\left(n-1\right) - \left(1-\varepsilon_s\right) I_{in}\left(n-\frac{1}{2}\right) \qquad (16)$$

The transfer function with settling time error is given by:

$$H_{\varepsilon_s}\left(z\right) = -z^{-\frac{1}{2}}\frac{1-\varepsilon_s}{1-\varepsilon_s z^{-1}} = H_i\frac{1-\varepsilon_s}{1-\varepsilon_s z^{-1}} \qquad (17)$$

We notice that settling time gives rise to an additional multiplicative error term in the overall transfer function.

3.3 Charge injection error

Referring to Fig. 5(a), switches are realized through MOS transistors operating alternatively in linear and cut-off region. When switch M_s goes off, channel charges flow out of its drain, substrate and source. Part of this charge is dumped to the memory capacitance C. In addition, due to the overlapping capacitance C_{ol} and the channel capacitance C_{ch}, the memory gate-source voltage Vgs of M vary [8, 13].

We consider tow cascaded memory cell shown in Fig. 5(b). During phase *Φ1* of period *(n-1)Ts*, where *Ts* is the sampling period, the drain current in *M1* is:

$$I_a\left(n-1\right) = I_{bias} + I_{in}\left(n-1\right) \qquad (18)$$

At the end of phase *Φ1*, switch *S1* opens and its charge q_a causes an error δI_a in the current stored during the next phase *Φ2*. The expressions of stored current in *M1* and *M2* are given respectively by Equ. 19 and Equ. 20.

$$I_a\left(n-\frac{1}{2}\right)=I_a\left(n-1\right)-\delta I_a \quad (19)$$

$$I_b\left(n-\frac{1}{2}\right)=2I_{bias}-I_a\left(n-\frac{1}{2}\right)=I_{bias}-I_{in}\left(n-1\right)+\delta I_a \quad (20)$$

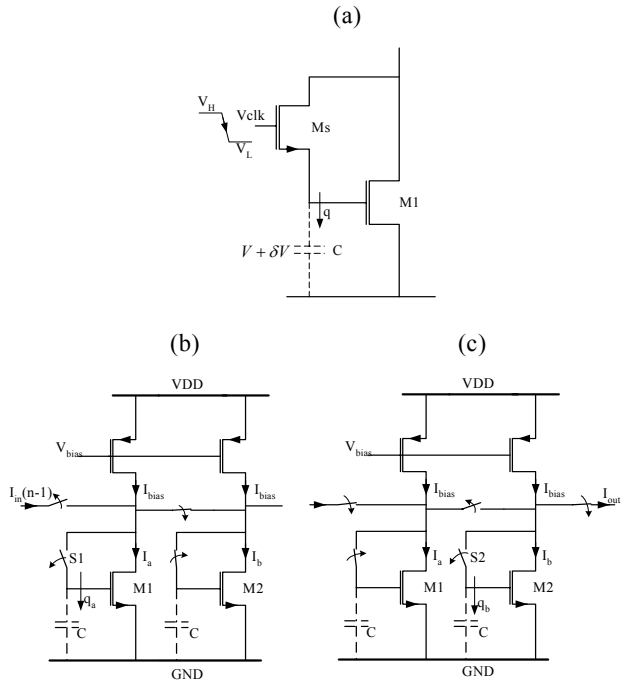


Fig. 5. Cascaded SI memory cell. (a) SI memory cell with a switch transistor. (b) Phase *Φ1*. (c) Phase *Φ2*.

At the end of clock phase *Φ2*, shown in Fig. 5(c), switch *S2* opens and its charge q_b causes an error δI_b in the current stored during the next phase *Φ1*.

$$I_b\left(n\right)=I_b\left(n-\frac{1}{2}\right)-\delta I_b=I_{bias}-I_{in}\left(n-1\right)+\left(\delta I_a-\delta I_b\right) \quad (21)$$

As reported in [8] and [13], $\left(\delta I_a-\delta I_b\right)$ is given by:

$$\delta I_a-\delta I_b=2\varepsilon_q I_{in}\left(n-1\right),\qquad \varepsilon_q=\frac{K_A}{V_{gs}-V_T}-K_B \quad (22)$$

Where K_A and K_B are respectively the coefficient of the independent and the dependent parts of the signal, which are given by:

$$K_A=\alpha\frac{C_{ch}}{C}\left(V_H-\left(2+\frac{\gamma}{3}\right)V_{gs}-V_T\right)+\left(V_H-V_L\right)\frac{C_{ol}}{C}$$
$$K_B=2\alpha\left(1+\frac{\gamma}{3}\right)\frac{C_{ch}}{C} \quad (23)$$

With V_T is the threshold voltage of switch transistor M_s, γ is bulk-threshold parameter, α determines the portion of the channel charge that flows to the memory capacitance *C*

Substituting Equ. 23 in Equ. 22, for $I_{out}\left(n\right)=I_{bias}-I_b\left(n\right)$, and after performing the z-transform, the transfer function of the pair memory cell yields:

$$\left[H\left(z\right)\right]^2=\left(1-2\varepsilon_q\right)z^{-1} \quad (24)$$

And then, the transfer function of single SI cell can be written as:

$$H_{\varepsilon_q}\left(z\right)=\frac{-z^{-\frac{1}{2}}}{1+\varepsilon_q}=\frac{H_i\left(z\right)}{1+\varepsilon_q} \quad (25)$$

4 Cumulative Errors Effect On The Non-Inverting Lossless SI Integrator

The isolated influence of main SI errors on the transfer function of SI memory cell has been analysed in the previous section. In this section, analysis will be extended from the memory cell to another higher hierarchical level circuit such as integrator.

We consider the SI realization of Non-Inverting Lossless Integrator shown in Fig. 6(a). On clock phase *Φ1* the small signal equivalent circuit is shown in Fig. 6(b). The steady state drain current $\hat{I}_{a1}$ of memory transistor *M1* is given by:

$$\hat{I}_{a1}\left(n\right)=\left(1-\varepsilon_g\right)\left(I_{in}\left(n\right)-\left(1-\varepsilon_q\right)I_{a2}\left(n-1\right)\right) \quad (26)$$

Equ. 27 presents the influence of the settling time error on the memory transistor drain current.

$$I_{a1}\left(n\right)=\varepsilon_s I_{a1}\left(n-1\right)+\left(1-\varepsilon_s\right)\hat{I}_{a1}\left(n\right) \quad (27)$$

On clock phase *Φ2* the small signal equivalent circuit is shown in Fig. 6(c). The steady state drain current $\hat{I}_{a2}$ of memory transistor *M2* is given by:

$$\hat{I}_{a2}\left(n\right)=-\left(1-\varepsilon_g\right)\left(1-\varepsilon_q\right)I_{a1}\left(n\right) \quad (28)$$

Due to settling time error,

$$I_{a2}\left(n\right)=\varepsilon_s I_{a2}\left(n-1\right)+\left(1-\varepsilon_s\right)\hat{I}_{a2}\left(n\right) \quad (29)$$

Assuming that the current mirror is ideal, the output current will be:

$$I_{out}\left(n\right)=-\left(1-\varepsilon_q\right)I_{a2}\left(n\right) \quad (30)$$

From Equ. 26 to Equ. 30 and after performing z-transform, the transfer function of the Non-

Inverting Lossless Integrator with all errors mentioned in the above section (ε_g,ε_q and ε_s) is expressed by Equ. 31.

$$H^{int}_{\varepsilon_g,\varepsilon_q,\varepsilon_s}(z)=\frac{\left(1-\varepsilon_g\right)^2\left(1-\varepsilon_q\right)^2\left(1-\varepsilon_s\right)^2 z^{-1}}{1-\left(2\varepsilon_s+\left(1-\varepsilon_g\right)^2\left(1-\varepsilon_q\right)^2\left(1-\varepsilon_s\right)^2\right)z^{-1}+\varepsilon_s{}^2 z^{-2}} \quad (31)$$

By nullifying errors (ε_g, ε_q and ε_s) in Equ. 31, we obtain the ideal transfer function of the integrator shown in Fig. 1. Furthermore, all error mechanisms contribute as a gain error, but the settling time error is the only one that changes the poles of the SI integrator transfer function.

After identifying the error mechanisms of SI memory cell and SI integrator, next section will be focused on the effect of these errors on 2nd order SI-LPΣΔM dynamic and static performances.

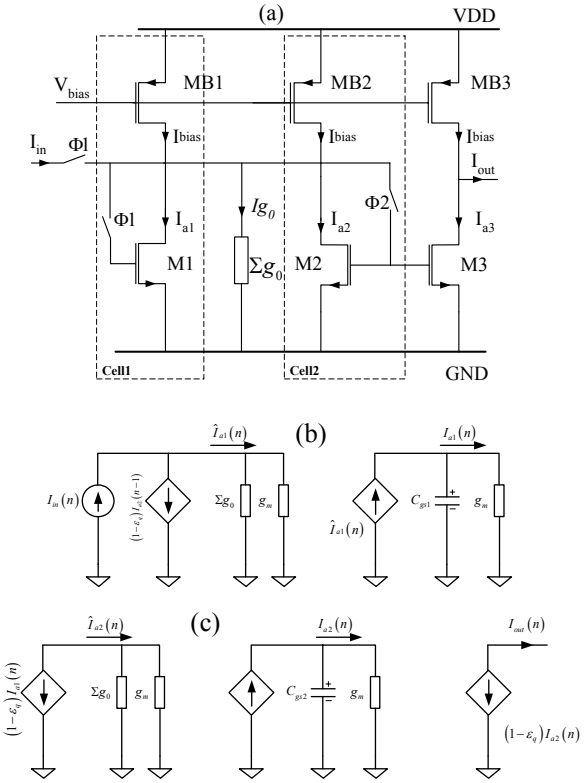


Fig. 6. Non-inverting Lossless Integrator. (a) SI schematic. (b) Small signal equivalent circuit during *Φ1*. (c) Small signal equivalent circuit during *Φ2*

5 Non-Idealities Effects On 2nd Order LP-SIΣΔM

This section analyses the influence of the fundamental error mechanisms, detailed in the previous sections, on the performances of 2nd order LP-SIΣΔM. Analysis will be focused on: firstly, the separately effect of each non ideality by keeping one error and nullifying the rest (e.i. ε_g=ε_q=0, 0<ε_s<5%) (Equ.32 and Equ. 33).

$$H^{int}_{\varepsilon_{g,q}}(z)=\frac{\left(1-\varepsilon_{g,q}\right)^2 z^{-1}}{1-\left(1-\varepsilon_{g,q}\right)^2 z^{-1}} \quad (32)$$

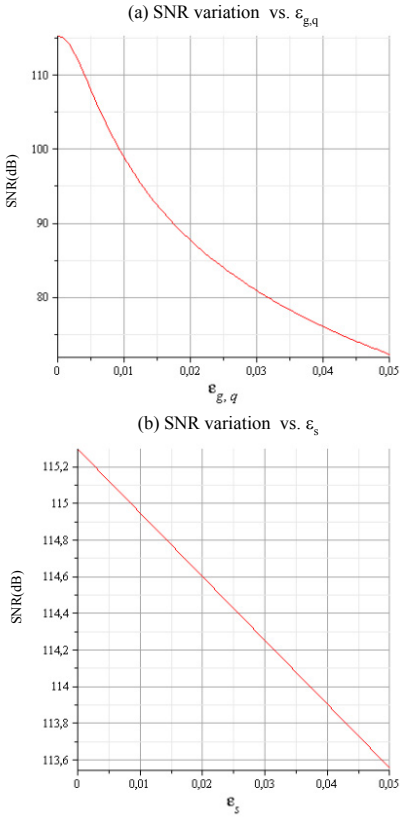
$$H^{int}_{\varepsilon_s}(z)=\frac{\left(1-\varepsilon_s\right)^2 z^{-1}}{1-\left(2\varepsilon_s+\left(1-\varepsilon_s\right)^2\right)z^{-1}+\varepsilon_s{}^2 z^{-2}} \quad (33)$$

Secondly, on their cumulative effects (Equ. 31)

5.1 Effects on dynamic Performances

The ideal transfer function of the integrator presented in Fig. 1 is replaced by the one given in Equ.31, Equ. 32 or Equ. 33. Table 1 shows the simulation parameters. According to Equ.4 to Equ. 6, for typical variations of the error parameters between *0* (the ideal case) and *5%*, Fig. 7 shows the *SNR* variation versus error mechanisms *(ε_g, ε_q and ε_s)*.

Fig. 7(a) and Fig. 7(c) show respectively the separately and the cumulative effect of ε_g and ε_q on the modulator *SNR*. We notice that these errors have a big effect on the *SNR* and their variation destroys the benefits of the oversampling. Unlike, the settling time error ε_s has not a significant effect on the *SNR* since its variation is between 113 and 115dB as shown in Fig. 7(b).



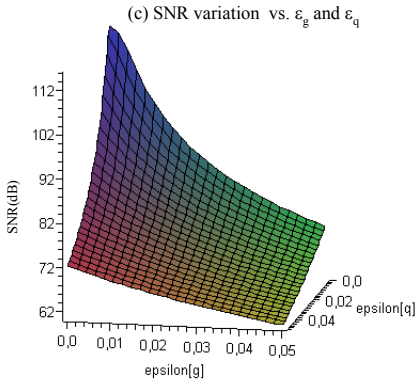


Fig. 7. SNR variation versus SI errors. (a) Influence of $\varepsilon_{g,q}$ (b) Influence of ε_s. (b) Influence of ε_g and ε_q.

Table 1. Simulation Parameters

Simulation parameters	**Value**
Oversampling Ratio (OSR)	*278*
Sampling frequency (fs)	*12.25 Mhz*
Input Signal frequency(f)	*5.4 Khz*
Band of interest (Bw)	*22.05 Khz*
FFT samples number (N)	*65536*

For the effect of these errors on the noise-shaping of ΣΔM, we perform a simulation of the modulator output Power Spectral Density (PSD). As shown in Fig 8(a) and Fig 8(c) the in-band noise increases when ε_g or/and ε_q increase. But in-band noise remains unchanged when ε_s increases as shown in Fig. 8(b). Table 2, Table 3 and Table 4 show respectively the effect of separately and cumulative SI-related errors on dynamic performances and then on the *ENOB*.

The Dynamic Range (DR) of the modulator is given by the difference between the maximum input amplitude and the input amplitude that gives an SNR equal to zero as shown in Fig. 9. For ε_g or ε_q vary from 0% to 5%, DR decrease from 142 to 132dB. For the same variation of ε_s, DR remain unchanged and equal to 142dB.

Table 2. Variation of dynamic performances for $\varepsilon_{g,q}$= *0.1%*, *1%* and *5%*

$\varepsilon_{g,q}$	SNR (dB)	S_THD (dB)	ENOB (bits)
0%(Ideal)	*106.33*	*103.54*	*17.38*
0.1%	*101.96*	*104.82*	*16.65*
1%	*90.41*	*91.25*	*14.74*
5%	*66.71*	*64.08*	*10.80*

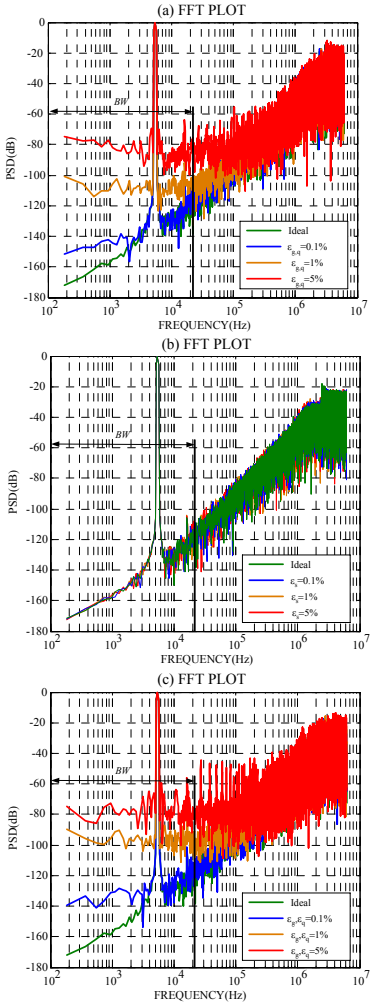


Fig. 8. Output modulator Power Spectral Density. (a) PSD for typical value of $\varepsilon_{g,q}$ (b) PSD for typical value of ε_s. (c) PSD for cumulative effect of ε_g and ε_q

Table 3. Variation of dynamic performances for ε_s= *0.1%*, *1%* and *5%*

ε_s	SNR (dB)	S_THD (dB)	ENOB (bits)
0%(Ideal)	*106.33*	*103.54*	*17.38*
0.1%	*101.61*	*104.42*	*16.59*
1%	*104.32*	*106.57*	*17.05*
5%	*104.91*	*105.71*	*17.14*

Table 4. Variation of dynamic performances for ε_g and ε_q= *0.1%*, *1%* and *5%*

ε_g andε_q	SNR (dB)	S_THD (dB)	ENOB (bits)
0%(Ideal)	*106.33*	*103.54*	*17.38*
0.1%	*102.71*	*100.85*	*16.78*
1%	*80.02*	*78.81*	*13.01*
5%	*61.03*	*55.40*	*9.85*

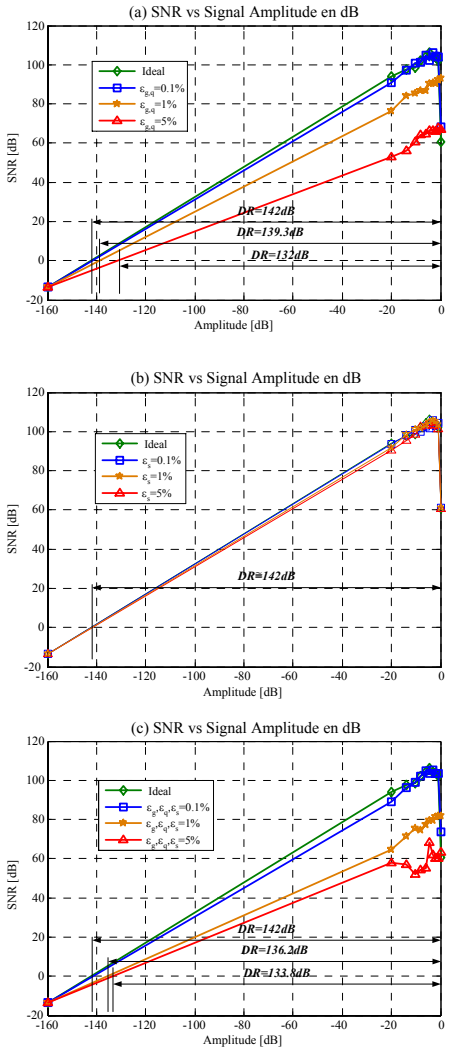


Fig. 9. SNR vs. Amplitude (dB). (a) For typical value of $\varepsilon_{g,q}$ (b) For typical value of ε_s. (c) For cumulative effect of ε_g,ε_q and ε_s.

5.2 Effects on static performances

According to [27-29], when characterizing an imperfect modulator, we intend to find its DC offset and gain. The DC I/O transfer curve characterizes the non-ideal modulator better than the Integral/*D*ifferential non Linearity (INL/DNL). The output bit stream of an ideal modulator, for a rational DC input value x, is a series of repetitive patterns which the base one are called limit cycle. The average over a complete period is equal to x. As shown in Fig. 10(b) the limit cycle is not affected when the settling time error ε_s vary. But, we notice that, from Fig. 10(a) and Fig. 10(c), the limit cycle is invariable in the range of input within [-0.01, 0.01] for separately variation of ε_g or ε_q. For cumulative effect, the limit cycle is constant for a range of input [-0.04, 0.04].

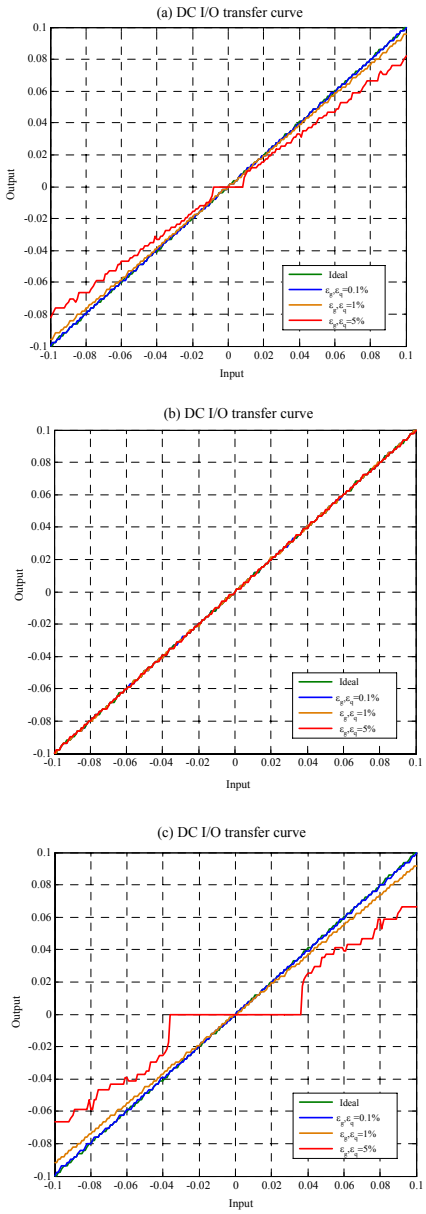


Fig. 10. DC I/O modulator transfer curve. (a) For typical value of $\varepsilon_{g,q}$ (b) For typical value of ε_s. (c) For cumulative effect of ε_g and ε_q

6 Conclusions

A behavioral study regarding to the non-idealities of SI memory cell has been detailed. This study has been extended to a higher level such as integrator and then modulator. An erroneous Non-inverting Lossless Integrator transfer function has been developed. The simulation results show the influence of these non idealities on the dynamic and static performances on the 2nd order SI-LPΣΔM. We can conclude that I/O conductance ratio as well as charge injection errors have a remarkable effect on both dynamic and static performances. Unlike, settling time error has not a significant effect on the modulator output. Future

work will be focused on test and calibration of the modulator in order to minimize the effect of these errors and improve performances of SIΣΔ–ADC.

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