The Counterfeit Components V-I Characteristics Difference Study

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Abstract: - The electronic component V-I characteristics express a relationship between the current flowing via a chosen couple of pins, and the voltage applied on those pins. That voltage varies between two safe, for the component health limits, during the V-I characteristic recording. The applied voltage variation follows a certain function like sinus or ramp. The V-I characteristics of an individual component type can differ according to production technology, according to a particular manufacturer, or according to measurement conditions itself. Those so called natural differences can be registered by the study of statistically significant component population with known origin and history, and they can be subsumed in the comparison master pin print. That comparison master pin print is subsequently used as a criterion for discovering differences caused by improper treatment, failure or by the counterfeiting process. The article illustrates a counterfeit detector application for comparative V-I characteristics analysis aimed at a relevant knowledge base development for particular production technologies and component types.

Key-Words: - counterfeit component, counterfeit detector, V-I characteristic, scan profile, pin print, comparison criteria, master component

1 Introduction

The method of electronic component V-I characteristic displaying has been using for circuit and component failure diagnostics quite a long time. Its recent remarkable revival was caused both by counterfeit component occurrence increase and by the curve tracers sophisticated circuitry design noticing even small differences between the master and analysed component characteristics. Such devices have a possibility to set applied safe voltage sweep range, source internal resistance to limit the current through the component pin couple, and also the way the pin couples are created for V-I characteristic analysis. The evaluation criteria can be set according to the permissible variances related to the component type and its application in the particular circuit. Each analysis can be documented with the predefined report comprising evaluation criteria, pin results summary, and all pin V-I characteristics overview.

As there is no universally valid criterion for component V-I characteristic difference assessment, it is necessary to create a set of measurements for every component type to be able to estimate the degree of variation in the component V-I characteristic shape at the particular producer or supplier. The ambient temperature influence and the characteristic time stability have to be taken into account as well. The goal is to restrict the potentiality of analysis result misinterpretation. Only in case of more distinctive difference, there is a reason to consider a relation to a certain component internal structure change caused by the external influence or by the fact that it is a counterfeit component.

We can encounter counterfeited products at various complexity levels and in various product commodities. In the area of electronics, we can encounter not only established brand counterfeited devices like satellite receivers, mobile phones, and GPS navigation units. We are unfortunately encountering also counterfeited electronic components in a dramatically increasing rate in course of recent years. The counterfeit components range over the passive and active components from stable precise resistors up to sophisticated integrated circuits. The counterfeit components penetration in supply chains threatens not only consumer electronic products quality and reliability, but also all sensitive systems in medical electronics, automation and control systems, weapon systems, civil and military aviation systems, space research systems etc. [1].

The counterfeit component infiltration in product assemblies are influenced and promoted by several

factors. Accessibility and price are playing a very important role. Cost reduction pressure may favour interesting price offers not only at up-to-date components supply limited by the lead phase of production, but also at obsolete components needed for long life equipment maintenance and service [3].

There exists a wide variety of counterfeit components on the market. One extreme represents a chip-less package with relevant pin count and package labelling. On the other hand, we can encounter very elaborate counterfeit integrated circuit parametrically almost identical with original component, but for instance with reduced reliability, narrower application temperature range, latent damages, or with other dissimilarities hardly detectable by the immediate measurement and simple analysis with common apparatus. Such components should undergo long time testing in a statistical set and in conditions supporting the manifestation of pertinent dissimilarities [5].

The authenticity test methods can be basically branched as destructive and non destructive. Destructive methods require special equipment and tooling, for example a de-capsulation set for component package opening to find out whether the circuit system type and origin corresponds with the package labelling. Non-destructive methods encompass mainly costly analytical equipments like micro-focus X-ray units, ultrasound scanning microscopy and others [4][7][8]. We need reference original component sample for comparative analysis for majority of these methods.

However, we can use also quite simple and cheaper methods for a preliminary identification and assessment of suspect components. The visual and simple optical analysis of component appearance, component labelling including producer logo, accompanying documentation check, package dimensional and shape analysis, pin condition analysis belong among such widely accessible methods [5]. The appearance analysis combined with an affordable component electric analysis constitutes an efficient tool applicable also outside the specialized laboratories. The knowledge of related technology and physical background can also help for internal structure possible changes identification if possible at all [9].

Just V-I characteristics comparative analysis offers an interesting preventive method for relatively quick, simple and accessible new source component evaluation. Moreover, that methods is still applicable for a standard diagnostics studies of technological and mistreatment consequences on the component with V-I characteristics recorded in advance.

2 V-I characteristic analysis modes

The V-I characteristic recording preparation starts with a suitable pin couple choice for the measurement voltage application and response current registering. The choice is apparent at two terminals component like resistor, capacitor, or diode. The pin combination method for the analysis couple at more than two terminals component depends mainly on its inclination to V-I characteristic change caused by different external or internal influences. Generally speaking, the pin pair can be created from any two pins combination.

We are using the Sentry counterfeit IC detector by ABI Electronics Ltd. in our diagnostic laboratory. That device has 256 independent and identical measurement channels which can be arbitrarily connected to all component pins providing their count is not higher than 256. In case of pin count higher than 256, the measurement performs successively in more than one step. There exists a wide range of package contact adapters for THT and SMD package components. Components with smaller pin count can be analysed in corresponding package groups at the same time [6].

We can choose from three variants for component pin combination at the Sentry device. The Normal Mode combines all pins with the common pin like V_{ss} or GND pin at integrated circuits. Transistors are free to choose any pin as the common pin. We talk about referring all pins to a chosen one. The Matrix Mode creates all possible pin combinations in successive couples. The preference for the Normal Mode or for the Matrix Mode depends on the particular component type and its production technology. The basic criterion for such choice is the higher sensitivity for V-I characteristic change because of monitored phenomenon at compared component. That sensitivity may differ at each Mode and for a particular component situation so that neither Normal Mode nor Matrix Mode has a general priority in advance. There is more or less no difference between both modes at two pins components like resistors, capacitors and diodes. We can only distinguish the measuring signal ramp direction (positive or negative) with them if it could have any benefit because of V-I characteristic shape.

The Sentry device has one more Mode called Automatic. That mode combines pins in a couple according to the current magnitude flowing via that couple. It prefers higher magnitudes and excludes combinations with very small or zero current. That mode is a supplementary mode because we have necessary technical specifications at our disposal and a verified component master in most cases so

that we can use the grounding pin (V_{SS}) as a reference pin in Normal Mode.

Fig.1 illustrates the V-I characteristic example for pin 1 referred to the ground pin 9 at the master integrated circuit HT 46R47 recorded with Sentry in Normal Mode.

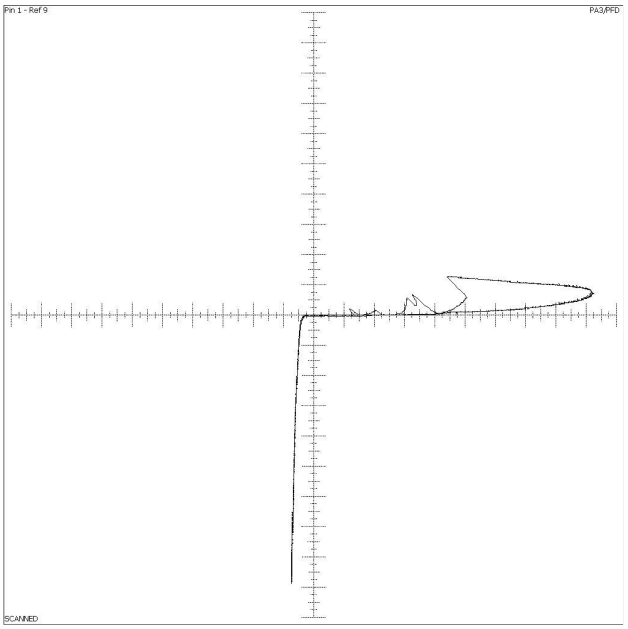

Fig.1 Pin 1 V-I characteristic of a good circuit.

Fig. 2 illustrates an example of a failure V-I characteristic deformation at the same pin 1 referred to pin 9 in Normal Mode for the faulty integrated circuit HT46R47 recorded in our laboratory.

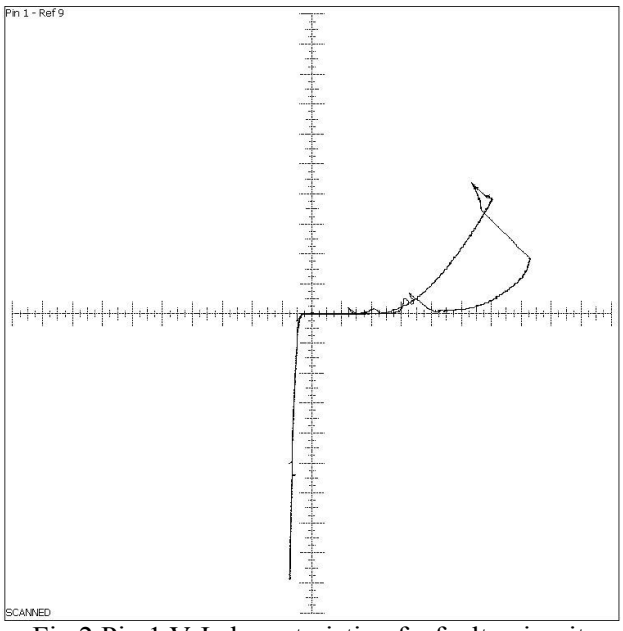

Fig.2 Pin 1 V-I characteristic of a faulty circuit.

As we have experienced, the sensitivity to differences can be very similar for all three pins successively in the role of reference at transistors, or some reference configurations can be more sensitive unlike the others. Fig. 3 displays a master transistor V-I characteristics of the Source referred to the Drain in Normal Mode.

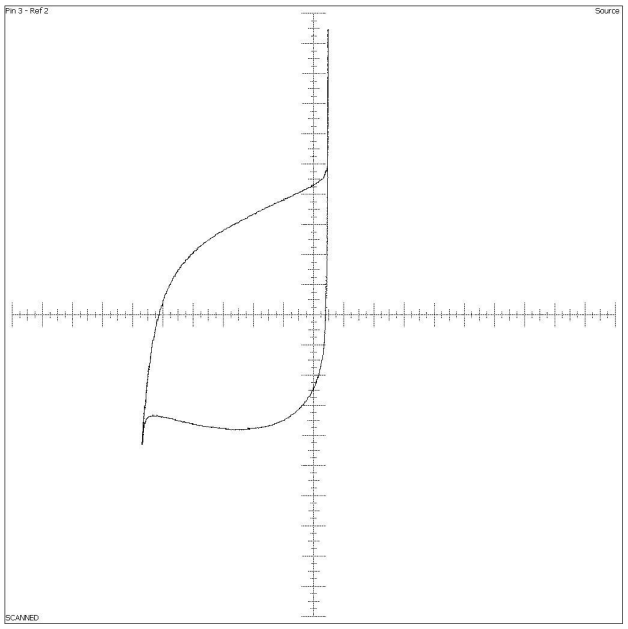

Fig.3 MOSFET transistor Source referred to Drain V-I characteristic example in Normal Mode.

Fig. 4 shows master transistor V-I characteristics example recorded in Matrix Mode.

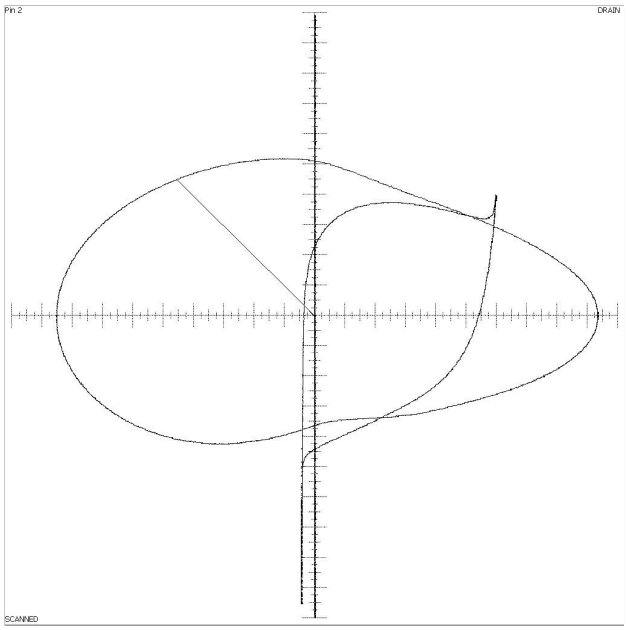

Fig.4 MOSFET transistor Drain referred to all other pins V-I characteristic example in Matrix Mode.

The so called pin print of a master component can be stored in memory and used as a comparison reference for all analysed components later on.

3 Real samples experimental analysis

The experimental analysis has been performed on components used for electronic modules assemblies in a current industrial production. One sample group marked as ***A*** group comprised Cool MOS power enhanced N channel transistor (20N60C3). The second sample group marked as ***B*** group comprised MOSFET Fast diode SuperMESH enhanced N channel power transistor (D4NK50ZD). The cooperating partner specified one master transistor and three others to be analysed in group ***A***. Group ***B*** comprised 5 undistinguished transistors without any reference master defined in advance.

As already mentioned above, the V-I characteristic differences can be caused not only by the fact that they are counterfeited, but also production process differences at the same component type but from different producers can exhibit certain characteristic variation without functionality influence on a particular application. We can register slight differences even among various lots at the same producer. On the other hand, V-I characteristic changes caused by thermal exposition and electrostatic discharge exposition can help to trace the component history and the way of treatment.

Table 1 indicates the V-I characteristic scan parameters used for both transistor groups.

Scan Profile	
Voltage Range:	±10V
Waveform:	Sine
Source Resistance:	100 kOhm
Frequency:	100 Hz

Table 1 Scan Profile set for both transistor groups.

Table 2 indicates all comparison criteria levels used for both transistor groups.

Comparison Criteria			
Horizontal Tolerance:	3%	Vertical Tolerance:	3%
Pin Fail Tolerance:	75%	Pin Suspect Tolerance:	95 %
Fail if Fails Tolerance:	5%	Fail if Suspects Tolerance:	15 %
Suspect if Fails Tolerance:	3%	Suspect if Suspect Tolerance:	10 %

Table 2 Comparison Criteria set for both transistor groups.

Our transistor samples were not obvious counterfeits. The group ***A*** was created by one master transistor with known history and three samples from an alternative source and with a different lot code. Group ***B*** comprised of 2 transistors with one lot code and 3 transistors with another lot code. No master was defined in advance in group ***B***. The V-I characteristic comparison analysis has confirmed the lot code sub-grouping.

The reference pin for Normal Mode was successively chosen Gate, Drain and Source pin to compare all three choices from the sensitivity-to-changes point of view. The group ***A*** Normal Mode results did not show noticeable differences related to the reference pin choice.

The following figures display recorded master V-I characteristics and comparative characteristics for Normal Mode in Group ***A*** successively for reference pin Drain, Gate, and Source.

Fig. 5 displays Group ***A*** master transistor pin 1 (Gate) referred to pin 2 (Drain) V-I characteristic in Normal Mode.

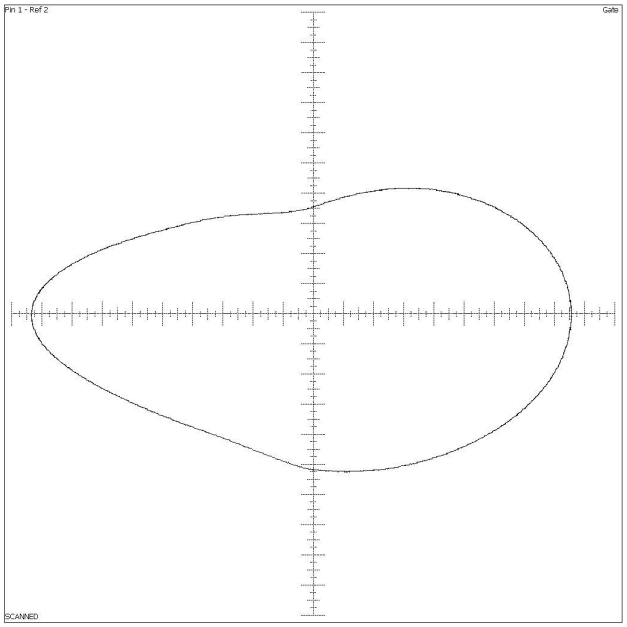

Fig.5 Group ***A*** Master transistor Gate pin 1 referred to Drain pin 2 V-I characteristic in Normal Mode.

The pin 3 (Source) referred to pin 2 (Drain) of this master transistor is in the Fig. 3. Fig.6 displays the comparative V-I characteristic of the same pin and its reference for the first analysed transistor in group ***A***. The tolerance range for both vertical and horizontal direction was set to 3% according to the Table 2. The similarity evaluation algorithm calculates the compared V-I characteristic dots percentage included in the set tolerance area as the ratio of that dots included in the area to all dots number of the compared component pin couple V-I characteristic. That percentage of similarity is in each comparison result figure comment indicated in parenthesis.

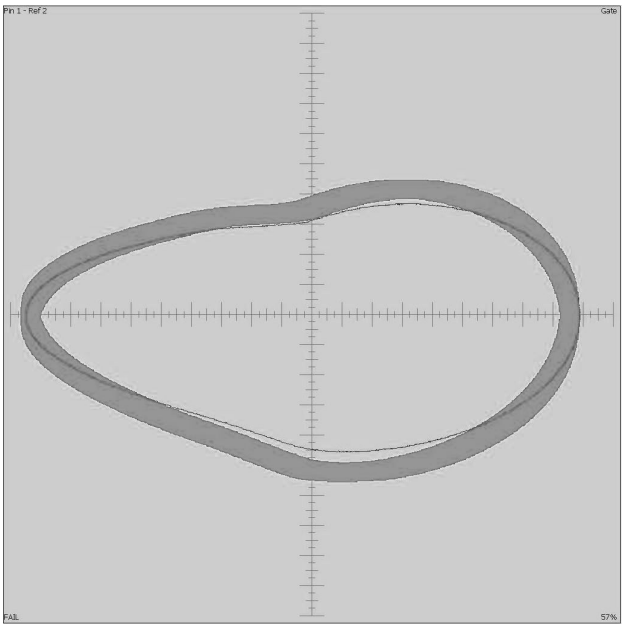

Fig.6 Group ***A*** analysed first transistor Gate pin referred to Drain pin result in Normal Mode (57%).

Fig.7 displays the comparison result for pin 3 (Source) referred to pin 2 (Drain) of the first analysed transistor in group ***A***.

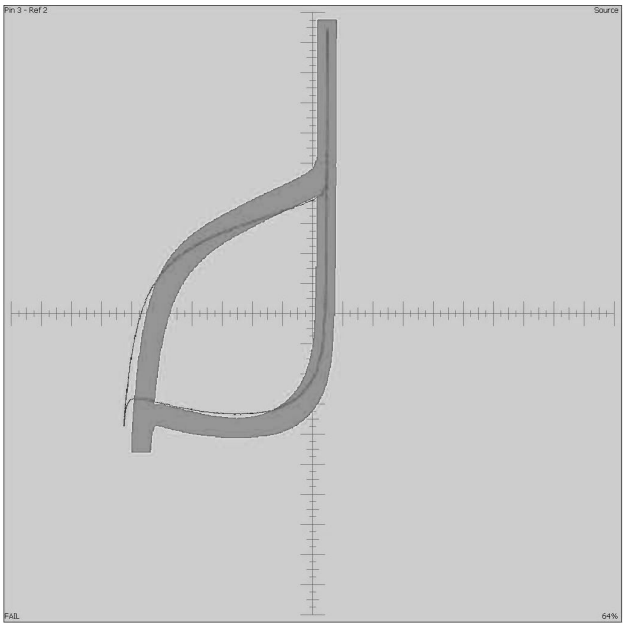

Fig.7 Group ***A*** analysed first transistor Source pin referred to Drain pin result in Normal Mode (64%).

Fig.8 displays the comparison result for pin 1 (Gate) referred to pin 2 (Drain) of the second analysed transistor in group ***A***.

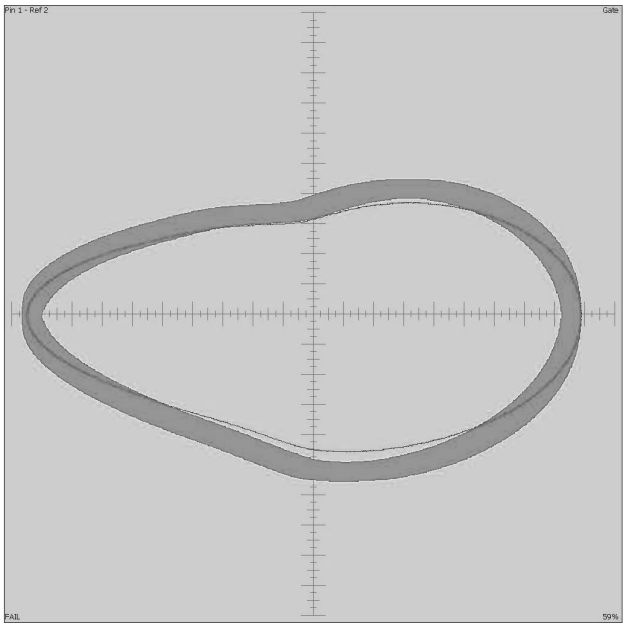

Fig.8 Group ***A*** analysed second transistor Gate pin referred to Drain pin result in Normal Mode (59%).

Fig. 9 displays the comparison result for pin 3 (Source) referred to pin 2 of the second analysed transistor in group ***A***.

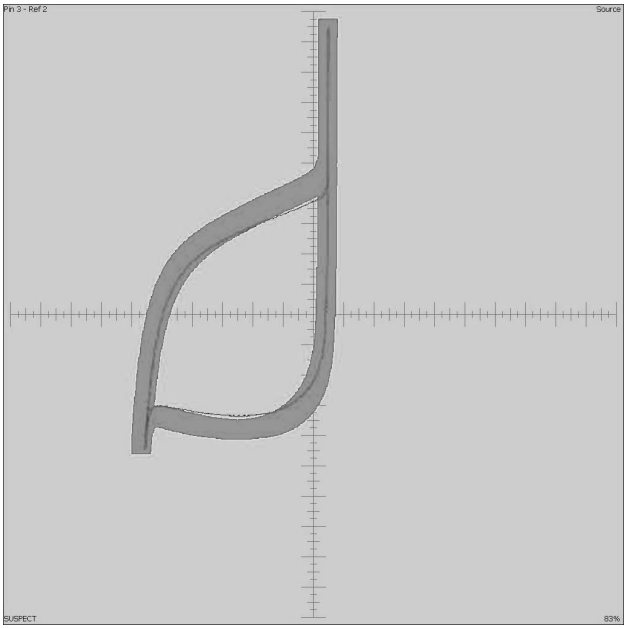

Fig.9 Group ***A*** analysed second transistor Source pin referred to Drain pin result in Normal Mode (83%).

Fig.10 displays the comparison result for pin 1 (Gate) referred to pin 2 (Drain) of the third analysed transistor in group ***A***.

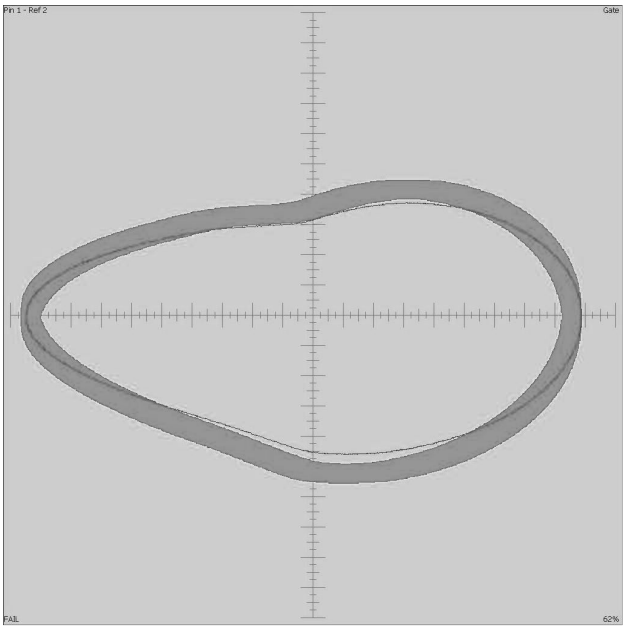

Fig.10 Group ***A*** analysed third transistor Gate pin referred to Drain pin result in Normal Mode (62%).

Fig.11 displays the comparison result for pin 3 (Source) referred to pin 2 (Drain) of the third analysed transistor in group ***A***.

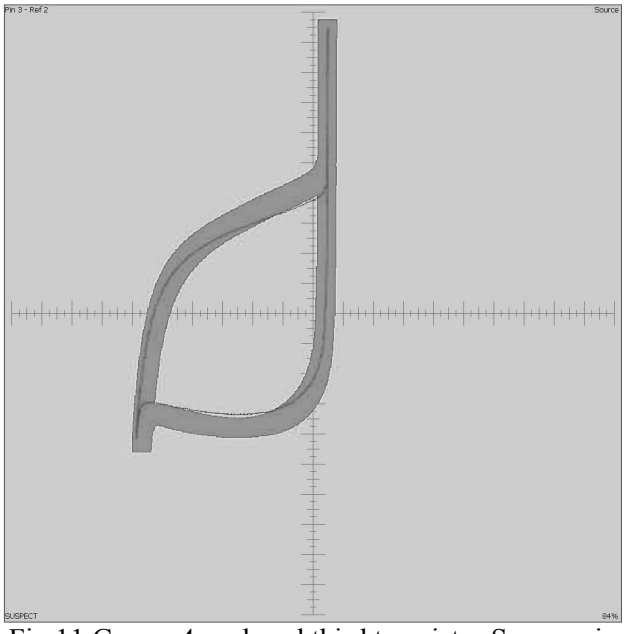

Fig.11 Group ***A*** analysed third transistor Source pin referred to Drain pin result in Normal Mode (84%).

Fig.12 displays Group ***A*** master transistor pin 2 (Drain) referred to pin 1 (Gate) V-I characteristic in Normal Mode.

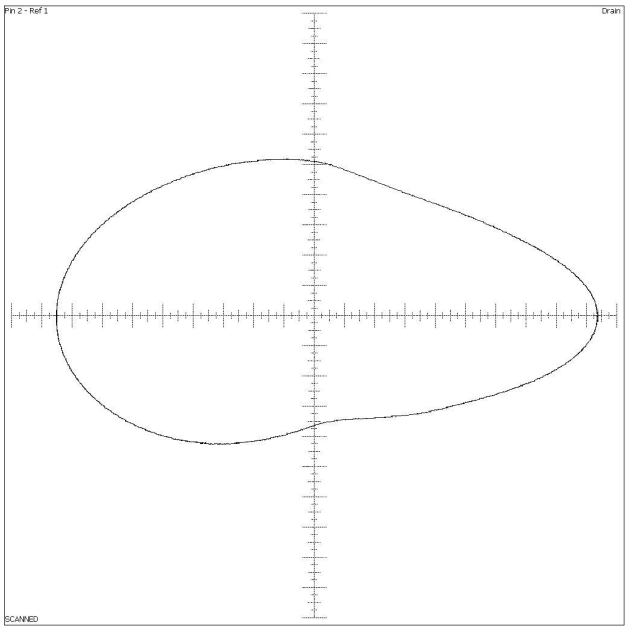

Fig.12 Group ***A*** Master transistor Drain pin referred to Gate pin V-I characteristic in Normal Mode.

Fig.13 displays Group ***A*** master transistor pin 3 (Source) referred to pin 1 (Gate) V-I characteristic in Normal Mode.

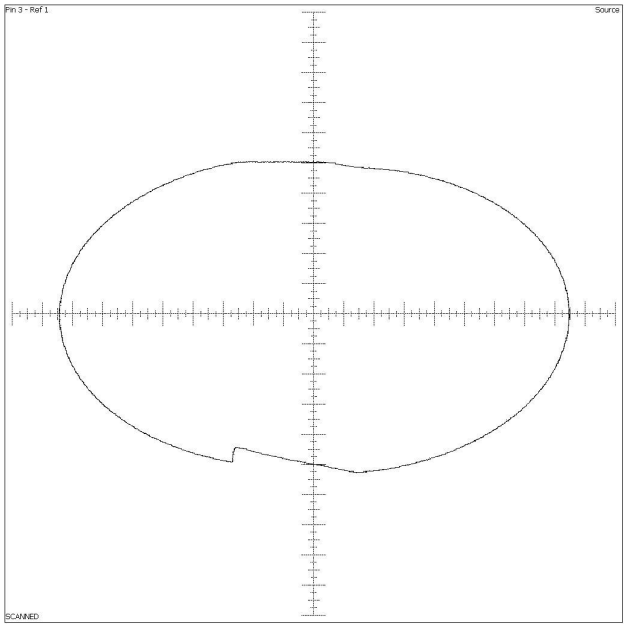

Fig.13 Group ***A*** Master transistor Source pin referred to Gate pin Normal Mode characteristic.

Fig.14 displays the comparison result for pin 2 (Drain) referred to pin 1 (Gate) of the first analysed transistor in group ***A***.

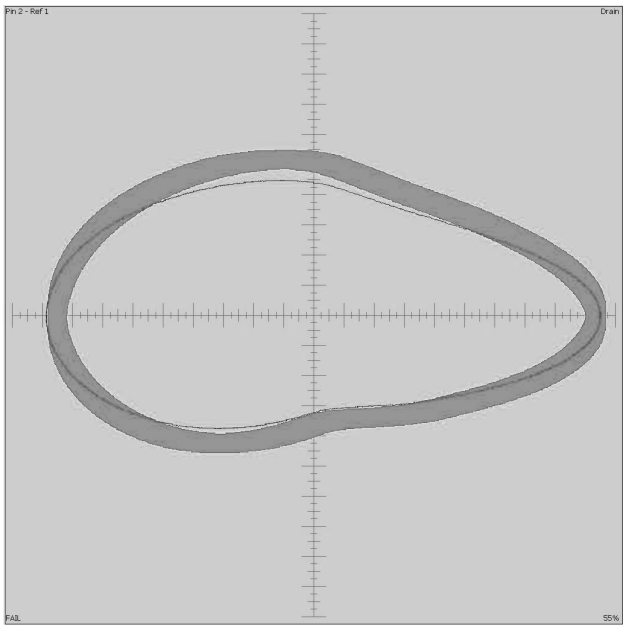

Fig.14 Group ***A*** analysed first transistor Drain pin referred to Gate pin result in Normal Mode (55%).

Fig.15 displays the comparison result for pin 3 (Source) referred to pin 1 (Gate) of the first analysed transistor in group ***A***.

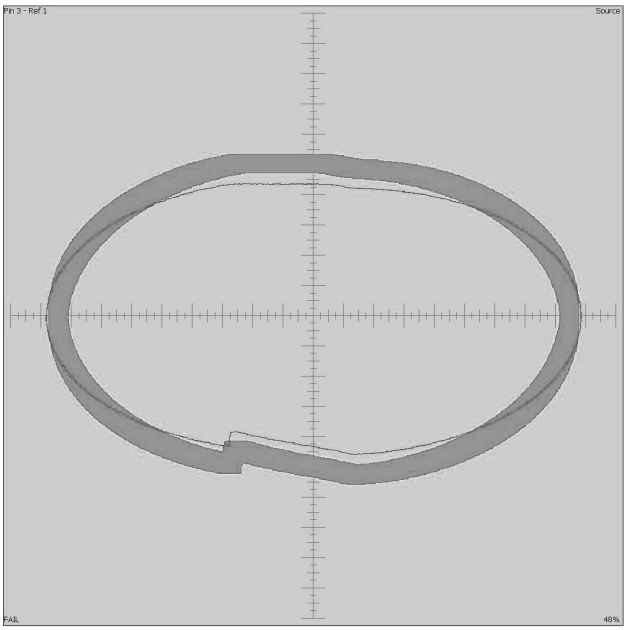

Fig.15 Group ***A*** analysed first transistor Source pin referred to Gate pin result in Normal Mode (48%).

Fig.16 displays the comparison result for pin 2 (Drain) referred to pin 1 (Gate) of the second analysed transistor in group ***A***.

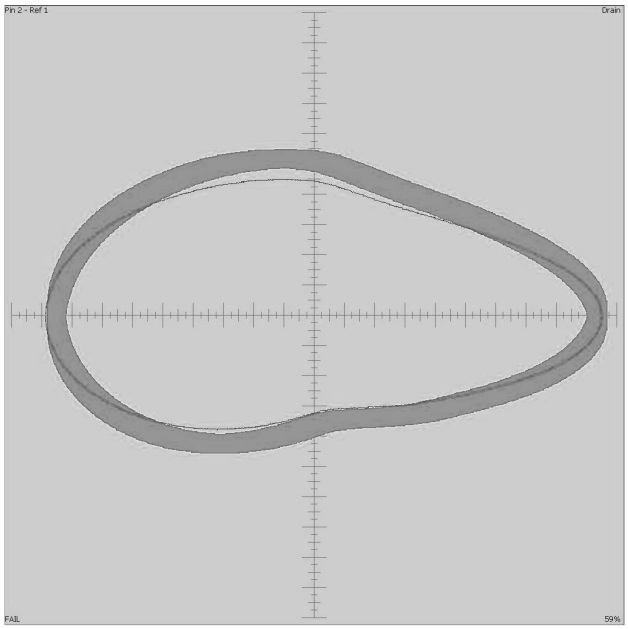

Fig.16 Group ***A*** analysed second transistor Drain pin referred to Gate pin result in Normal Mode (59%).

Fig.17 displays the comparison result for pin 3 (Source) referred to pin 1 (Gate) of the second analysed transistor in group ***A***.

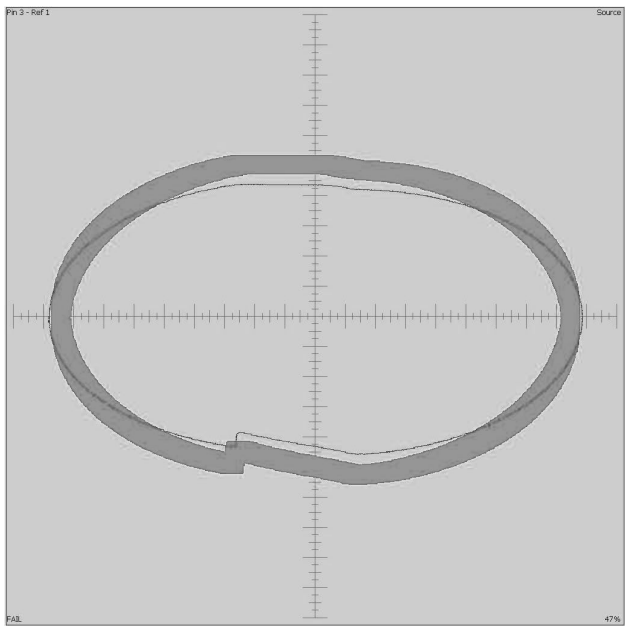

Fig.17 Group ***A*** analysed second transistor Source pin referred to Gate pin result in Normal Mode (47%).

Fig.18 displays the comparison result for pin 2 (Drain) referred to pin 1 (Gate) of the third analysed transistor in group ***A***.

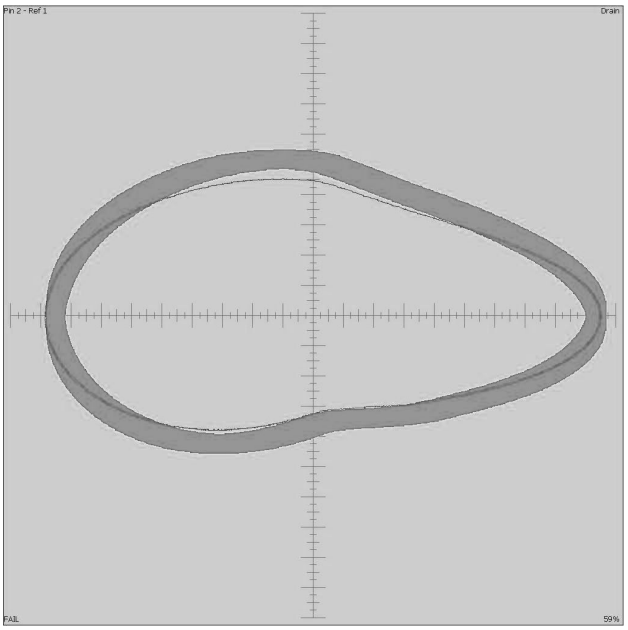

Fig.18 Group ***A*** analysed third transistor Drain pin referred to Gate pin result in Normal Mode (59%).

Fig.19 displays the comparison result for pin 3 (Source) referred to pin 1 (Gate) of the third analysed transistor in group ***A***.

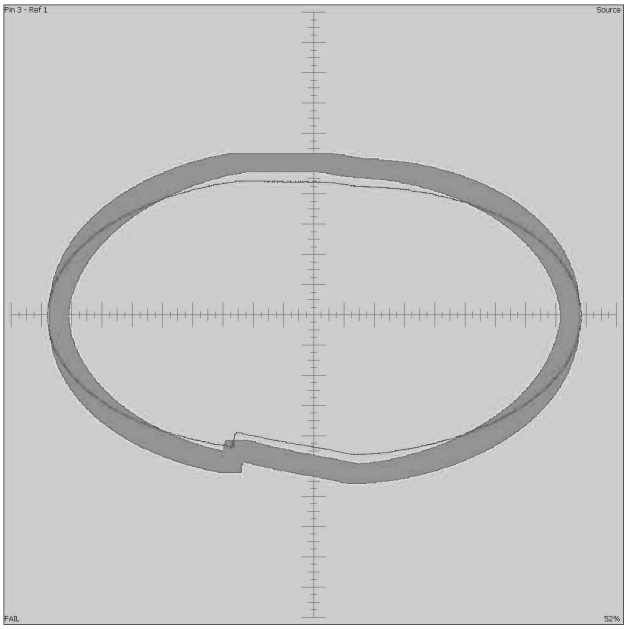

Fig.19 Group ***A*** analysed third transistor Source pin referred to Gate pin result in Normal Mode (52%).

The analysis results for the whole group have been arranged in following Tables 3 to 5 according to the analytical mode and reference pin to make results more readable. The comparison results for individual pins and transistors are highlighted in gray scale (originally in relevant colours) according to the tolerance range classification (see Table 2) – SUCCESS, SUSPECT, FAIL. Numbers indicate the similarity percentage. The FAIL level dissimilarities are highlighted in dark.

20N60C3				
Sample	MATRIX MODE			Result
	Pin1	Pin2	Pin3	
M	100	100	100	Ref
1	90	92	88	fail
2	90	97	91	fail
3	93	98	94	fail

Table 3 Group ***A*** in Matrix Mode Comparison Results Overview.

20N60C3				
Sample	NORMAL MODE Ref – 1 (Gate)			Result
	Pin1	Pin2	Pin3	
M	100	100	100	Ref
1	100	55	48	fail
2	100	59	47	fail
3	100	59	52	fail

Table 4 Group ***A*** in Normal Mode with Reference Pin 1 Comparison Results Overview.

20N60C3				
Sample	NORMAL MODE Ref – 2 (Drain)			Result
	Pin1	Pin2	Pin3	
M	100	100	100	Ref
1	57	100	64	fail
2	59	100	83	fail
3	62	100	84	fail

Table 5 Group ***A*** in Normal Mode with Reference Pin 2 Comparison Results Overview.

20N60C3				
Sample	NORMAL MODE Ref – 3 (Source)			Result
	Pin1	Pin2	Pin3	
M	100	100	100	Ref
1	49	65	100	fail
2	48	83	100	fail
3	52	75	100	fail

Table 6 Group ***A*** in Normal Mode with Reference Pin 3 Comparison Results Overview.

We can see that there are only inessential differences between the master transistor and the analysed group in Matrix Mode. In contrary, the

differences in Normal Mode are more significant for all three reference pin variants.

The analysed transistor group ***B*** had inessential differences only for reference pin 1 (Gate) in Normal Mode. All other comparison variants including Matrix Mode have approvingly separated that group in two subgroups according to the lot codes. The sub-grouping was realised first according to the V-I characteristic comparative analysis and only then, the lot codes were checked. The lot code sub-grouping has confirmed the analysis results.

The following Figures 20 to 24 displaying characteristics in Matrix Mode for the group ***B***. The Matrix Mode characteristics have been chosen as an illustration to complete the idea about another analysis variant to the Normal Mode.

Fig.20 displays the master V-I characteristics in Matrix Mode of the randomly chosen transistor in group ***B***.

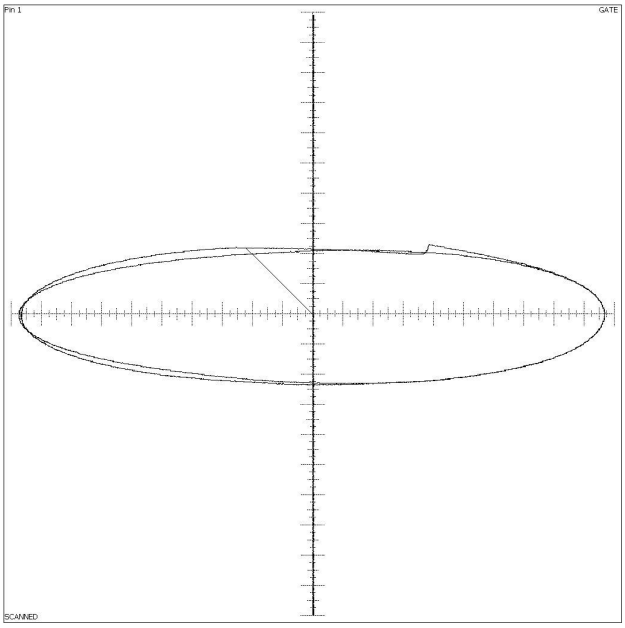

Fig. 20 Group ***B*** master transistor Gate pin V-I characteristics in Matrix Mode.

Figures 21 to 24 illustrate the comparison with all other transistors in that group results for pin 1 (Gate) combined successively with pin 2 (Drain) and pin 3 (Source) in one scan cycle.

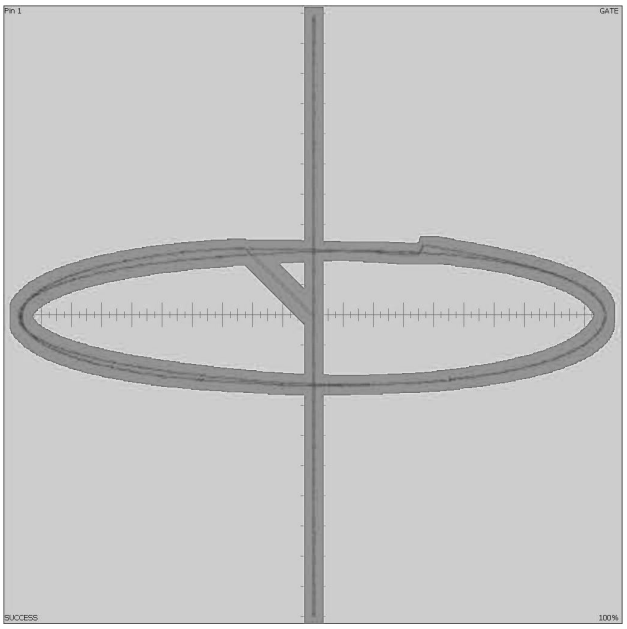

Fig.21 Group ***B*** analysed second transistor Gate pin result in Matrix Mode (100%).

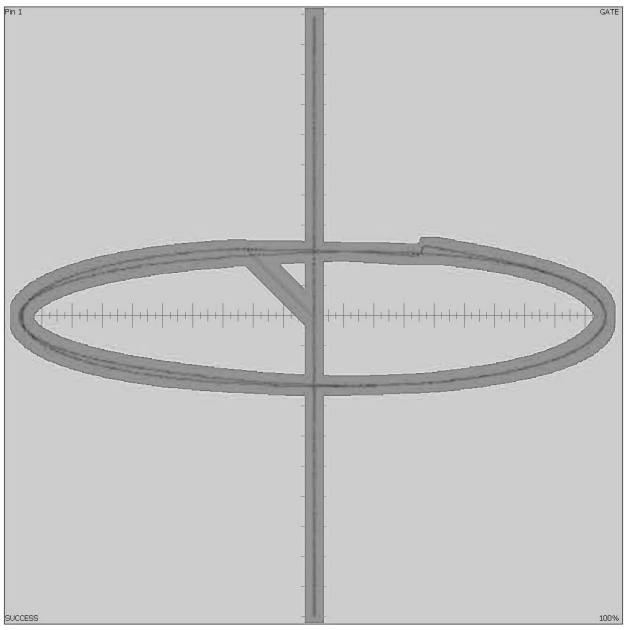

Fig.22 Group ***B*** analysed third transistor Gate pin result in Matrix Mode (100%).

The form of V-I characteristic can be individually influenced by the scan frequency and test voltage source internal resistance according to the component type.

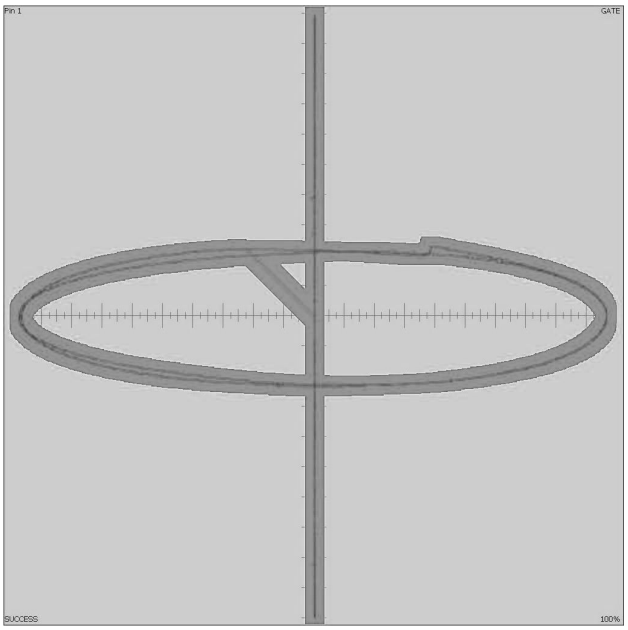

Fig.23 Group ***B*** analysed fourth transistor Gate pin result in Matrix Mode (100%).

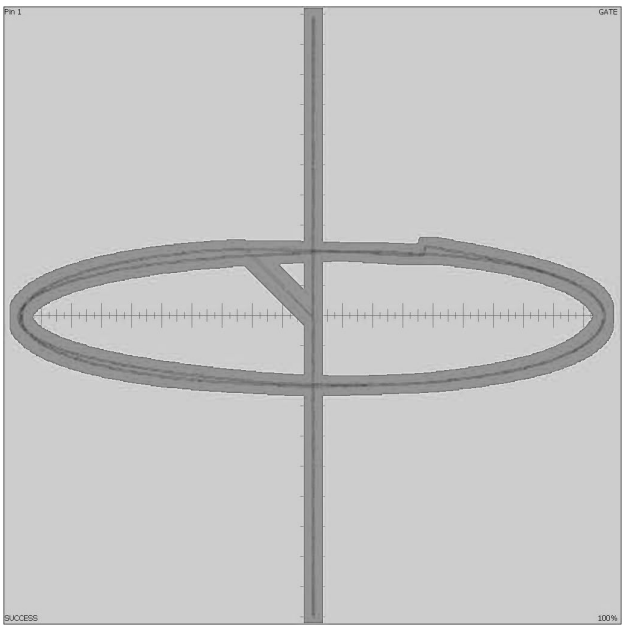

Fig.24 Group ***B*** analysed fifth transistor Gate pin result in Matrix Mode (100%).

The following Figures 25 to 29 are displaying master V-I characteristics in Matrix Mode of the same randomly chosen transistor in group ***B*** and the comparison results for pin 2 (Drain) with other transistors in that group.

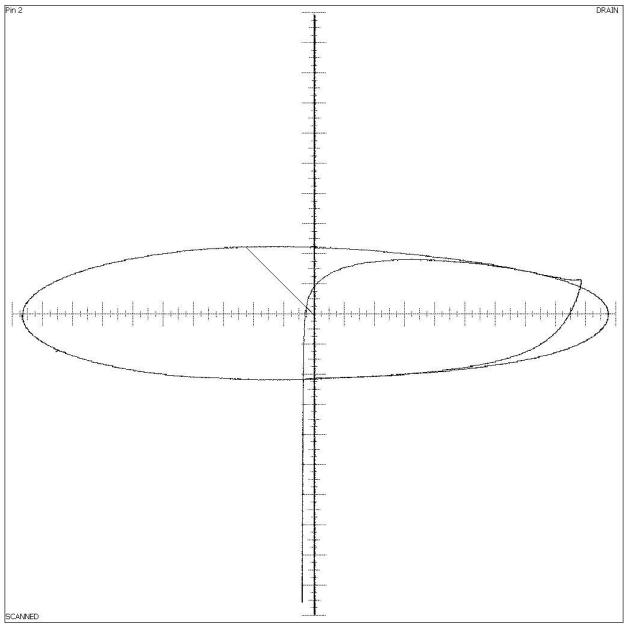

Fig.25 Group ***B*** master transistor Drain pin V-I characteristics in Matrix Mode.

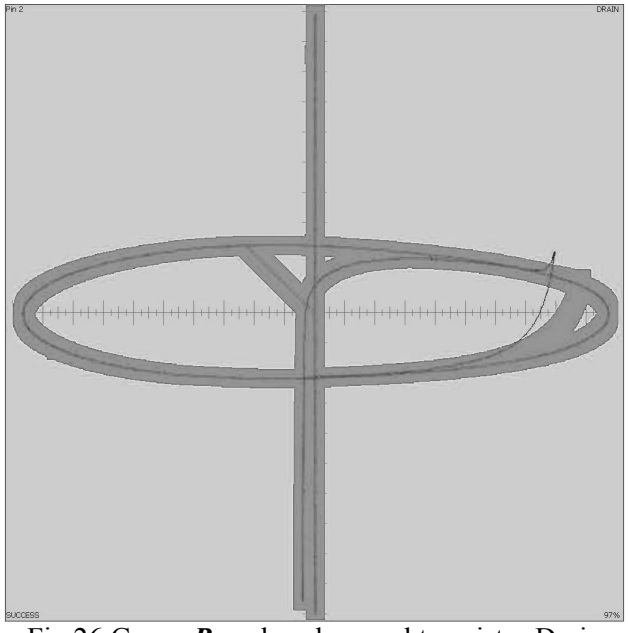

Fig.26 Group ***B*** analysed second transistor Drain pin result in Matrix Mode (97%).

The Matrix Mode tolerance range area can mask slight differences between the master pin print and the compared component characteristics in certain cases because of individual pin V-I characteristic tolerance areas overlapping.

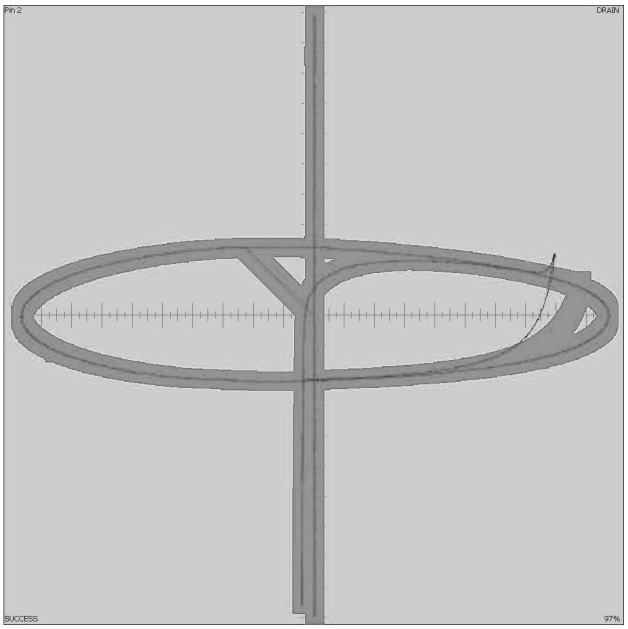

Fig.27 Group ***B*** analysed third transistor Drain pin result in Matrix Mode (97%).

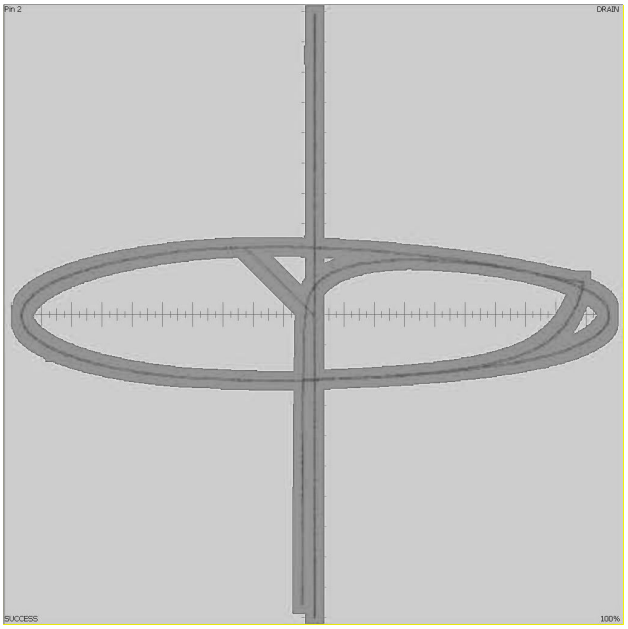

Fig.28 Group ***B*** analysed fourth transistor Drain pin result in Matrix Mode (100%).

The decision whether to use Matrix Mode or Normal Mode for traced differences evaluation depends exclusively on particular data collected for the respective authentic component type. The authentic component pin print dispersion applies for comparison criteria settings, and component pins classification in fixed categories – SUCCESS, SUSPECT, and FAIL.

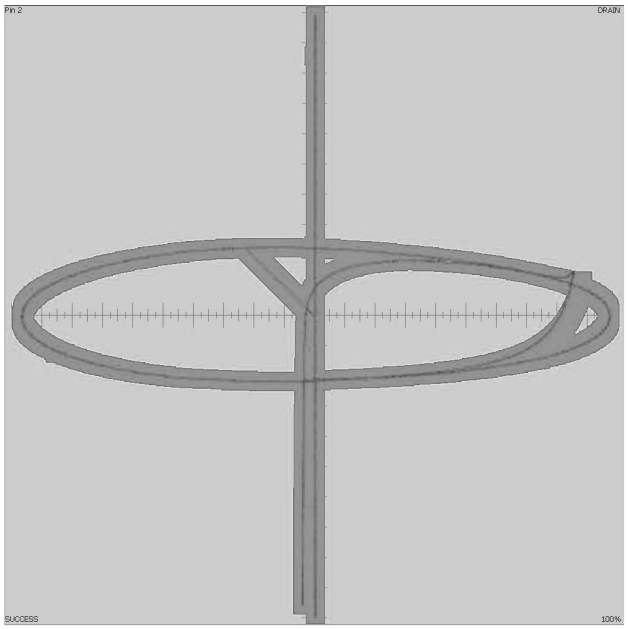

Fig.29 Group ***B*** analysed fifth transistor Drain pin result in Matrix Mode (100%).

The following Figures 30 to 34 are displaying master V-I characteristics in Matrix Mode of the same randomly chosen transistor in group ***B*** and the comparison results for pin 3 (Source) with other transistors in that group.

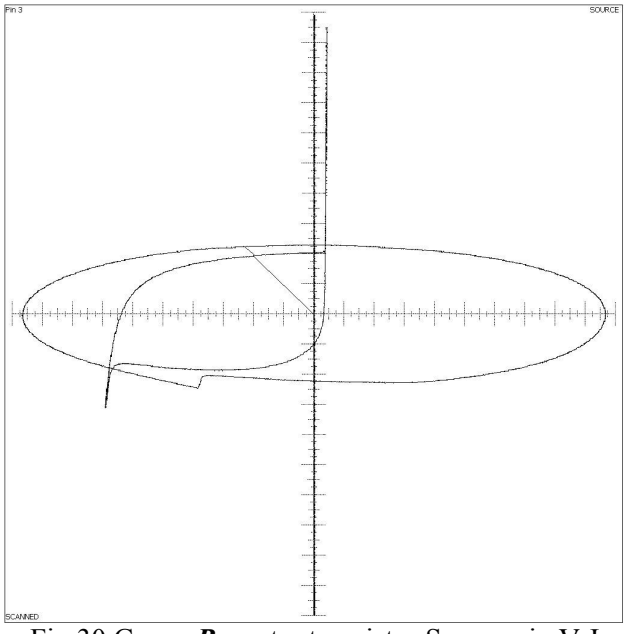

Fig.30 Group ***B*** master transistor Source pin V-I characteristics in Matrix Mode.

Each picture holds the pin number and its function label entered during component entry.

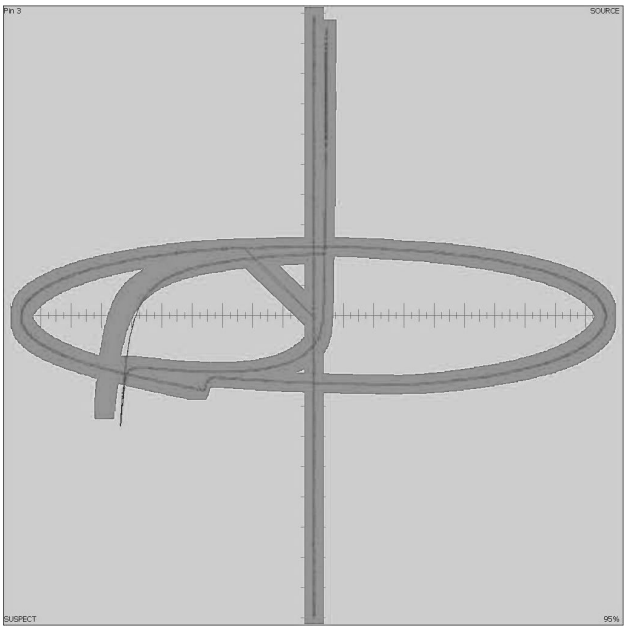

Fig.31 Group ***B*** analysed second transistor Source pin result in Matrix Mode (95%).

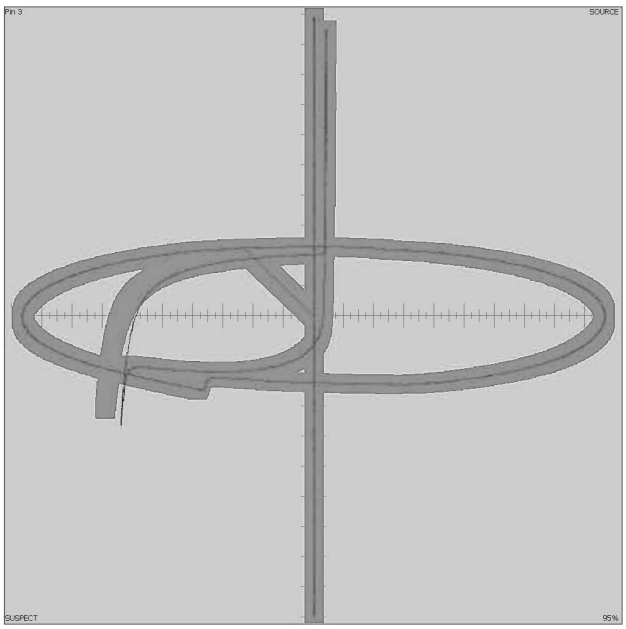

Fig.32 Group ***B*** analysed third transistor Source pin result in Matrix Mode (95%).

The comparison results in group ***B*** are indicating that differences between both sub-groups are not so significant, and that they can be imputed to lot differences. The Sentry device horizontal and vertical tolerance range can be set symmetrically from a very strict level of 0.1% up to 5% in 0.1% steps. Our experience so far points to the tolerance range level of 3% for common diagnostic evaluations, and 5% for coarse differences.

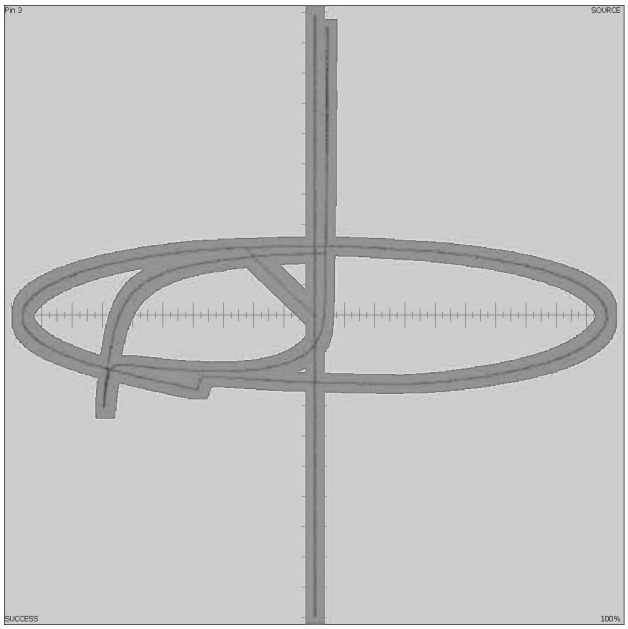

Fig.33 Group ***B*** analysed fourth transistor Source pin result in Matrix Mode (100%).

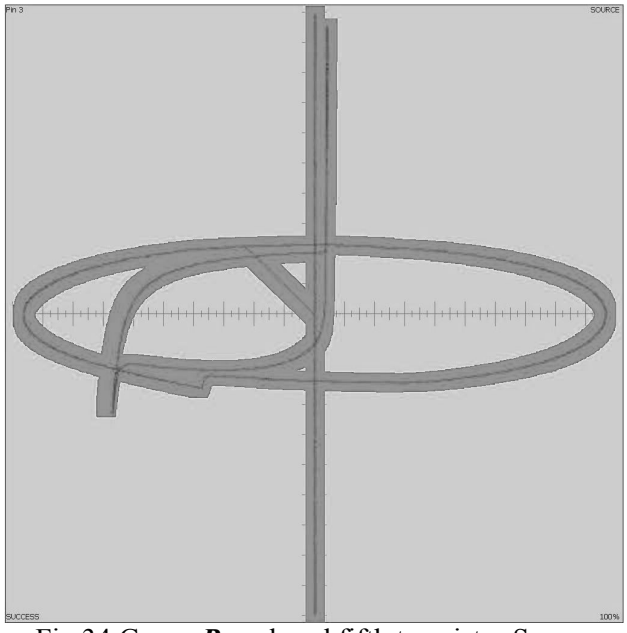

Fig.34 Group ***B*** analysed fifth transistor Source pin result in Matrix Mode (100%).

The following Tables 7 to 10 display the group ***B*** comparison results according to the mode and to the Normal Mode reference pin variant in summary. Table 7 sums up the group ***B*** transistors results in Matrix Mode and with transistor sample 1 chosen randomly as a comparison master for all analysis variants. Numbers indicate the similarity percentage. The dissimilar sub-group consisting from samples 2 and 3 is highlighted dark.

ST D4NK50ZD				
Sample	MATRIX MODE			Result
	Pin1	Pin2	Pin3	
1	100	100	100	Ref.
2	100	97	95	fail
3	100	97	95	fail
4	100	100	100	ok
5	100	100	100	ok

Table 7 Matrix Mode Comparison Results Overview

ST D4NK50ZD				
Sample	NORMAL MODE Ref – 1			Result
	Pin1	Pin2	Pin3	
1	100	100	100	Ref.
2	100	100	100	ok
3	100	100	100	ok
4	100	100	100	ok
5	100	100	100	ok

Table 8 Normal Mode Reference Pin 1 (Gate) Comparison Results Overview

ST D4NK50ZD				
Sample	NORMAL MODE Ref – 2			Result
	Pin1	Pin2	Pin3	
1	100	100	100	Ref.
2	100	100	85	fail
3	100	100	85	fail
4	100	100	100	ok
5	100	100	100	ok

Table 9 Normal Mode Reference Pin 2 (Drain) Comparison Results Overview

ST D4NK50ZD				
Sample	NORMAL MODE Ref – 3			Result
	Pin1	Pin2	Pin3	
1	100	100	100	Ref.
2	100	89	100	fail
3	100	89	100	fail
4	100	100	100	ok
5	100	100	100	ok

Table 10 Normal Mode Reference Pin 3 (Source) Comparison Results Overview

4 Conclusion

The presented results for two types of MOSFET power transistor are illustrating the V-I characteristic comparative analysis possibilities for detecting and monitoring differences caused by diverse reasons and influences. Such differences can be caused by natural technological process dispersion at the same producer, by parameters variations among different producers, by differences caused by latent or apparent damages, and frequently also differences caused by counterfeiting processes. We need authentic specimen characteristics, so called pin prints, prepared in advance for a reliable analysis and decisions based on it. The comparison criteria setting for analysis evaluation and the scan profile choice depends individually on the authentic component type analysis database to incorporate lot or inter-lot dispersion.

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