A 2.4-GHz LNA: Design, Simulation, and Comparison in 0.2-µm GaAs p-HEMT Process and 0.35-µm SiGe BiCMOS HBT Process

Farshad Eshghabadi[1], Fatemeh Banitorfian[1], Massoud Dousti[2], Norlaili Mohd Noh[1]
[1]School of Electrical and Electronic Engineering, Universiti Sains Malaysia, Nibong Tebal, Malaysia
[2]Department of Electrical Engineering, Azad University (IAU), Science and Research Branch, Tehran, Iran

***Abstract*— An LNA design and simulation using ED02AH Technology in 0.2-µm GaAs Pseudomorphic HEMT process and 0.35-µm HBT SiGe BiCMOS process are reported as a case of comparison. This work uses an identical circuit topology for both processes which is a 3-volt two stage cascode single-ended topology with a resistive shunt feedback. This LNA is developed for 2.4 GHz ISM band applications. This letter describes the differences of the achieved specifications such as gain, noise figure, impedance matching, third-order intercept point, linearity, and power consumption using these processes.**

***Keywords*— MMIC; GaAs; ED02AH; pHEMT; SiGe; BiCMOS; HBT; LNA; comparison**

I. INTRODUCTION

Monolithic Microwave integrated circuits (MMICs) for wireless applications market have gained much interest owing to their potential low cost and the prospect of system level integration. The needs for low voltage operating RF chips with lesser power consumption and higher performance/price ratio have led to increased interest and research of the front-end receiver. This huge increase in interest in microwave communications has resulted in an effort to provide components and complete systems on an integrated circuit.

The Viable IC technology for RF circuits continues to change. Performance, cost, level of integration, and prior successful experience are critical factors in the decisions made by the designers. At present, GaAs and SiGe BiCMOS technologies constitute the major section of the RF market [1].

The year 1985 heralded the era of "band-gap engineering," which is the technique of mixing different semiconductor materials to create transistors with specific solid-state properties. This eventually led to the development of a high-electron-mobility transistor (HEMT) low-noise amplifier (LNA) MMIC in 1988 and a heterojunction bipolar transistor (HBT) power amplifier in 1989 [2].

Other milestones along the MMIC development pathway include the appearance of the launch of Plessey's commercial 0.2-µm-gate-length pseudomorphic HEMT (pHEMT) process in 1996 [3]. Silicon germanium (SiGe) transistors are also in resurgence with frequency responses comparable to GaAs [4].

The most challenging building block in the front-end receiver is the low noise amplifier (LNA). The basic function of the LNA is to provide signal amplification while adding as little noise and distortion as possible to improve the overall noise figure and linearity of the front-end.

This paper focuses on a 2.4-GHz low noise amplifier (LNA) using two different MMIC technologies. An ED02AH pHEMT LNA design with gate length of 0.2-µm and a 0.35-µm HBT BiCMOS LNA design open up the possibility of comparison between these technologies. This LNA was designed in a single-ended two-stage cascode-topology with a resistive shunt feedback to be integrated in a small area.

The comparison is based on the key specifications such as gain, noise figure, impedance matching, third-order intercept point, linearity, and power consumption in an identical single-ended cascode-topology LNA using the mentioned processes.

Section 2 describes the principle of circuit topology used to dedicate the design. Section 3 presents the simulation results and the comparisons made in two processes. Finally, section 4 derives the conclusion.

II. CIRCUIT TOPOLOGY AND ANALYSIS

This LNA was designed in a single-ended two stage cascode topology with a resistive shunt feedback to be integrated in a small area (fig. 1). In addition to noise figure (NF) and gain, the stability of LNAs is also of concern. Stern Stability factor is defined as:

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{11}||S_{22}|} \quad (1)$$

where $\Delta=S_{11}S_{22}-S_{12}S_{21}$. If $K>1$ and $\Delta<1$ then the circuit is unconditionally stable. Equation (1) suggests that stability improves as S_{12} decreases, i.e., as the reverse isolation of the circuit increases.

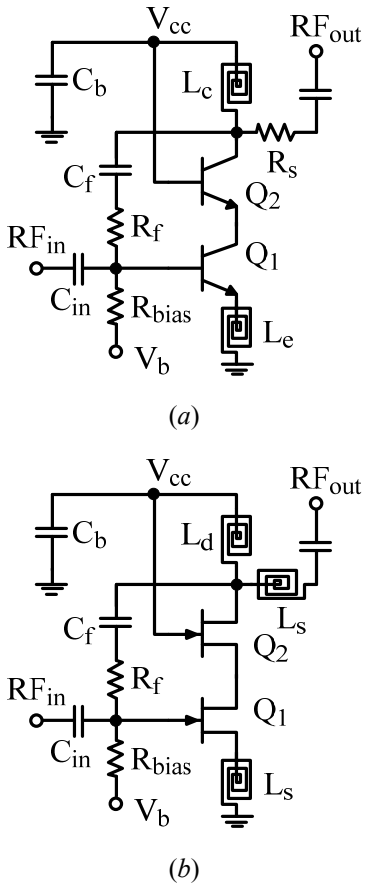


Fig. 1. Schematics of (*a*) SiGe HBT LNA (*b*) GaAs pHEMT LNA

Stray reactance coupled with Miller capacitance could act to produce a 180° phase shift from collector to base in the feedback signal. This 180° phase shift, when added to the 180° phase shift that is produced in the normal signal inversion from base-to-collector during amplification, could turn an amplifier into an oscillator very quickly [1].

Another problem associated with the internal feedback of the transistor is the fact that the collector circuitry is not truly isolated from the base circuitry. Thus, any change in the load resistance of the collector circuitry directly affects the input impedance of the transistor. This malady is especially important to consider when you are trying to perform an impedance match on both the input and the output of the transistor simultaneously [5].

The higher isolation is achieved by avoiding miller effect. This can be done using a cascode topology, but at the cost of a somewhat higher noise figure [1]. Also, the higher reverse isolation helps more attenuation of LO leakages from the mixer to the antenna which can cause severe interferences. The reverse isolation performance is very important for direct conversion receivers to keep the LO-to-RF leakage to a minimum.

The specification for a low-noise amplifier will generally require a low noise figure and a good input match, but the conjugate of S11 (required for a good match) is seldom the same as Γopt (required for low noise figure), so these cannot be achieved simultaneously [6]. The cascode topology has the inherent advantage of separating the output and input optimization criteria in the LNA circuit [7].

For a MOSFET, the source impedance that yields minimum noise factor is inductive in character and generally unrelated to the conditions that maximize power transfer. Furthermore, the input impedance of a MOSFET is inherently capacitive, so providing a good match to a 50-Ω source without degrading noise performance would appear to be difficult.

In this topology, using an input matching network is avoided as low-Q MMIC inductors add thermal noise of its resistance, and attenuates the signal. The combination of these two effects generally produces unacceptably high noise figures. [8]

The resistive feedback network continues to generate thermal noise of its own, but presents the FET LNA, an impedance that equals optimum impedance. Also, the broadband capability of this circuits is frequently enough of a compensating advantage that the shunt-series amplifier is found in many LNA applications, even though its noise figure is not the minimum possible. The feedback resistor R1 is chosen on the compromise among the parameters such as NF, gain, input impedance matching and linearity (see fig. 2).

Transmit time effects cause a resistive component of input impedance. Because of the finite velocity of charge, then, a real term is an unavoidable reality in charge-controlled devices such as FETs. In the context of LNAs, we actually seek to enhance this effect, for it can be used to create a resistive input impedance without the noise of real resistors.

A useful method is to employ inductive source degeneration. So control over the value of the real part of the impedance through the choice of inductance is available. Use of inductive degeneration at the emitter/source leads to a wideband match at the input. For a FET device model that includes only a transconductance and a gate-source and a gate-source capacitance, the input impedance has the following form:

$$Z_{in} = sL + \frac{1}{sC_{gs}} + \frac{g_m}{C_{gs}} L \approx sL + \frac{1}{sC_{gs}} + w_T L \qquad (2)$$

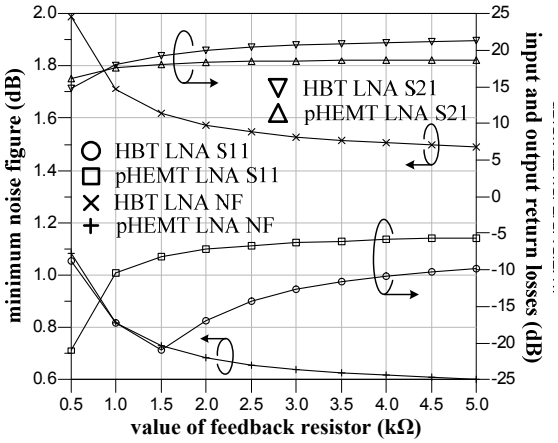


Fig. 2. LNAs' NF, gain and input impedance matching versus feedback resistor

Hence, the input impedance is that of a series RLC network with a resistive term that is directly proportional to the inductance value [8]. Here, Le value is approximately 0.2 nH for pHEMT LNA and 0.25 nH for HBT LNA which is realized by on-chip planar spiral inductors. However, the lossy low-Q inductors degrade the noise figure significantly. Hence, a compromise is prudent between the matching and noise figure.

R_{bias} is chosen large enough that its equivalent noise current is small enough to be ignored. Here, we selected a value of 5 KΩ. Off-chip DC blocking capacitors Cin and Cout are present to prevent upsetting the gate-to-source/base-to-emitter bias of transistors.

Their values are chosen large enough to have a negligible reactance at high frequency.

L2 plays the role of DC feed inductor which forms the output matching network with L3 in pHEMT LNA, and R2 in HBT LNA. The feedback resistor is chosen on a compromise among noise figure, gain and impedance matching.

In low-noise applications throughout the microwave and millimeter-wave frequency range, FETs are preferred to bipolar transistors [9]. This advantage is demonstrated by the comparison of the minimum noise figure for the two devices in GaAs pHEMT process and SiGe HBT process.

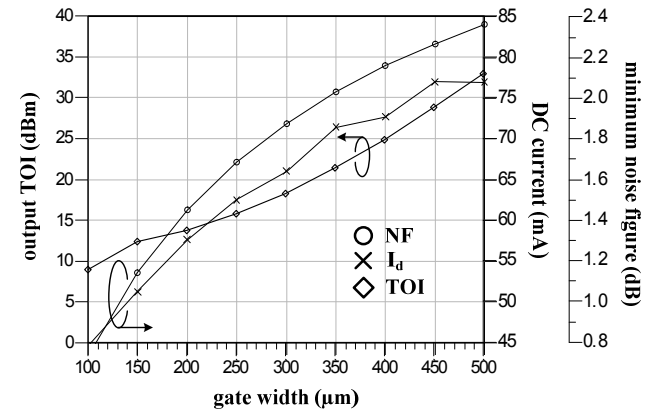
As can be seen in figure 3, in pHEMT LNA, the more the gate width of the transistors is increased, the higher an IP3 and ICP_{1dB} is achieved; but the DC current consumption and minimum noise figure increase significantly.

III. Simulation Results and Comparison

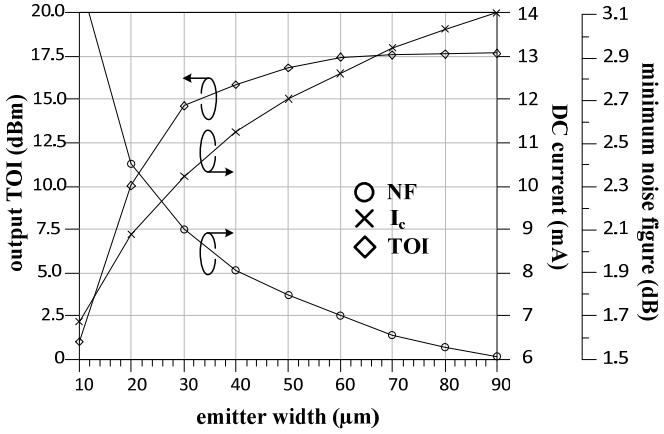
The LNA was designed and simulated in a 0.35-µm SiGe BiCMOS technology and a 0.2- µm GaAs pHEMT process using Agilent's Advanced Design System. Figure 4 shows the gain and noise figure of HBT LNA and pHEMT LNA. As it was expected, the NF of pHEMT LNA is lower than that of HBT LNA. Also, pHEMT design illustrates a relatively flatter gain than the HBT one. The gain and noise figure are given in table 1 at 2.45-GHz center frequency.

As shown in figure 5, the HBT LNA had better impedance matching than the pHEMT one at center frequency. But the pHEMT LNA provided a wide band match for both input and output matching. The linearity is provided in figure 6. Both designs have an identical linearity. That is to say that their input 1-dB gain compression point (ICP1dB) of both circuits are about -19dBm. But the input-referred third-order intercept point (IIP3) in the HBT LNA shows a better improvement than the one in pHEMT process. However, as input power increase, the pHEMT LNA shows a better IP3 point rather than the HBT LNA does.

HBT LNA has a 13-mA current consumption from a 3-volt DC power supply and pHEMT LNA consumes a 28-mA current from the similar supply. However, the HBT LNA transistors occupy less area than pHEMT FETs does. Area of transistor Q2 In both designs are half of that for Q1 to compromise between gains, and linearity, DC current consumption and noise figure.



(*a*)



(*b*)

Fig. 3. OIP3, DC current consumption, and NF versus gate width for (*a*) pHEMT LNA and (*b*) HBT LNA

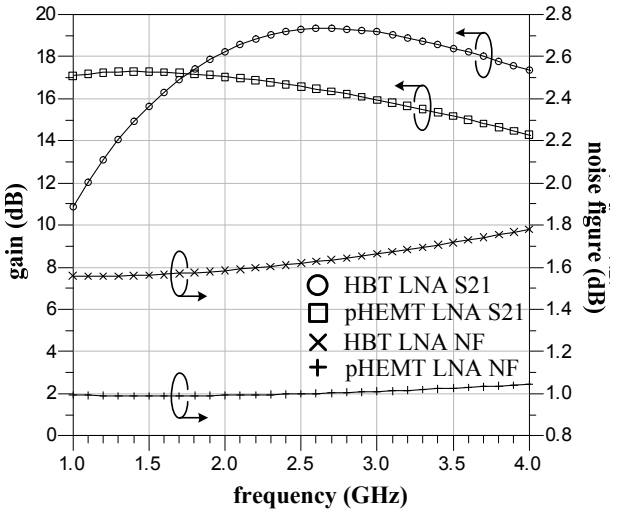


Fig. 4. LNA's simulated gain and noise figure

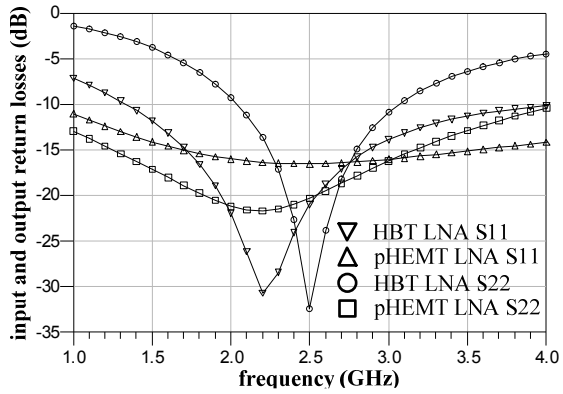
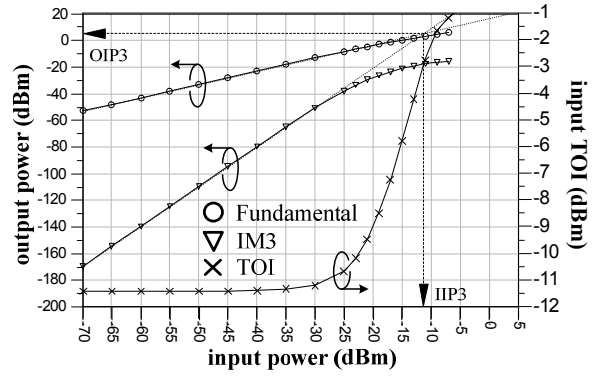
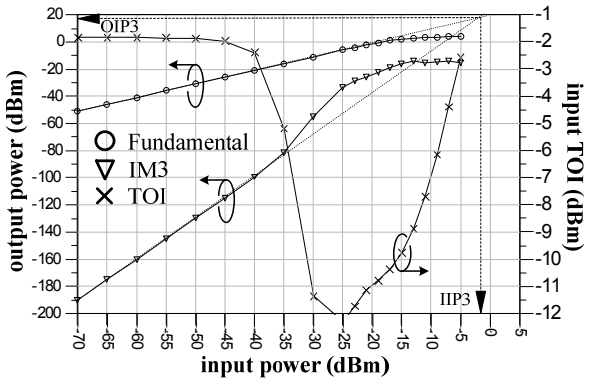


Fig. 5. LNA's simulated input and output return losses



(*a*)



(*b*)

Fig. 6. simulated linearity and input-referred intercept point for (*a*) HBT LNA and (*b*) pHEMT LNA

IV. CONCLUSION

A 2.4-GHz cascode LNA was designed and simulated in 0.2-µm GaAs Pseudomorphic HEMT process and 0.35-µm HBT SiGe BiCMOS process as a case of comparison between these two popular technologies. As illustrated, the pHEMT LNA consumes a DC current two times more than the HBT LNA to present the identical gain; but it gave the benefits of lower noise figure and wider matching band. Both LNAs presented an identical linearity, but the third-order intermodulation component grew sooner in pHEMT LNA than the one in HBT LNA. As a result, the SiGe HBT process shows a perfect narrow-band characteristics and GaAs pHEMT is a proper choice for broadband and low-noise component designs. The HBT LNA and pHEMT LNA parameters are summarized in the table 1 to simplify the comparison.

TABLE I. PERFORMANCE SUMMARY

Parameters	Technology	
	GaAs pHEMT LNA	***SiGe HBT LNA***
Gain (dB)	16.6	19.2
NF (dB)	1.00	1.62
S_{11} (dB)	< -16.5	< -20.3
S_{22} (dB)	< -20.6	< -22.6
S_{12} (dB)	-22.5	-25
ICP_{1dB} (dBm)	-19	-17
IIP3(dBm)	-11.4	-1.88
Current (mA)	28	14
Supply Voltage (V)	3	
Frequency (GHz)	2.4 ~ 2.5	
1-dB Gain BW (GHz)	> 3	> 1.5
Matching BW (GHZ) [S_{11} < -10]	> 6.8	> 2.6
Matching BW (GHZ) [S_{22} < -10]	> 3.4	> 1

REFERENCES

[1] Behzad Razavi, RF Microelectronics (Prentice Hall PTR, 1998).

[2] E. C. Niehenke, R. A. Pucel, I. J. Bahl, Microwave and Millimeter-Wave Integrated Circuits, IEEE Trans. Microwave Theory Tech., vol. 50, March 2002, pp. 846 – 857.

[3] H. Morkoc, Semiconductor with Strained InGaAs Layer, U.S. Patent No.4,827,320, May 2, 1989.

[4] T. Whitaker, IEDM Highlights Include SiGe HBTs Operating at 350 GHz, Compound Semiconductor Magazine, Institute of Physics Publishing Ltd., London, January 2003; available at http://www.compoundsemiconductor.net/articles/magazine/9/1/2/1

[5] Chris Bowick, RF Circuit Design (Newnes, 2007).

[6] Steve Marsh, Practical MMIC Design (Artech House, 2006).

[7] J. Laskar, B. Matinpour, S. Chakraborty, Modern Receiver Front-Ends (Wiley Interscience, 2004).

[8] Thomas H. Lee, The Design Of CMOS Radio-Frequency Integrated Circuits (Cambridge University Press, 1998).

[9] I. Bahl, P. Bhartia, Microwave Solid State Circuit Design (Wiley-Interscience, 2003).