Robust Controller for Limit Cycle Elimination of Two Input DC-DC Converter with Constant Power Load in Dc µGrid Applications

CH. NAYAK BHUKYA, B. AMARENDRA REDDY, ALLAM VENKATESH, T. R. JYOTHSNA
Department of Electrical Engineering,
Andhra University,
Vishakhapatnam, Andhra Pradesh,
INDIA

Abstract: - Direct Current (DC) µgrid is gaining more attention than Alternating Current (AC) µgrid, because of their simplicity in structure, which raises the utilization of dc power sources. However, for proper operation of dc µgrids, dc-dc power converters are required. MIMO converter systems are more commonly used in µgrid applications because of their vast benefits over SISO converter systems. The power converter operates under the previous state of tight control regulation which acts as constant power loads (CPL). Most loads in dc µgrid are CPLs, hence, one of the prime challenges in dc µgrid with CPLs is, an exhibition of negative incremental impedance (NII) which causes limit cycle behavior in the system. which tends to undesirable operations of the upstream converter and dc µgrid. The proposed double integral sliding mode controller (DISMC) control technique is designed to control and eliminate the dc µgrid bus voltage variations due to uncertainties of load and CPLs limit cycles. This control technique guarantees fast trainset response over system uncertainties and CPLs limit cycles. To validate the robustness of the proposed DISM controller, it is designed and simulated in a MAT lab environment.

Key-Words: - Dc µgrids, dc-dc two input power converter, CPLs, DISMC, INI, Limit cycle of CPLs, nonlinear loads.

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1 Introduction

As you can see from the title of the paper you must in the recent past, the adoption of dc µgrids is increasing in off-grid applications such as electric vehicles, data communication centers, electric aircraft, and shipboard, among others as depicted in Figure 1 over the alternating current (ac) µgrids. The Direct current (dc) µgrids are gaining more popularity. Its main benefits include resilience, ease of control, simplicity in integrating renewable energy sources, and the absence of reactive power management requirements (RES), etc., [1], [2]. The main problem with a dc grid is integrating renewable energy sources (RES), which can be made easier by using dc-dc power converters, [3]. The dc-dc power converters are either Single Input converters (SIC) or Multi Input converters (MIC). As compared to SICs, MICs have remarkable benefits like flexibility, reliability, and efficiency in operation. Owing to this, MICs are very commonly used in the integration operation of dc µgrid, [4].

Most loads linked to multi-input dc-dc power converters in dc grid applications are tightly regulated, forcing the loads to act as constant power loads (CPLs). The loads have negative increment impedance (NII) characteristics because of CPL's behavior. This will cause the output to exhibit limit cycle behavior or oscillatory response. As a result, the switching components will be under extreme stress, which will raise the temperature and cause problems with voltage instability in the converter system, [5]. As a result, many methods for dc µgrids with CPLs have been discussed to overcome the instability difficulties; among these methods, sliding mode controller (SMC) is widely employed in the dc µgrid application, [6].

SMC is also known as a variable structure control system since it is a nonlinear controller whose control law alternates between two distinct continuous structures (VSS). In comparison with other types of nonlinear controllers, SMC gained more attraction due to its robust capabilities and ensures the stability towards variations in the parameters and load uncertainties. Moreover, the design choice of SMC is easy and more flexible, [6], [7]. Because of its viable nature, SMC is the most adoptable base line controller in the field of integrated power converter dc µgrid with CPLs, [8]. But frequently, power converters' inconsistent operating frequency, chattering around the

switching surface, and steady state error prevent them from being used for real-time SMC adoption, [9]. Several adaptive strategies using SMCs help to alleviate the variable frequency issue. Higher-order sliding mode control solutions are implemented to mitigate the chattering tendency. Many scientists have attempted to reduce SSE by including an extra integral term in the SMC state variable; this method is known as an integral sliding mode controller (ISMC), [10], [11], [12].

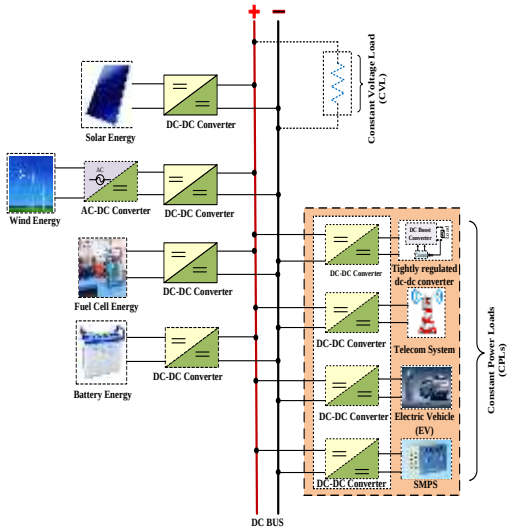


Fig. 1: Structure of dc µgrid with CPLs and CVL

The main drawback of ISMC is that, will not mitigate the SSE of the converter completely, [13]. The mitigation of SSE can be achieved by the increment in order of the ISM controller, i.e.by adding an additional second order integral term, which is called double integral sliding mode controller (DISMC), [14], [15], [16].

Hence, the main objective of this article is to present, the modeling and robustness analysis of a double integral sliding mode controller (DISMC) for two input dc-dc power converter with CPLs in dc µgrid applications.

The existing research is mainly focused on the regulation of SISO dc-dc converters with constant voltage loads. Here, the voltage across the load is maintained constant and the current variation is observed depending on changes in load resistance. Most of the literature discusses SISO converter regulation using conventional SMC. The main drawback of SMC is the chattering effect due to high frequency phenomena weakens the system stability. To overcome this drawback an integral sliding mode controller is implemented. The main limitation of an integral sliding mode controller is it will not eliminate the steady-state error. To overcome this double-integral sliding mode controller (DISM) is used. The novelty of this paper is the regulation of a two-input integrated converter system under constant power load. Constant power load requires voltage and current product constant at load, and it is a non-linear characteristic (hyperbola). To maintain constant power at the load terminals of a multi-input and multi-output dc-dc converter double integral sliding mode controller (DISMC) is considered which can be used for dc µgrid applications.

A detailed modeling, design, and analysis of two input dc-dc power converters with CPLs in dc µgrid applications with DISM controller are enumerated as follows: (i) section 2 problem formulation discussed (ii) section 3 problem to solution discussed (iv) section 4 brief description, modes of operation of two input dc-dc converter with CPL and its state space equations are discussed (v) section 5 Constant power load and its limit cycles impacts are discussed (vi) section 6 mathematical modeling of DISM controller are discussed (vii) section 7 Simulation results under different conditions are discussed.

The contribution of this article is as follows.

1. Modeling of two input dc-dc with CPL.
2. Performed impact analysis of CPL on the proposed system.
3. Elimination of Limit cycles with the help of DISM controller.
4. Validating the robustness of the proposed DISM controller under uncertainty situations.

2 Problem Formulation

When CPLs are under the umbrella of a dc µgrid through a two-input dc-dc converter, it is prone to characteristics of negative increment impedance (NII), owing to this there will be a limited cycle behavioral operation of the system. It will lead to an unstable situation, and switching devices will undergo stress and be prone to failure of the system, it is the major challenge in dc µgrid with CPL's operation.

3 Problem Solution

To mitigate the challenges associated with CPL's operation in dc µgrid applications, a robust controller is desirable. This work deals with a robust sliding mode controller. The main limitation of a single integral sliding mode controller is it will not eliminate the steady state error caused by the CPLs completely. To overcome this, an addition of another integral component to the single integral

sliding mode controller, which is known as a double-integral sliding mode controller (DISM). In this article, DISMC is used to alleviate the SSE and eliminate the limit cycles due to the CPL's operation. The proposed DISMC gives accurate results for the operation of two input dc-dc power converters with CPLs in the application of dc µgrid. The DISMC's design and guiding principles are covered in detail in the section that follows.

4 Two Input DC-DC Converter with CPL and CVL

The two input SEPIC converters with CPL and CVL are depicted in Figure 2. It consists of two switches, these switches are regulated independently, and each may undergo either of two positions (ON and OFF), and collectively behave as a control function of the converter circuit. The two switches are represented by S_1 and S_2. The switch positions are represented by "u_1 and u_2", which can take the discrete values of {0,1}, these switch positions are controlled by the duty cycle ratios ($d_1$andd_2). The duty cycle of the converter is controlled by pulse width modulation, and it is extremely important for power processing. The two switches (S_1, and S_2) can be regulated in three different ways based on switching periods of duty-cycles. These are: (i) d_1= d_2 (ii) $d_1 < d_2$ (iii) $d_1 > d_2$.

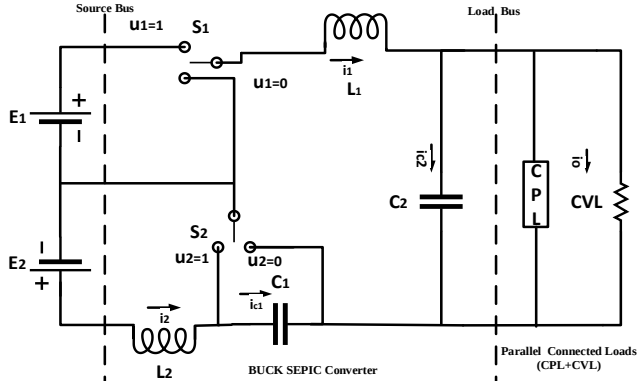


Fig. 2: Schematic diagram of two-input SEPIC converter with CPL and CVL

To accomplish the anticipated output of the two-input converter, it will undergo three modes of operation.The state-variable modeling of this converter circuit is obtained by applying Kirchhoff's current and voltage laws. Here, L&C elements without parasitic resistance are considered in writing the equations. The three modes of operation of the converter are given in the form of differential equations, state-space averaging has been proven to be an effective analysis method. which are written as follows:

Mode-1: (S_1=u_1=1, D_1=u_1=0; S_2=u_2=1, D_1=u_1=0)

$$\dot{i_1} = -\frac{V_{C_2}}{L_1} + \frac{V_{C_1}}{L_1} + \frac{1}{L_1}E_1 \quad (1)$$

$$\dot{i_2} = \frac{1}{L_2}E_2 \quad (2)$$

$$\dot{v}_{C_1} = \frac{i_1}{C_1} \quad (3)$$

$$\dot{v}_{C_2} = \frac{i_1}{C_2} - \frac{V_{C_2}}{C_2 R} - \frac{P}{C_2 V_{C_2}^2} \quad (4)$$

Mode-2: (S_1=u_1=1, D_1=u_1=0; S_2=u_2=0, D_1=u_1=1)

$$\dot{i_1} = -\frac{V_{C_2}}{L_1} + \frac{1}{L_1}E_1 \quad (5)$$

$$\dot{i_2} = -\frac{V_{C_1}}{L_2} + \frac{1}{L_2}E_2 \quad (6)$$

$$\dot{v}_{C_1} = \frac{i_2}{C_1} \quad (7)$$

$$\dot{v}_{C_2} = \frac{i_1}{C_2} - \frac{V_{C_2}}{C_2 R} - \frac{P}{C_2 {V_{C_2}}^2} \quad (8)$$

Mode-3: (S_1=u_1=0, D_1=u_1=1; S_2=u_2=0, D_1=u_1=1)

$$\dot{i_1} = -\frac{V_{C_2}}{L_1} \quad (9)$$

$$\dot{i_2} = -\frac{V_{C_1}}{L_2} + \frac{1}{L_2}E_2 \quad (10)$$

$$\dot{v}_{c_1} = \frac{i_2}{C_1} \quad (11)$$

$$\dot{v}_{c_2} = \frac{i_1}{C_2} - \frac{V_{C_2}}{C_2 R} - \frac{P}{C_2 V_{C_2}^2} \quad (12)$$

It is observed that the mathematical state space equations of the three modes of operation of the converter have inter relation to each other, which influences the output of the converter.

5 Constant Power Loads and its Limit Cycles

Constant power loads are electrical devices or systems that consume a constant amount of power regardless of variations in voltage or current. The basic CPL model depicted in Figure 3(a), according to Ohm's law like resistive loads, CPLs have a fixed resistance and consume constant power ($P=V^2/R$), [17], [18], [19].

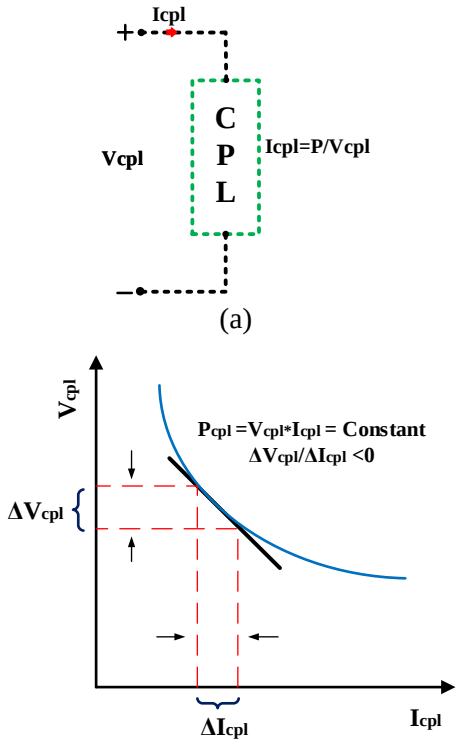


Fig. 3: **(**a) CPL model. (b) Constant power load V-I Characteristics

In Figure 3(a) I_{cpl} is current through the CPL terminal which is expressed in (13)

$$I_{cpl} = \frac{P}{V_{cpl}} \tag{13}$$

For a given operating point $I = \frac{P}{V}$, the CPL small signal model can be approximated by a straight-line tangent to the curve as illustrated in Figure 3(b), which is computed as:

$$I_{cpl} = -\frac{P}{V^2} v_{cpl} + \frac{2P}{V} \tag{14}$$

Equation (14) can be represented with a negative resistance ($R_{cpl} = -\frac{V^2}{P}$) and constant current source "I" given in (15)

$$I = \frac{2P}{V} \tag{15}$$

In general, Source-side converters and CPLs are often close to each other in power electronic converter systems, like EVs, electric shipboard, and the telecom sector. A tightly controlled Point of Load (POL) converter behaves like as CPL depicted in Figure 4(a) and is susceptible to instability, due to negative incremental impedance (NII) characteristics. This can cause limit cycle oscillations in the system, reduce system damping, voltage collapse, high stress on switching devices, and even system shutting down. The limited cycle oscillations which are the biggest challenge in dc µgrid with CPL's operation, [20], [21], [22], depicted in Figure 4(b).

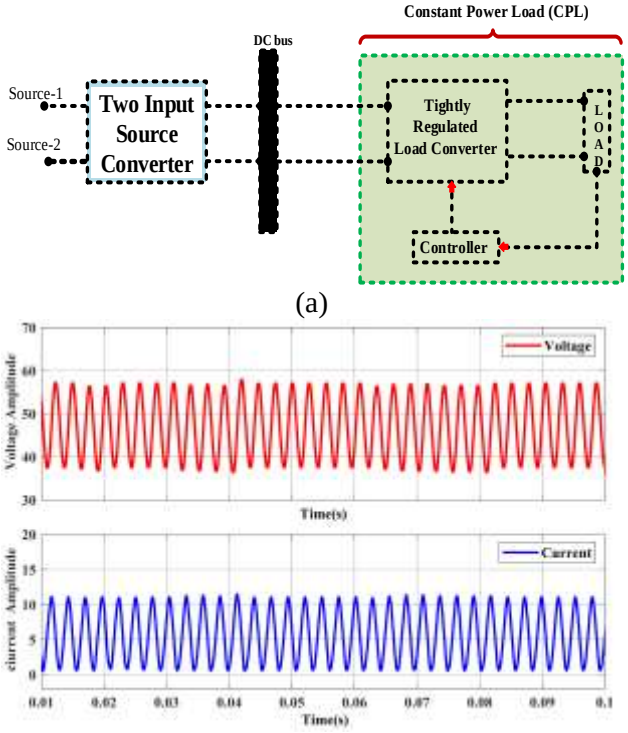


Fig. 4: (a)Point of Load converter acts as CPL (b) limit cycle oscillations of CPL

6 Double-Integral Sliding Surface Application to PWM-Based Indirect SM Controller

This section explores the application of DISM configuration to the PWM-based SM controller for buck SEPIC converter with CPLs of voltage and the current control, [23], [24], [25]. Furthermore there are several kinds of nonlinear controllers; SM Controllers are the most often used due to their enormous advantages when it comes to handling uncertainty and elimination of limit cycles caused by CPLs.

A practically single integral sliding mode controller (ISM) can eliminate steady state and transient error to some extent only i.e. it will not alleviate completely. To overcome these limitations an additional integral term is added to ISM, and it is called double integral sliding mode controller (DSIM) which is represented in equation (16).

$$s = \sum_{i=1}^{n-1} \alpha_i x_i + \alpha_n \int \sum_{i=1}^{n-1} x_i dt + \alpha_{n+1} \iint \sum_{i=1}^{n-1} x_i dtdt \quad (16)$$

The use of a double-integral term in a controller to improve steady-state accuracy while addressing stability concerns. The additional double-integral term i.e. $\int \left[\int x_i dt\right] dt$ for i=1, 2…n-1, is introduced to correct errors in the indirect integral computation of Integral Sliding Mode (ISM) controllers. By incorporating an integral closed-loop, the steady-state errors of the controlled state variables are indirectly reduced. This approach is referred to as the double-integral (indirect) sliding mode (DISM) controller, [21].

6.1 Control Law of DISMC for dc-dc Converter

Figure 5 describes the realization scheme of the PWM-based DISM controller for two input dc-dc converters with CPL. The form of control law used in the design of the DISM controller for a two-input dc-dc converter is given in (17) and the sliding surface is defined using equation (18).

$$\mu = \frac{1}{2}(1 + Sign(S)) \quad (17)$$

$$S = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4 \ldots. \quad (18)$$

where 'μ' represents the control logic for regulating the power switch, and α_1, α_2, α_3, and α_4 represent the desired sliding coefficients.

The procedure to derive double integral control law for voltage control and current control loops of integrated dc-dc converter is enumerated as follows.

(i) Define the switching surface equations for voltage and current loops of the integrated dc-dc converter.

$$S_v = \alpha_1 x_1 + \alpha_2 x_2 + \alpha_3 x_3 + \alpha_4 x_4 \quad (19)$$

$$S_i = \alpha_5 x_5 + \alpha_6 x_6 + \alpha_7 x_7 + \alpha_8 x_8 \quad (20)$$

In a two-input dc-dc converter, the state variables x_i, i = 1, 2, 8, are utilized to define the switching surfaces of the voltage and current loops. Current error and voltage error are described by the variables, x_1. And x_5. The variables, x_2. And x_6. describe the dynamics of the voltage error and the current error, respectively. The variables x_2 and x_6 describe the voltage and current error integrals, respectively. The double integrals of the errors of the voltage and current are described by x_4 and x_8, respectively. Equations (21) and (22) are used respectively, to provide a mathematical description of these.

$$\begin{cases} x_1 = V_{ref} - \beta_v V_0 \\ x_2 = \dot{x_1} \\ x_3 = \int x_1 dt \\ x_4 = \int (\int x_1 dt)\, dt \end{cases} \quad (21)$$

$$\begin{cases} x_5 = i_{ref} - \beta_i i_{L2} \\ x_6 = \dot{x_5} \\ x_7 = \int x_5 dt \\ x_8 = \int (\int x_5 dt)\, dt \end{cases} \quad (22)$$

where V_{ref}, i_{ref} signifies reference voltage and current, V_o, and i_{L2} are instantaneous voltage and current outputs of two-input integrated converter respectively. β_v, β_i denotes the feedback network ratios of voltage and current loops respectively.

(iii) By considering the first order differentiation of the equations (21) and (22) the dynamics of the stated state variables are derived (22). The dynamic model of this integrated dc-dc converter system is described using equations (23) and (24).

$$\begin{cases} \dot{x_1} = -\beta_v \frac{dV_0}{dt} = -\frac{\beta_v}{C_2} i_{c2} \\ \dot{x_2} = -\frac{\beta_v}{C_2} \frac{di_{c2}}{dt} \\ \dot{x_3} = \frac{d}{dt}\left(\int x_1 dt\right) = V_{ref} - \beta_v V_0 \\ \dot{x_4} = \frac{d}{dt} \int \left(\int x_1 dt\right) dt = \int \left(V_{ref} - \beta_v V_0\right) dt \end{cases} \quad (23)$$

$$\begin{cases} \dot{x_5} = \frac{\beta_i}{L_2}(1 - u_2) V_{c1} - \frac{\beta_i}{L_2} V_{g2} \\ \dot{x_6} = \frac{\beta_i}{L_2 C_2}(1 - u_2) i_{c1} \\ \dot{x_7} = \frac{d}{dt}\left(\int x_5 dt\right) = i_{ref} - \beta_i i_{L2} \\ \dot{x_8} = \frac{d}{dt} \int \left(\int x_1 dt\right) dt = \int \left(i_{ref} - \beta_i i_{L2}\right) dt \end{cases} \quad (24)$$

(iv) Determine the linear part of sliding mode control law and it is denoted by "U_{eq}" i.e., equivalent control. The equivalent control signal of voltage and current loops of the integrated converter of DISM are denoted by u_{1v} and u_{2i}. To obtain the equivalent control laws for voltage and current loops , consider the derivative of switching surface equations defined using (19) and (20), and equate these to zero. As the derivative of switching surface equations are functions of the equivalent control signals and equated to zero results u_{1v} and u_{2i}. These are given in equations (25) and (26).

$$u_{1v} = \frac{i_{c2}}{\beta_v V_{g1}}\left(-\frac{\alpha_1}{\alpha_2}(\beta_v L_1) + \frac{L_1}{R_L C_2}\right) + \frac{\beta_v V_{c1} - \beta_v V_{g2}}{\beta_v V_{g1}} + \frac{\alpha_3}{\alpha_2} L_1 C_2 \left(\frac{V_{ref} - \beta_v V_0}{\beta_v V_{g1}}\right) + \frac{\alpha_4}{\alpha_2} L_1 C_2 \frac{(\int (V_{ref} - \beta_v V_0) dt)}{\beta_v V_{g1}} \quad (25)$$

$$u_{2i} = -\frac{\alpha_5}{kL_2}(\beta_i E_2 - \beta_i V_{C_1}) + \frac{\alpha_6}{kL_2 C_1}\beta_i i_{c1} + \frac{\alpha_7}{k}(i_{ref} - \beta_i i_2) + \frac{\alpha_8}{k}(\int (i_{ref} - \beta_i i_2)\, dt) \quad (26)$$

Where $k = \frac{\alpha_5}{L_2}\beta_i V_{c1} + \frac{\alpha_6}{L_2 C_1}\beta_i i_{c1}$

(v) (v) PWM is generated by comparing ramp signal with V_C. Use an indirect SM control approach to develop a set of equations for the control signal (V_C) of voltage loop and a ramp signal (V_{ramp}) with peak magnitude, [26], [27]. V_C is defined as in (27). Similarly, i_C is defined as in equation (28).

$$V_C = -K_{1v} i_2 + K_{2v}(V_{ref} - \beta_v v_0) + K_{3v} \int (V_{ref} - \beta_i v_0) dt + \beta_v v_0 \quad (27)$$

$$i_C = K_{1i}(i_{ref} - \beta_i i_2) + K_2 \int (i_{ref} - \beta_i i_2) dt + K_1 [K(i_{ref} - \beta_i i_2) - i_2] + K_2 \int [(i_{ref} - \beta_i i_2) - i_2] dt - K_3 i_{C1} + G_s(v_o - E_{1)} \quad (28)$$

(vi) Compare the equation (27),(28) with equations (25),(26) and coefficients are defined as follows.

$$u_{1v} = i_{c2}\left(\frac{1}{\beta_v E_1}\right) K_{1v} + \frac{V_{C_2}}{E_1}\left(\frac{1}{\beta_v E_1}\right) K_{2v}(V_{ref} - \beta_v V_0) + \left(\frac{1}{\beta_v E_1}\right) K_{3v}[(\int (V_{ref} - \beta_v V_0)\, dt)] \quad (29)$$

$$u_{2i} = -k_{1i}(\beta_i E_2 - \beta_i V_{c1}) + k_{2i}\beta_i i_{c1} + k_{3i}(i_{ref} - \beta_i i_2) + k_{4i}(\int (i_{ref} - \beta_i i_2)\, dt) \quad (30)$$

where 'u_{1v}' and 'u_{2i}' are continuous and bounded by 0 and 1.

$$k_{1v} = -\beta_v L_1\left(\frac{\alpha_1}{\alpha_2}\right) + \frac{L_1}{R_L C_2}, k_{2v} = \frac{\alpha_3}{\alpha_2} L_1 C_2, k_{3v} = \frac{\alpha_4}{\alpha_2} L_1 C_2 ,k_{1i} = \frac{\alpha_5}{kL_2}, k_{2i} = \frac{\alpha_6}{kL_2 C_1}, k_{3i} = \frac{\alpha_7}{k}, k_{4i} = \frac{\alpha_8}{k}.$$

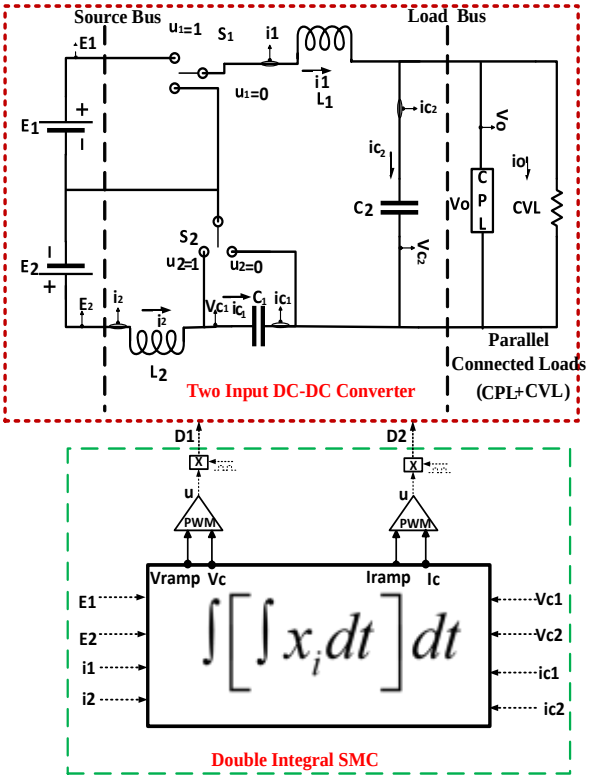


Fig. 5: realization scheme of the PWM-based DISM controller for two input dc-dc converter with CPL

7 Simulation Results and Discussion

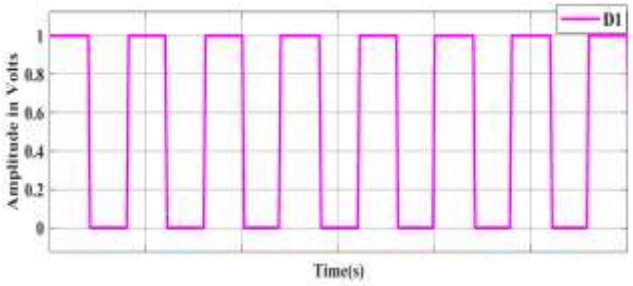
The theoretical considerations are verified to confirm the performance of the proposed Double Integral Sliding Mode Controller with CVL and CPL, it is executed with the structure of Figure 5 in MATLAB environment. Two-input dc-dc converter with CVL and CPL simulations are executed under different situations. The system parameters are chosen as illustrated in Table 1.

Table. 1. System and Control Parameters

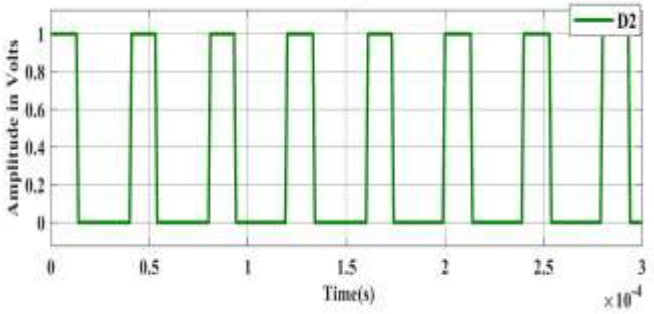
Description	Value
Input voltages (E_1, E_2)	60V,36V
Output voltage (V_o)	48V
Switched frequency (f_{BW})	25kHz
Inductances (L_1, L_2)	650µH,600µH
Capacitances (C_1, C_2)	20µf,220µf
feedback network ratio of voltage (β_v)	0.1250
feedback network ratio of current (β_i)	0.4
Voltage Coefficients (K_{1v}, K_{2v}, K_{3v})	-2.255,11.231,600
Current Coefficients (K_{1i}, K_{2i}, K_{3i})	-3.04,13.24,854

Figure 6, Figure 7, Figure 8, Figure 9, Figure 10, Figure 11 and Figure 12 show the unstable,

stable operation of the converter under the impact of CPL, and uncertainties in source, load is modeled. The converter operates with duty cycles of $d_1>d_2$ as depicted in Figure 6(a) and Figure 6(b). Performance results were analyzed in three different situations. (i) Consider the converter without DISMC and with CPL, the converter exhibits limit cycle behavior. The converter state-variables V_{c2} , I_{L1} are depicted in Figure 7, and V_{c1}, I_{L2} are depicted in Figure 8. (ii) Consider the converter with DISMC and with CPL, and the closed-loop converter does not exhibit the limit cycles the converter state-variables V_{c2} , I_{L1} are depicted in Figure 10, and V_{c1}, I_{L2} are depicted in Figure 11. Here, the DISM controller eliminated limit cycles caused by the CPL. (iii) Consider the converter with DISMC and with CPL under source and load perturbations depicted in Figure 12. The closed-loop converter rapidly reaches its reference value without any limit cycles. The results of state variables are depicted in Figure 13 and Figure 14. Under these situations the robustness of the DISM controller reflects provides constant power to CPL without limited cycles and disturbances.

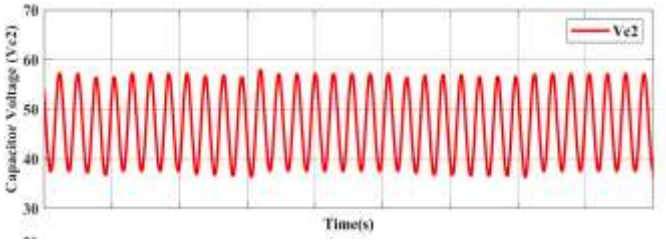


(a)

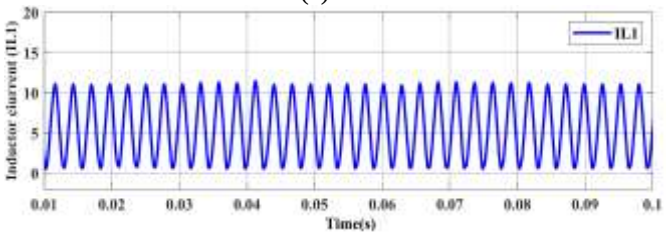


(b)

Fig. 6: Simulated Duty Cycles of the proposed system: (a) Control input of Switch, S_1; (b) Control input of Switch, S_2

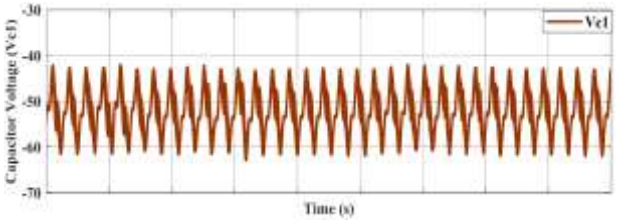


(a)

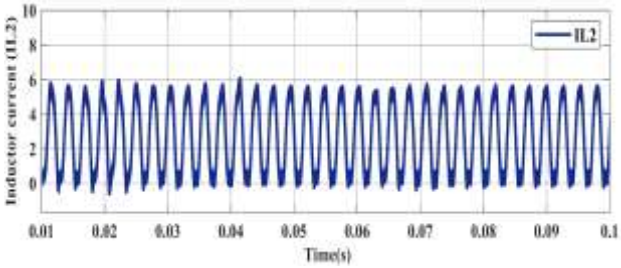


(b)

Fig. 7: Simulated response of proposed system without DISMC: (a) Capacitor Voltage, Vc_2; (b) Inductor Current, I_{L1}

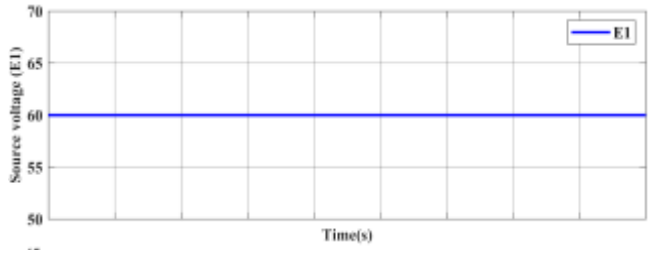


(a)

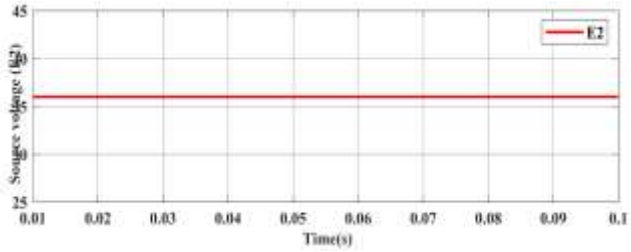


(b)

Fig. 8: Simulated response of proposed system without DISMC: (a) Capacitor Voltage, Vc_1; (b) Inductor Current, I_{L2}

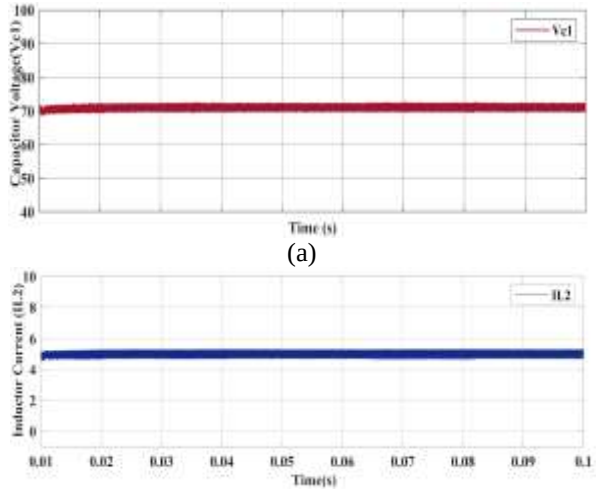


(a)



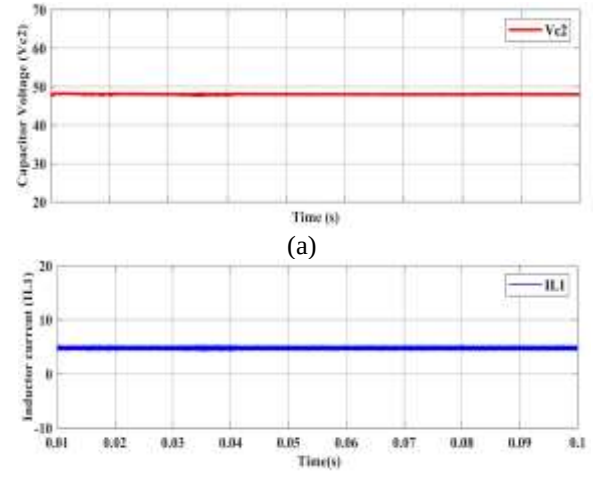
(b)

Fig. 9: Simulated response of the proposed system with DISMC: (a) Input Source Voltage, E_1; (b) Input Source Voltage, E_2



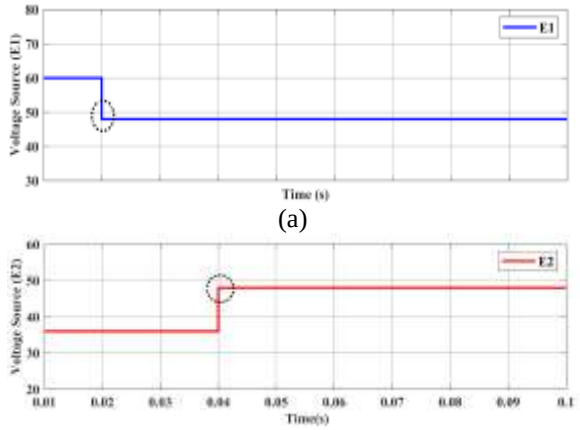
(b)

Fig. 10: Simulated response of the proposed system with DISMC: (a) Capacitor Voltage, Vc_1; (b) Inductor Current, I_{L2}



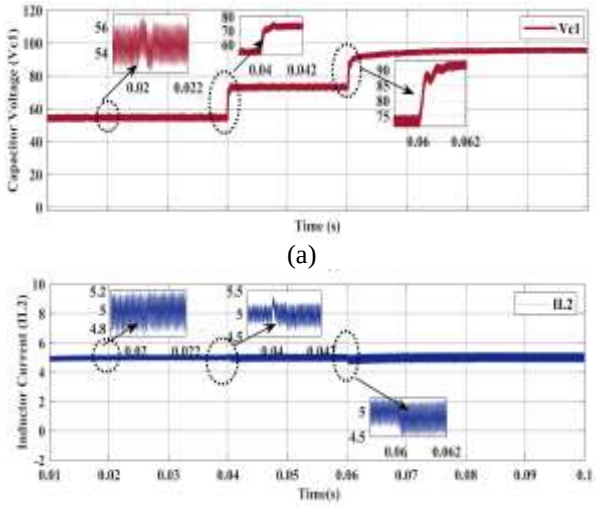
(b)

Fig. 11: Simulated response of the proposed system with DISMC: (a) Capacitor Voltage, Vc_2; (b) Inductor Current, I_{L1}



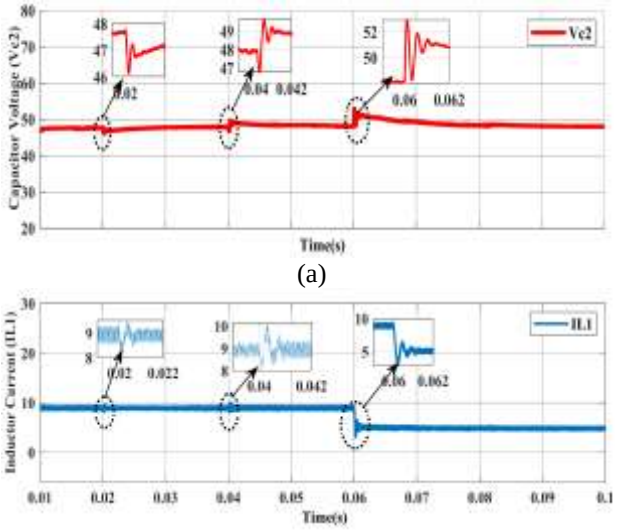
(b)

Fig. 12: Simulated uncertainties in source and load response of the proposed system with DISMC:(a) uncertainty in Input Source Voltage, E_1;(b) uncertainty in Input Source Voltage, E_2



(b)

Fig. 13: Simulated uncertainties in source and load response of the proposed system with DISMC:(a) Capacitor Voltage, Vc_1; (b) Inductor Current, I_{L2}



(b)

Fig. 14: Simulated uncertainties in source and load response of the proposed system with DISMC:(a) Capacitor Voltage, Vc_2; (b) Inductor Current, I_{L1}

8 Conclusion

This work presents the design aspects of the DISM controller for a two-input dc-dc converter with CVL and CPL. DISM controller eliminates limit cycle behaviour caused by the constant power loads in dc μgrid applications specifically in electric shipboard, electric vehicles etc., The simulation results prove that the use of a double integral sliding mode controller offers robustness, fast response, reduced steady-state error, and disturbance rejection, and handles the negative increment impedance (NII) effect sensibly well. It is an effective control solution for applications where precise regulation of output voltage is required despite source and load uncertainties. Results gave a close treaty between theoretical study and simulation. Future research will examine the potentiality of DISM controllers for fault tolerant converters introduced in dc microgrid to achieve extreme reliable operation and quick steady state response.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

- Ch Nayak Bhkuya, B.Amarendra Reddy, and A.Venkatesh have carried out the mathematical modelling and prescribed analysis of this article.
- Ch Nayak Bhukya has written this article and has performed simulations and taken the results for this article.
- B.Amarendra Reddy, and T.R.Jyothsna have supervised this article.

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The authors have no conflicts of interest to declare.