Research on a Two-level Single-phase Active Power Factor Corrector Using Gray Prediction and Repetitive Control

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Abstract: The traditional single-phase active power factor correction (APFC) has been widely used. There are two voltage levels between the output terminal of boost inductor and the negative rail of DC link, which correspond to turn-on time and turn-off time of IGBTs. IGBT is the normally used power device. One level is near zero, the other is approximately the positive Output DC voltage. Just due to this, no matter which control strategy is used, zero-crossing distortion of the mains current occurs theoretically that is inevitable. In the paper a novel two-level APFC topology is presented. It can completely eliminate the zero-crossing distortion in essence, at the time the current control strategies can be used. The two voltage levels between the output terminal of boost inductor and the negative rail of DC link are the positive Output DC voltage when IGBT is in on state and the negative Output DC voltage when IGBT is in off state, respectively. With regard to single-phase APFC's control strategies, in order to generate the primitive driving pulse used for the next switching cycle, it is common that the data used in the current switching cycle is those measured in the previous switching cycle and the current switching cycle. It is inevitable that the method causes lagging control effects. Considering the function of gray prediction, the modulation of GM(1,1) is employed in order to achieve precise control. Thus the electrical quantities required in the next switching cycle can be accurately predicted, including the input AC voltage, the output DC voltage, the boost inductor current, the boost inductor current error and the output DC voltage error. It is also true that the single-phase APFC is powered by sinusoidal voltage, and the expected are DC voltage and sinusoidal current in phase with input voltage. It is inevitable that the method causes steady state errors, when using the traditional double loop control strategy, consisting of the voltage outer loop and the current inner loop. Therefore, the repetitive control strategy is utilized at the same time. The steady state errors can be eliminated and the dynamic characteristics can be improved by both adding voltage error in current switching cycle to the predicted current error and adding voltage error in current switching cycle to the predicted output voltage error. After analysis of the operation principle of the novel two-level APFC, a comprehensive control strategy based on gray prediction and repetitive control is designed. Then the comprehensive control strategy based two-level APFC is simulated and analyzed by means of MATLAB/SIMULINK and implemented. The obtained results are satisfactory and prove comprehensive control strategy.

Key words: Power factor corrector, Two voltage-level, Zero-crossing distortion, Gray predictive control, Repetitive control, comprehensive control

1 Introduction

Single-phase active power factor corrector (APFC) can eliminate harmonic currents and gain unitary power factor at mains side, which can make electrical equipment fed by single-phase power supply meet the harmonic current standards[1~2]. Till now, it has been applied extensively in the fields of the inverter-powered household appliances and communication power supplies. Great progress has been made to single-phase APFC in terms of circuit topology, control strategy, modulation algorithm, analysis approach and implementation technology.

Specifically speaking, a lot of different power circuits has arisen, inclusive of bridged APFC and bridgeless APFC[3], single-channel APFC and interleaved APFC[4], and three-level APFC[5~7], and so on.

There also are many distinct control strategies, including the traditional double closed-loop control, one-cycle control, follower control and many other classical control and intelligent control strategies.

In addition, there are a variety of modulation algorithms, including pulse width modulation (PWM), pulse phase modulation (PPM) and pulse frequency modulation (PFM), the latter two can be used as single random modulation, double-random modulation.

In practice, there are various practical technologies, including planar inductor, inductor current synthesis and current sharing.

For the traditional single-phase APFC, there are totally two voltage levels between the output terminal of boost inductor and the negative rail of DC link, one level is near zero, the other is approximately the positive Output DC voltage. The two voltage levels correspond to turn-on time and turn-off time of IGBTs respectively. Given this, when any control strategy is used, zero-crossing distortion of the input current at mains side comes into being in theory.

In the paper a novel two-level APFC topology is presented. It can completely eliminate the zero-crossing distortion in essence, at the time the current control strategies can be used. The two voltage levels between the output terminal of boost inductor and the negative rail of DC link are the positive Output DC voltage when IGBT is in on state and the negative Output DC voltage when IGBT is in off state, respectively. Within the on time of IGBT, the boost inductor stores energy in the form of magnetic field. During the off time of IGBT, it releases energy into the electrolysis capacitor in the form of chemical energy. The form of boost inductor current looks sinusoidal with consequent ripple current. As a consequence, the form of input current at mains side is almost pure sinusoidal waveform after filtered by filter capacitor placed between the two AC lines. Considering the voltage drop of the rectifier bridge, even though the duty ratio is large enough in the neighborhood of zero crossing of the input sinusoidal voltage, it is hard to form inductor current. The worst case will happen when a greater inductance is selected. It causes zero crossing distortion and deteriorates the hoped correction effect. In order to eliminate the zero crossing distortion of the input current, a novel two-level APFC topology is presented, simulated and experimented in a consecutive way. It can completely eliminate the zero-crossing distortion naturally, featuring the positive Output DC voltage when IGBT is on and the negative Output DC voltage when IGBT is off. At the same time, all the current control strategies can be used only with a little modification.

It is well known that control strategy used efficiently or not decides the whole controlling performance. Single-phase APFC is fed by the sinusoidal voltage, and even more the expected are DC voltage and sinusoidal current in phase with input voltage. The direct results state that the method causes steady state errors inevitably, when the traditional plain double-loop control strategy is used, which consists of the voltage outer loop and the current inner loop. Therefore, the repetitive control strategy is utilized. The steady state errors can be eliminated and the dynamic characteristics can be improved by both adding voltage error in current switching cycle to the predicted current error and adding voltage error in current switching cycle to the predicted output voltage error.

The other fact can't be neglected that the single-phase APFC is powered by sinusoidal voltage, and the expected are DC voltage and sinusoidal current in phase with input voltage. The method causes steady state errors certainly, when using the traditional double loop control strategy, that is, voltage outer loop and the current inner loop. Therefore, the repetitive control strategy is utilized [14~20], which can bring about the eliminated steady state errors and the improved dynamic characteristics through both adding voltage error in current switching cycle to the predicted current error and adding voltage error in current switching cycle to the predicted output voltage error.

Considering the above said, a

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comprehensive control strategy based on gray prediction and repetitive control is designed for the novel two-level APFC in order to reduce zero crossing distortion of the mains current, to implement real time control and to eliminate steady state errors for the whole system. Then the novel two-level APFC using the comprehensive control strategy is simulated by means of MATLAB/SIMULINK and experimented. The gained results are satisfactory and prove comprehensive control strategy.

2. Two-level APFC

2.1 Circuit topology

The circuit topology of two-level APFC is shown in Fig.1, which is powered by the single-phase AC power supply and produces DC voltage at output and sinusoidal current at input side. It consists of a diode rectifier B1 (D1~D4), a boost inductors (L1), an inverter bridge by power devices (S1~S4), an electrolysis capacitor (E1), a filtering capacitor (C1) and stabilizing resistor (R1). A stable DC voltage is desired at output side.

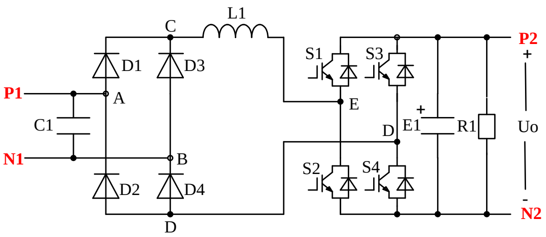

Fig.1 Topology of the novel single-phase APFC

Power devices S2 and S3 are defined as the first group, and S1 and S4 are defined as the second group, and the switching states of the two groups of switches are complementary. Assuming the circuit stays in the steady state and the Output DC voltage keeps unchanged at $+U_{dc}$.

When only the first group of power devices is turned on in one switching cycle, the voltage of the output end of inductor with respect to point D is close to $+U_{dc}$. The energy stored in the boost inductor is transferred to the electrolysis capacitor partially or completely according to the used conduction mode, DCM or CCM. The current of inductor drops. The electrolysis capacitor releases energy to the load.

When only the second group of power devices is turned on for the rest time in the same switching cycle, the voltage of the output end of inductor with respect to point D is close to $-U_{dc}$. The boost inductor stores energy coming from mains side. The current of inductor rises. The electrolysis capacitor releases energy to the load.

It is certain that the proposed novel two-level APFC can holds all the conversion function by the control of the duty cycle of two groups of power devices. In fact, the single-phase or three-phase voltage source PWM rectifier has the same conversion principle, where the voltage between two midpoints of the two or three arms is either positive or negative DC voltage one after another in any switching cycle.

As shown in Fig.1, considering the role of S1 and S4 on the APFC, they can be reduced and replaced by fast reverse recovery diode FRD1 and FRD2 respectively. The resultant topology is shown in Fig.2.

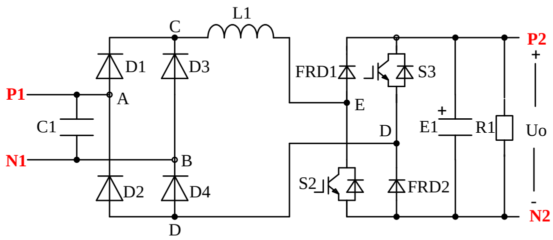

Fig.2 Topology of the reduced novel single-phase APFC

2.2 Voltage ratio

Take Fig.2 for example, the novel APFC is connected to the single-phase AC voltage source. u_{in} denotes its instantaneous value, and U_o denotes the average output DC voltage. When the second group of power devices S2 and S3 are turned on and their conduction voltage drops are neglected, the voltage between points E and D is $-U_o$. According to Fig.3, being in continuous conduction mode (CCM), the inductor loop equation can be written as

$$\left|u_{in}\right| = \mathrm{L}_1 \frac{\mathrm{d}i_{L1}}{\mathrm{dt}} \text{-} u_0 \tag{1}$$

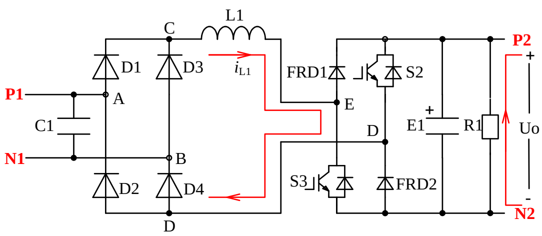

Fig.3 Inductor current path of single phase APFC when power devices S2 and S3 are turned on

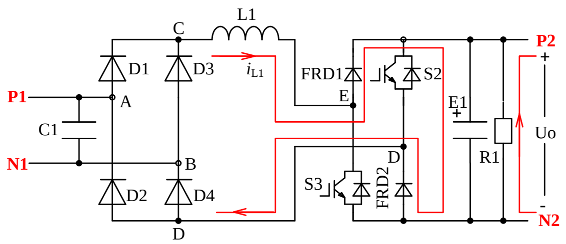

Fig.4 Inductor current path of single phase APFC when power devices S2 and S3 are turned off

When power devices S2 and S3 are turned off and their conduction voltage drops are neglected, the voltage between points E and D is $+U_o$. According to Fig.4, being in continuous conduction mode (CCM), the inductor loop equation can be written as

$$|u_{in}|+L_1\frac{di_{L1}}{dt}=u_0 \quad (2)$$

Therefore, the voltage transfer ratio of the APFC can be deduced by the volt-second equilibrium equation of inductor L1. Assuming the duty cycle of S1 and S2 is d, according to Fig.3 and Fig.4 and equation 1 and 2, the volt-second equilibrium equation of inductor L1 is written as

$$(|u_{in}|+u_o)dT_S=(u_o-|u_{in}|)(1\text{-}d)T_S \quad (3)$$

Then,

$$\frac{u_0}{|u_{in}|}=\frac{1}{1\text{-}2d}\ ,\quad (0\le d<0.5) \quad (4)$$

Obviously, compared to the traditional APFC, the maximum duty cycle of power device for the novel two-level APFC is 0.5 mathematically. Of course, the maximum available duty cycle of power device is less than 0.5 practically.

3 Control Strategy

3.1 Gray prediction control

Prediction can be used to estimate and predetermine the trends and results of an event happening in the future. Among all the existing prediction methods, the gray prediction method is dedicated to exponentially varying system. By employing the historically measured data, gray prediction can accurately predict the electrical quantities, which are needed as the primitive information in the next switching cycle, inclusive of the output DC voltage, the boost inductor current and the input AC voltage. that can bring about more precise regulation.

Take the boost inductor current for example to describe the prediction principle and process of gray prediction.

Assuming $x^{(0)}(k)=I_L(k)$ is the original data sequence,

$$x^{(0)}=\{x^{(0)}(1),x^{(0)}(2),\cdots,x^{(0)}(n)\} \quad (5)$$

where n denotes the number of sampled data.

Since the sampled data are either positive or negative, the original data should be processed to be positive by the following expression,

$$x_p^{(0)}(k)=M+N\cdot x^{(0)}(k) \quad (6)$$

where M, N>0 ,and $M>|N\cdot x^{(0)}(k)|$,k=1,2,...,n.

Then,

$$x_p^{(0)}=\{x_p^{(0)}(1),x_p^{(0)}(2),\cdots x_p^{(0)}(n)\} \quad (7)$$

According to gray prediction, after processed to be positive, $x_p^{(0)}$ can be accumulated,

$$x_p^{(1)}(k)=\sum_{i=1}^{k}x_p^{(0)}(i) \quad (8)$$

where k=1, 2, ..., n.

Then,

$$x_p^{(1)}=\{x_p^{(1)}(1),x_p^{(1)}(2),\cdots,x_p^{(1)}(n)\} \quad (9)$$

Therefore, the differential equations of GM(1,1) grey form of $x^{(0)}(k)$ is,

$$\frac{dx_p^{(1)}}{dt}+ax_p^{(1)}=u \quad (10)$$

where a and u are unknown parameters , which can be expressed as below,

$$\begin{bmatrix}a\\u\end{bmatrix}=(B^TB)^{-1}B^TY_N \quad (11)$$

where， $$B=\begin{bmatrix} -\frac{1}{2}(x_p^{(1)}(1)+x_p^{(1)}(2)) & 1 \\ -\frac{1}{2}(x_p^{(1)}(2)+x_p^{(1)}(3)) & 1 \\ \cdots & \cdots \\ -\frac{1}{2}(x_p^{(1)}(n-1)+x_p^{(1)}(n)) & 1 \end{bmatrix} \quad (12)$$

$$Y_N=\begin{bmatrix} x^{(0)}(2) \\ x^{(0)}(3) \\ \cdots \\ x^{(0)}(n) \end{bmatrix} \quad (13)$$

Substitute parameters a and u into Equation 10, the discrete solution is gained as below,

$$\overline{x}_p^{(1)}(k+1)=\left[x_p^{(1)}(1)-\frac{u}{a}\right]e^{-ak}+\frac{u}{a} \quad (14)$$

Restore them to the positive column,

$$\begin{aligned}\overline{x}_p^{(0)}(k+1)&=\overline{x}_p^{(1)}(k+1)-\overline{x}_p^{(1)}(k)\\&=(1-e^{a})\left[x_p^{(1)}(1)-\frac{u}{a}\right]e^{-ak}\end{aligned} \quad (15)$$

And then restore them to the original data column,

$$\overline{x}^{(0)}(k+1)=\frac{1}{N}\left\{(1-e^{a})\left[x^{(0)}(1)-\frac{u}{a}\right]e^{-ak}-M\right\} \quad (16)$$

Therefore, on the basis of the sampled data sequence, the boost inductor current in next switching cycle can be predicted. Likewise, the output DC voltage and the input AC voltage in a switching cycle can also be predicted.

3.2 Repetitive control

Repetitive control was presented in 1981 by Inoue, a Japanese scholar, which can acquire high-precision control over the repetitive track for the servo system.

Repetitive control is derived from the internal model principle. The reason for the improved tracking accuracy for a system under control is that the input signal for the controlled object includes not only the error signal but also the control error at the same time of the prior period. Hence, the periodic disturbance for the output signal can be suppressed dramatically.

In other words, the grid voltage prediction error and model parameter errors make the mains current and the output DC voltage not properly track the expected values. Fortunately, the interfering factors recur with the same period of mains voltage. Therefore the repetitive control method can be used to weaken the interfering impact.

The basic block diagram of repetitive control is shown in Fig.5.

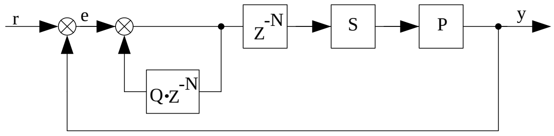

Fig. 5 Block diagram of repetitive control system

As shown in Fig.5, r is the reference signal, y is the output signal, e is the error signal, z is the cycle delay, S is compensation of repetitive control loop, P is the controlled plant. Q·z-N the internal model of repetitive controller, and it is used to achieve the error memory function. Q is the key parameter to design the controller, whose value is closely relevant to the system steady-state accuracy and error convergence rate, and is.

Graphical representation of the stable condition of the repetitive control is shown in Fig.6. The stability of control system must satisfy the constraints as below,

$$\|Q-SP\|_{\infty}<1 \quad (17)$$

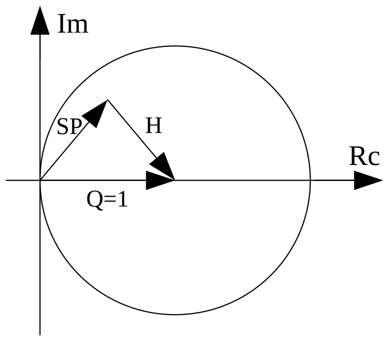

Fig.6 Graphical representation of repetitive control system stability

When Q=SP, all the poles of system are at the origin, the speed of convergence is the fastest. Assuming Q=1, the error can be decayed to 0 by repetitive controller. Theoretically, the system behaves without steady state error and SP=1. When SP is characteristic of zero gain and zero phase-shift, the system acquires the best performance. So the ideal compensation should be the reciprocal of the control object.

However, normally it is difficult for the controlled object to meet the constraint equation 15 within the scope of frequency spectrum. In order to make the circuit satisfy the constraint conditions, being a constant, Q is less than 1 or a function with a low-pass nature. In practice, Q is about 0.95. S is a first-order low-pass filter as below.

$$S = \frac{m}{Ts+1} \quad (18)$$

where m and T are constant, the low-frequency gain of the control object can be rectified to one, and the higher resonant peak can offset by the filter, so that it does not do damage to stability. It can enhance the high frequency attenuation characteristics of the forward channel, and improve the stability and resist the high-frequency interference.

4 Simulation analysis and experimental study

4.1 Comprehensive control strategy

As a single-phase APFC, the two-level APFC can adopt the existing control algorithms. The system control block diagram of the two-level APFC designed with voltage outer loop and current inner loop is shown in Fig.7.

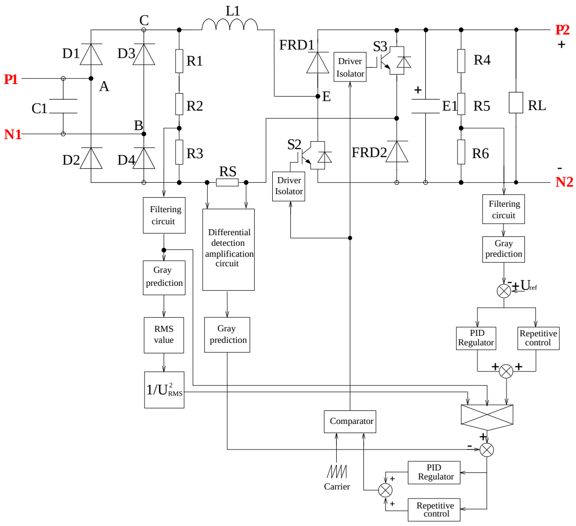

Fig.7 Control block diagram of the two level APFC with double-loop control

As an outer loop, the voltage loop is used to control the output DC voltage. The error between the given output voltage U_{ref} and the actually detected output voltage U_o are delivered to an error amplifier with low-pass filtering and amplification, the error amplifier can be a PID regulator. The purpose of the error amplifier is to maintain the output voltage unchanged.

A multiplier is employed to multiply the output of the voltage loop, the reference input voltage (sinusoidal half-wave), and the reciprocal of the squared RMS of input voltage, and then output a comprehensive current reference signal. The effect of the reciprocal of the squared RMS of input voltage is to make the APFC meet the requirements for the worldwide power supply. In addition, it also can maintain input power constant.

As an inner loop, the current loop is used to control the input AC current. The error between the reference current signal and the detected current signal are delivered to a current PI regulator. The current PI regulator output the final control signal, after compared with the triangular carrier or saw tooth carrier, which can output the original PWM driving signal.

In the paper, a novel comprehensive control strategy is designed, which integrates the double-loop control, gray prediction and repetitive control. It can improve the system dynamics and steady-state characteristics and suppress periodic interference. The control block diagram of the recommended comprehensive control for the two-level APFC is shown in Fig.8, where the voltage outer loop and current inner loop are controlled with repetitive control strategy. Output DC voltage, boost inductor current and input AC voltage are controlled by gray prediction control strategy.

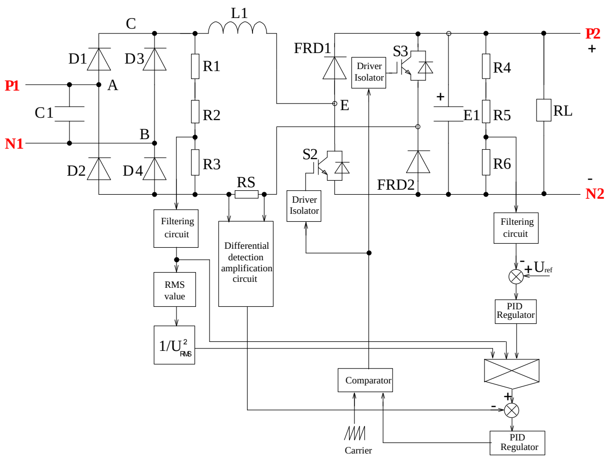

Fig.8 Control block diagram of two level APFC with comprehensive control

4.2 Simulation analysis

The two-level APFC is simulated by means of MATLAB/Simulink, including the power circuit and control circuit. The simulation platform of double loop control for the two-level APFC is shown in Fig.9, and that of comprehensive control for the two-level APFC is shown in Fig.10.

In order to imitate the practical situations to the largest degree, simulation parameters and conditions are specially stated as follows: the tow-level APFC is powered by standard single-phase power supply with RMS value of 240V, the desired output DC voltage is 385V, the inductance of L1 is 0.5mH, the switching frequency is 20kHz, the load resistance is 43.25Ω, the rated load is 3.5kW. Furthermore, let the voltage drop of FRD be 1.5V, the conduction voltage drop of power device IGBT be 1.5V, the voltage drop of rectifier diode be 2.0V, inductor DC resistance be 0.15Ω, AC capacitor C1 be 2.2μF and its ESR be 5mΩ, electrolysis capacitor E1 be 3,300μF and its ESR be 0.1Ω.

In order to arrive at a precise and evident comparison, the performance the traditional double-loop controlled APFC and the novel two-level comprehensively controlled APFC are adjusted to the best working conditions.

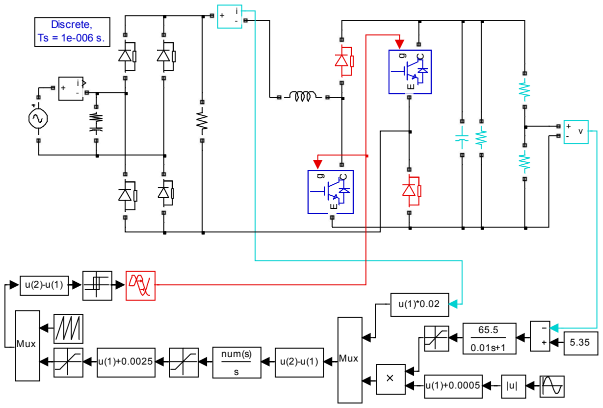

Fig.9 Simulation circuit of the two level APFC with double-loop control

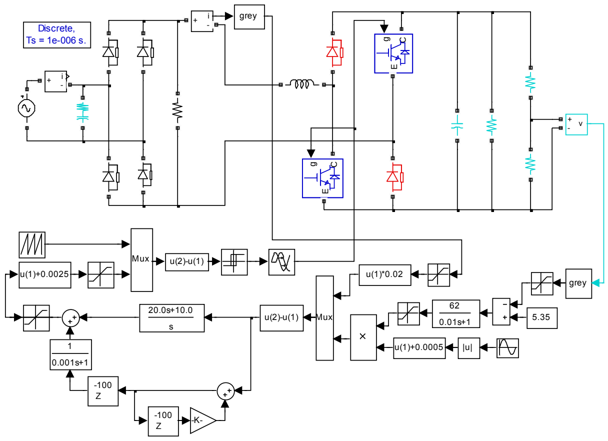

Fig.10 Simulation circuit of the two level APFC with comprehensive control

Case1: Neglecting a switching cycle delay

When not considering the simulation delay for a switching cycle and considering the voltage drops of all the power devices, for the double loop control and the comprehensive control for two-level APFC, at the rated output power, RMS of fundamental current is 16.84A, THD is 5.19%, the average of output DC voltage is 385V, the peak to peak value of ripple voltage is 8V.

When not considering the simulation delay for a switching cycle but considering no voltage drop of power devices, RMS of fundamental current is 15.93A, THD is 5.46%, the average of output DC voltage is 385V, and the peak to peak value of ripple voltage is 9V. The waveforms of the mains current are shown in Fig.11. The waveforms of the output DC voltage are shown in Fig.12. Evidently, when not considering the simulation delay for a switching cycle, the effects of double loop control and the comprehensive control for the two-level APFC is the same on the whole.

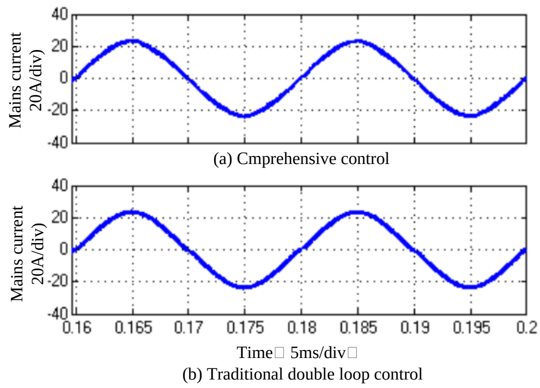

Fig.11 Waveforms of mains current at 3.5kW load

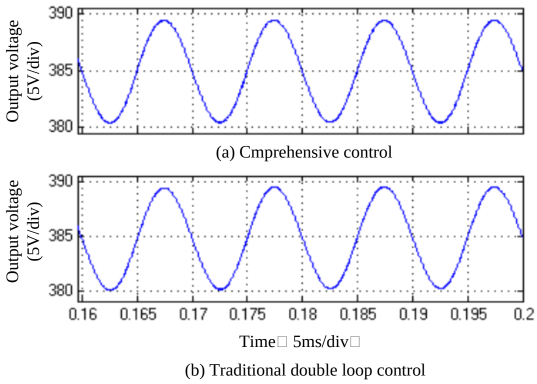

Fig.12 Waveforms of DC voltage at 3.5kW load

Case 2: Considering a switch cycle delay

When considering the simulation delay of a switching cycle and the other simulation conditions remain unchanged, for the double loop control and the comprehensive control for two-level APFC, at the rated output power, the waveforms of inductor current are shown in Fig.13. The waveforms of the mains current are shown in Fig.14.

Evidently, when considering the simulation delay for a switching cycle, the effects of the comprehensive control are better than those of the double-loop control for the two-level APFC. The waveforms of the DC voltage are shown in Fig.15. When load resistance remains unchanged, the effects of the comprehensive control remains unchanged and the effect of double-loop control deteriorates, but the average output DC voltage increases. When load resistance changes, the waveforms of the DC voltage are shown in Fig.16. The effects of the comprehensive control and the double loop control are the same as each other. Because the capacitance of the electrolysis capacitor is large enough, its filtering effect is strong so far.

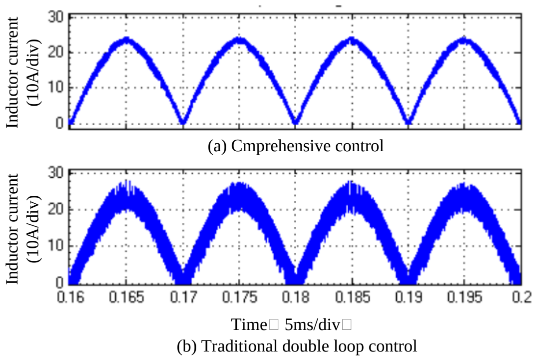

Fig.13 Waveforms of inductor current at load of 3.5kW

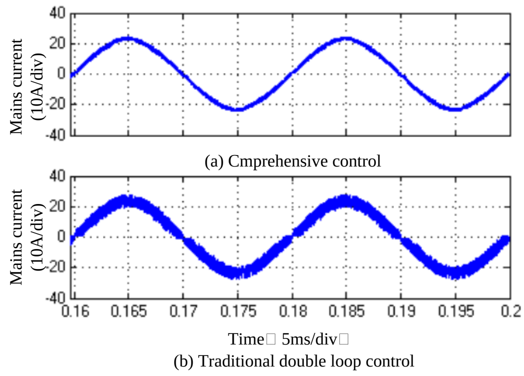

Fig.14 Waveforms of mains current at load of 3.5kW

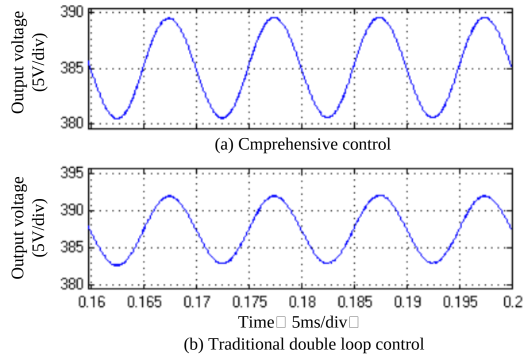

Fig.15 Waveforms of DC voltage at load of 3.5kW

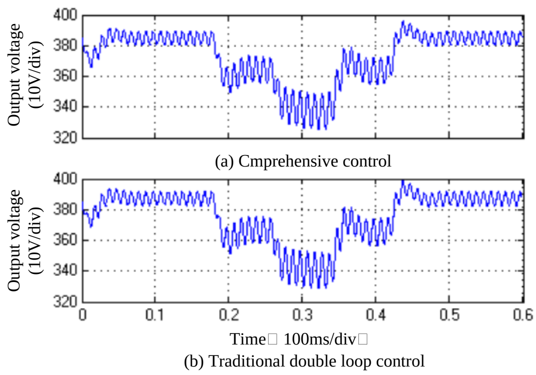

Fig.16 Waveforms of DC voltage at varying load

4.3 Experimental Study

Experimental parameters and conditions are stated as follows: the tow-level APFC is powered by standard single-phase power supply with RMS value of 240V, the desired output DC voltage is 385V, the inductance of L1 is 0.5mH, the switching frequency is 20kHz. The estimated overall efficiency is 95%, DSP TMS320F28335 is selected as the kernel controller.

The discrete boost inductor is made of magnetic material FeSiAl, and the inductance is 0.5mH under 20kHz and rated load current. The electrolysis capacitor is 6x680μF/450V, IGTB is IKW50N60H3: 50A/100°C/600V anti-paralleled with FWD. FRD is FFAF60UA60DN: 2x30A/45°C/600V. The diode rectifier is D50XB80. The driver of IGBT is HCPL-316J, which is powered by single channel power supply +15V.

Eventually, the two-level APFC platform is implemented with the double-loop control and the comprehensive control, including hardware design and software program. The overall efficiency is not less than 0.92 under light load and higher than 0.98 under rated load. The input current is perfect with only a small high frequency ripple. The average output DC voltage is 385V under light load and 380V under 3.5kW load. The ripple of high frequency voltage of electrolysis capacitor is small. When the comprehensive control is employed, the dynamic and static characteristics of the current waveform at mains side are better than those when the double-loop control is employed.

Fig.17, Fig.18 and Fig.19 shows the measured waveforms of mains voltage, mains current and the spectrum distribution of mains currents at loads of 1.4kW, 3.1kW, and 4.4kW under the comprehensive control. Fig.20 shows the measured waveforms of output DC voltage with soft power-on, soft-start and load change of 0.5kW.

Apparently, the newly proposed single-phase active power factor correction (APFC) equipped with the said comprehensive control gains satisfactory results, more specifically, better power factor correction, smaller static error, and quicker dynamic response.

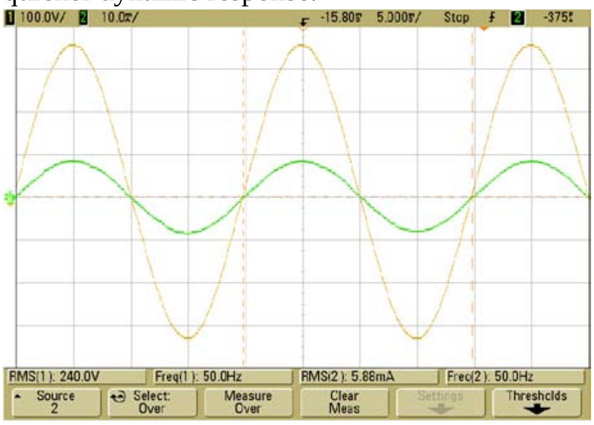

Fig.17 Waveforms of measured mains voltage and mains current at 1.4kW

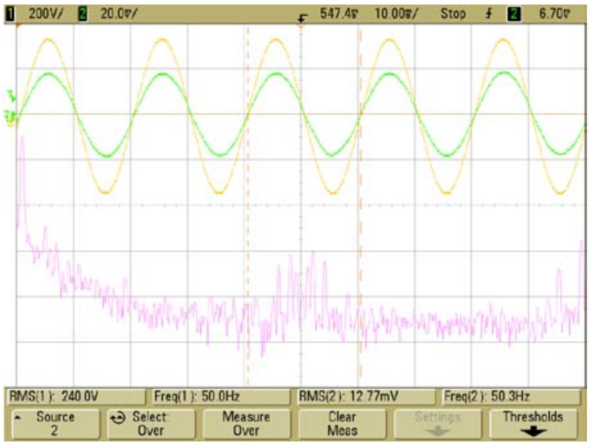

Fig.18 Waveforms of measured mains voltage, mains current and the spectrum distribution of mains current at 3.1kW

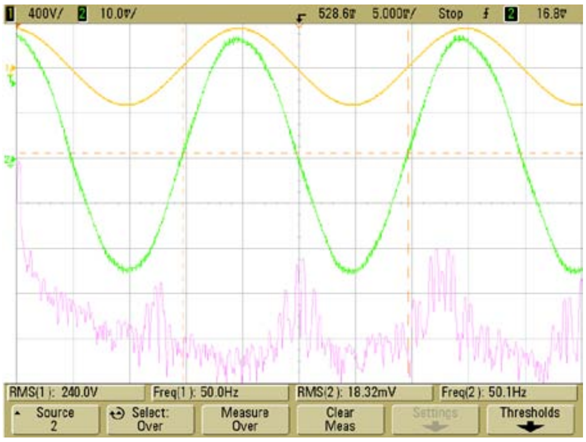

Fig.19 Waveforms of measured mains voltage, mains current and the spectrum distribution of mains current at 4.4kW

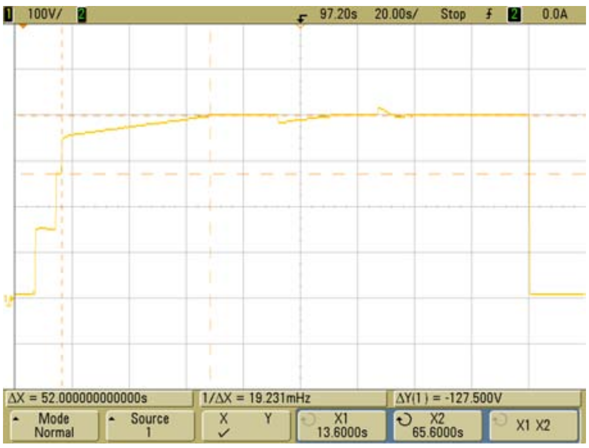

Fig.20 Waveforms of measured output DC voltage

Though the novel single-phase active power factor corrector has the ability to eliminate the zero crossing distortion of the mains current, which is be superior to the traditional topology, it increases the difficulty to the design of boost inductor, due to the increase of voltage stress across its two terminals.

While at the same time, the new topology can be used as active power filter to filter harmonic currents at the DC side, instead of at the AC side. Some preparatory work has been done to verify the idea.

5 Conclusions

Firstly, a novel two-level APFC topology is presented and analyzed, which can form two voltage levels of $\pm U_o$ between the output end of boost inductor and the negative rail of DC link. The feature is helpful to eliminate the zero-crossing distortion of the mains current. Secondly, a gray prediction, named GM(1, 1) is employed to predict the electrical quantities required in the next switching cycle in order to acquire a better real time control for the novel two-level APFC topology. Thirdly, repetitive control strategy is utilized to reduce steady state errors of input AC current and output DC voltage, because the novel two-level APFC is powered by a periodic sinusoidal voltage. Finally, a comprehensive control strategy based on the traditional double-loop PID regulator, gray prediction and repetitive control is designed, simulated by means of MATLAB/SIMULINK and implemented. The obtained results prove comprehensive control strategy, which makes the novel two-level APFC an ideal APFC with unitary power factor at mains side and more satisfactory dynamic and static performances.

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