Design of a LNA in the frequency band 1.8-2.2GHz in CMOS Technology

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Abstract: - As the first active stage of receivers, Low Noise Amplifier (LNA) play a critical role in the overall performance and their design is governed by the parameters. This paper presents the design of LNA and development of low bias (V_{DS}=3V,I_D=20mA), which operating in frequency range 1.8-2.2GHz using a feedback circuit. The proposed Single Stage and Two Stage LNA are simulated with Advanced Design System (ADS) 2012. The paper compares the simulated results of Single Stage LNA and Two Stage LNA. Simulation results of the final Single Stage LNA have indicated that the S21=16.332±0.348dB, NF=0.445± 0.05dB, S12<-22.441dB and S11<-16.631dB over the wide frequency band of 1.8-2.2GHz. Simulation results of the final Two Stage LNA have indicated that the S21=29.929±0.591dB, NF=0.482±0.055dB, S12<-40.783dB and S11<-16.126dB over the wide frequency band of 1.8-2.2GHz.

Key-Words: - Low noise amplifier, HEMT, Feedback, Noise Figure, ADS, RF

1 Introduction

In the era of wireless communications, devices that are able to exchange information through modulated radio frequency waves acquire more and more importance. Wireless communication and its applications have travelled through rapid growth in recent years. Cellular systems, WLANS, Bluetooth as well as WPANs have undergone numerous generations of evolution in the swift development in wireless communication [1]. These are required to be portable, low cost, with low power consumption and must meet several specifications given by the telecommunication standard they refer to. In the recent years, a great progress has been made in all these fields. Great importance assumes the advent of digital treatment of information, which enables far better performances over the analog counterpart. Many advances have been made in the signal modulation techniques too, thus allowing an increase of the communication distances with the minimum possible error. A device that is able to communicate with others must be equipped with a transmitter and a receiver.

Our work will focus on the latter, in all its aspects. LNAs are key components in the front-end receiver system, which amplify the received Radio Frequency (RF) signal from antenna. Nowadays, a lot of effort has been put into the design of LNA to provide gain as high as possible with lowest noise figure possible and lowest cost of fabrication.

LNAs are used at receiver's side in all communications systems in order to offer the first amplification to the received signal with the addition of the minimum noise. Although LNAs are parts of the receivers only, their design should

take into account the general features of the whole communications system[2].

2 LNA design

The design of LNAs, there are several common goals. These contain minimizing the noise figure of the amplifiers, providing gain with sufficient linearity, and supporting stable input impedance are all-important considerations [3]. In the paper, a Single Stage LNA and Two Stage LNA based on the E-pHEMT is simulated in ADS 2012 software. ATF-54143 transistors based on room temperature S-parameter are used.

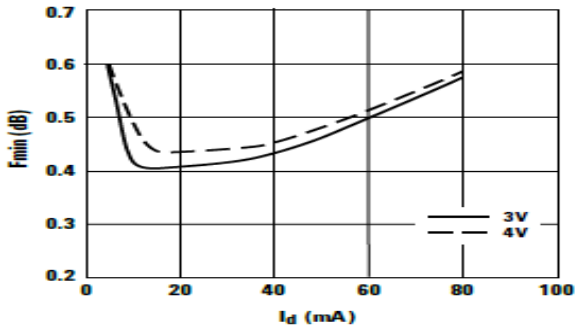

Fig. 1.Fmin vs. Ids Tuned for Max OIP3 and F_{min} at 2GHz

In this paper, the optimized LNA for a narrowband application around 2.0GHz are carried out by the ADS software of Agilent Technologies Inc. The device selected for this amplifier is the Agilent ATF-54143, an Enhancement-Mode Pseudomorphic HEMT(E-pHMT). This transistor offers good noise figure, high linearity, and significant gain up to 6GHz, making it useful a variety of applications from LNAs to small transmitter power amplifiers. Agilent Technologies's ATF-54143 is a high dynamic range, low noise, E-PHEMT housed. The combination of high gain, high linearity and low noise makes the ATF-54143 ideal for cellular/PCS base stations, MMDS, and other systems in the 450 MHz to 6GHz frequency range. In our LNA design, the most important factors are low noise, moderate gain, matching and stability [4]. In the ATF-54143 data sheet, we know the Fmin approach minimum value, when a drain-source voltage of Vds=3V, Ids=20mA and f=2GHz. The picture is shown in Fig. 1.

2.1 Bias Circuit Design

An indispensable building block in any RF circuit is the active or passive biasing network. The purpose of biasing is to provide the appropriate quiescent point for the active devices under specified operating conditions and maintain a constant setting, irrespective of transistor parameter variations and temperature fluctuations [5].

The S-parameters of the transistor are fixed and do not change as the correct bias current is maintained. In order to meet the design goals for noise figure, intercept point and gain, the drain source current(Ids) was chosen to be 40mA. FET in the amplifier is biased at a Vds of 3V and Id of 20mA, giving a total current of 40mA. As indicated by the characterization data shown in the device data sheet, 20mA gives the best NF. Also shown in the data sheet, a 3V drain to source voltage (Vds) gives a slightly higher gain and is also preferred since it easily allows the use of a 5 V regulated supply. The bias circuit of ATF-54143 is shown in Fig. 2. After processing of ADS simulation Data, we can obtain the actual bias circuit. The actual bias circuit is shown in Fig. 3, the actual electricity current and voltage can be seen in the figure. The resistors are calculated to be R1=50 ohm, R2=334.56ohm, R4=40.42ohm. Conduction a DC analysis in the ADS circuit simulator produces ID=20mA ,IdS=39.9mA and VD=3.0V, which are very close to our original goal (minimum noise figure).

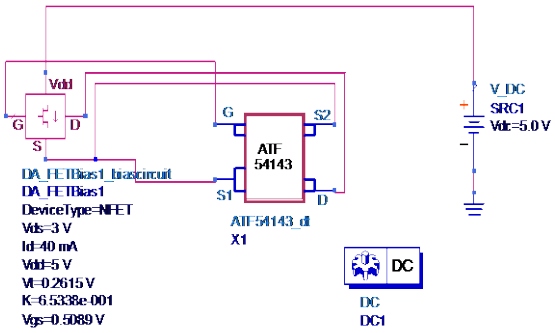

Fig. 2. ATF54143 bias circuit is designed in ADS

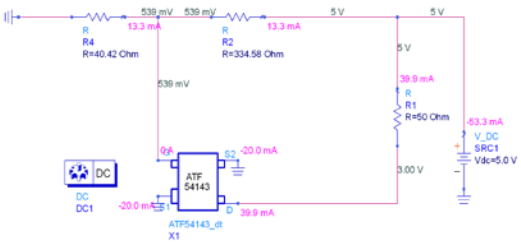

Fig. 3. Actual bias circuit is designed in ADS

2.2 Stability Analysis

Stability is important to consider when designing microwave transistor amplifiers. If a transistor is unconditionally stable it will not oscillate with any passive termination. On the other hand a potentially unstable transistor can be stabilized by adding resistive loadings. One way of expressing necessary conditions for unconditional stability is :

$$K=\frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|}>1 \qquad (1)$$

And

$$\Delta = S_{11}S_{22}-S_{12}S_{21} \qquad <1 \qquad (2)$$

When the K>1, the circuit will be unconditionally stable for any combination of source and load impedance. When K<1 then circuit is potentially unstable and oscillation may occur with a certain combination of source and /or load impedance presented to the transistor. The K factor represents a quick check for stability at given frequency and given bias condition.

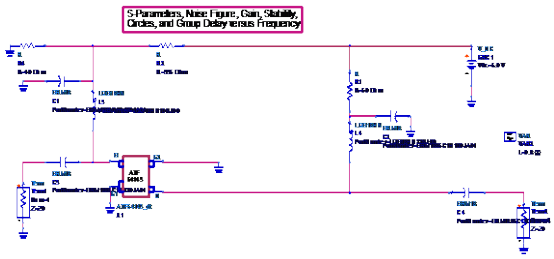

Fig. 4. The schematic diagram of simulating stability factor, when the feedback inductor does not add to the FET's source.

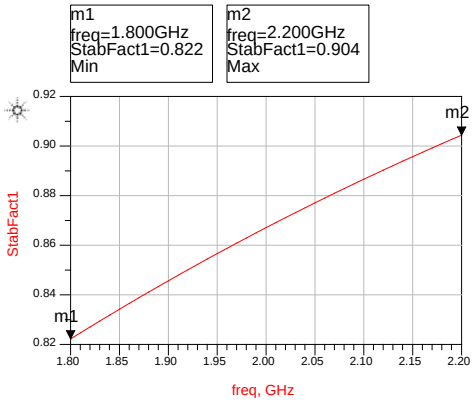

Fig. 5. the chart of simulating stability factor, when the feedback inductor does not add to the FET's source.

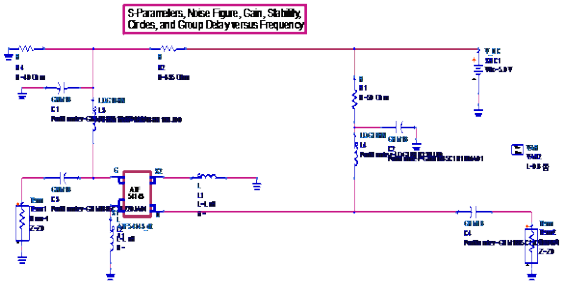

Fig. 6. The schematic diagram of simulating stability factor, when the feedback inductor adds to the FET's source.

The schematic diagram of simulating stability factor is shown in the Fig. 4, Here, the DC source of 5V supplies DC bias. C1, C2 and L3, L4 are bypass capacitors and choke inductors, respectively. where C1=C2=C3=C4=270pF, , L3=L4=120nH. Actual models of capacitor and inductor in the above circuit were adopted from the Murata Components Library for Agilent

ADS. The accuracy and efficiency of simulations have been improved, since physical effects of the layout components were taken into account. C1 and C2 can improve the stability of low frequency. When the feedback inductor does not add to the source, the LNA stability can be seen in the Fig. 5. In Fig. 5, we can know the K<1 over the frequency band of 1.8-2.2GHz. In order to get unconditionally stable circuit, we can add negative feedback inductor to the source of the transistor.

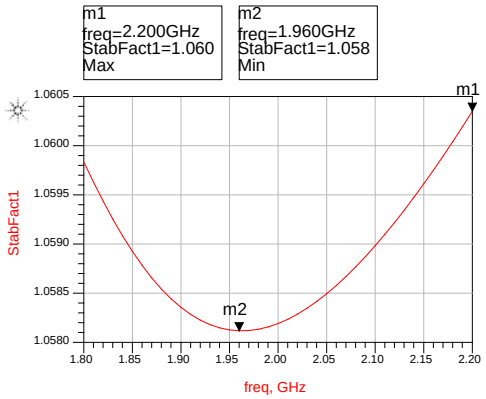

Fig. 7. The chart of simulating stability factor, when the feedback

When we add feedback inductor in the FET's source, the maximum stability is achieved for L1=L2=0.8nH. The schematic diagram of simulating stability factor be seen in Fig. 6. In Fig. 7, we can know the K>1 over the frequency band of 1.8-2.2GHz. This simulation includes goals to force the geometric source and load stability factors, mu_source and mu_load respectively, to be >1 over a broad frequency range.

2.3Noise in amplifiers

At this point, it is worthwhile to examine the notion of noise, and modeling of noise in fundamental circuits. Amplifiers are being used to enhance the signal that is generated by a weak signal source. LNAs are being used to receive and amplify weak signals transmitted by distant transmitters, which may be fixed or mobile, or installed on board a satellite. The total signal received at the input of the amplifier does not only consist of the signal sent by the transmitter, but in addition, it includes the unavoidable noise signal originating from the internal resistance of the antenna. To obtain a sufficiently high level of signal power with a reasonable signal-to-noise ratio (S/N) at the output of the LNA, the noise inherently generated in the amplifier must be kept as low as possible.

NF is one of the most important parameters to evaluate the radio performance of communication system. It is a measurement of degradation of signal-to-noise ratio (SNR) between the input and output of the component.

Rather, we view and design the RF chain as one entity, performing many iterations among the stages.

The NF can be calculated using the following mathematical equation. In modern RF electronics, we rarely design an LNA in isolation [6].

$$NF(dB) = 10\log F \quad (3)$$

$$\text{Where } F = \frac{(S/N)_{input}}{(S/N)_{output}} \quad (4)$$

We can characterize the performance of a particular receiver element by its NF, which is the ratio of actual output noise of the element to that which would remain if the element itself did not introduce noise. The total NF of a receiver system (a chain of stages) can be calculated using the Friss formula as follows:

$$NF = NF_1 + \frac{(NF_2 - 1)}{G_1} + \frac{(NF_3 - 1)}{G_1 G_2} + \ldots + \frac{(NF_n - 1)}{G_1 \cdots G_{n-1}} \quad (5)$$

Where NF1, NF2,…NFn are the noise coefficient of each amplifier, and G1, G2… Gn are the gains of each amplifier. This result suggests that the noise contributed by each stage decreases as the total gain preceding that stage increases, implying that the first few stages in a cascade are the most critical. It is understandable that the total NF is dominated by the NF1, which is the NF of the LNA. From the Friss formula we can see what affects the cascade amplifier most is the first stage amplifier, so we should try to get an amplifier of smaller noise coefficient and larger gain in the low noise design.

In receiver applications, it is often required to have a preamplifier with as low a noise figure as possible, as the first stage of a receiver front end has the dominant effect on the noise performance of the overall system.

Note that in a cascaded system, the NF1 of the first-stage is directly added to the overall system NF but noise contribution from any stage except the first stage is reduced by the gain of its preceding stage or stages. Therefore, for better noise performance of a cascaded system, along with a high gain the first stage should have the minimum possible NF.

2.4Input matching

Low-noise-amplifier (LNA) is one of the most important key components of the communication system. It is used in the input stage of the receiver. It deals with two important parameters such as gain (in dB) and the noise figure. In a few words, the purpose of the LNA is to amplify the received signal to acceptable levels while minimizing the noise which is added from the channel. According to Friss equation (equation 5), it is very important for RF and microwave engineers to design RF receiver with low noise at the input stage. Once the signal is received by the antenna, passing through LNA, it is not possible to get the high gain and low noise at the same time. That's why, it is important to consider a trade-off between gain and noise figure.

When designing a LNA we should consider many factors. First of all the added noise must be minimized, then we should have acceptable gain, good linearity and input adaptation. The last aspect is very important in order to avoid that part of the incoming signal is reflected back to the antenna and so reducing the signal gain. LNAs are typically designed to provide a 50Ω input resistance and negligible input reactance. This requirement limits the choice of LNA topologies. In other words, we cannot begin with an arbitrary configuration, design it for a certain noise figure and gain, and then decide how to create input matching. Fig. 8 shows a block diagram of the balanced Two Stage amplifier topology. There are three matching networks to be designed: the input to the first stage, the interstage between the first and second stage, and the output of the second stage. Fig. 9 outlines how the impedances to present to the devices were chosen.

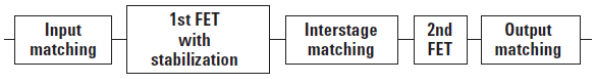

Fig. 8.Balanced amplifier block diagram,utilizing two, Two Stage amplifiers in parallel.

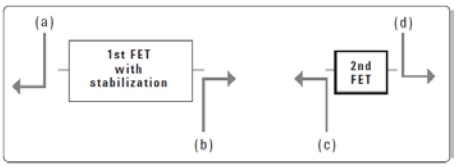

Fig. 9. Choosing impedance. (a) Choose source Z for minimum noise figure, as long as gain remains reasonable. (b) Choose load Z for conjugate matching, after choosing source Z (although a slight mismatch was found to give a higher 1dB gain compression out

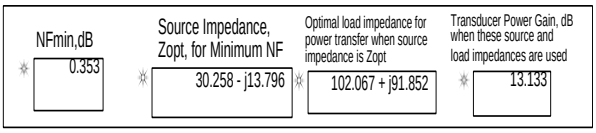

Fig. 10. Gain and noise circles and optimal source and load

In our LNA design, Noise is more important than gain, then a source impedance to minimize Noise could be chosen, so the first stage of the LNA is designed to drive the noise figure and the second stage of the LNA offers necessary gain. Determine the optimal source and load impedances to present to the stabilized FET, via S-parameter and noise figure simulations, using the SP_NF_GainMatchK schematic from the Amplifier DesignGuide. In Fig. 10, we can know that with a source impedance of 23.454-j*5.643 ohm, NFmin = 0.353dB.

2.5Simulation results and discussions

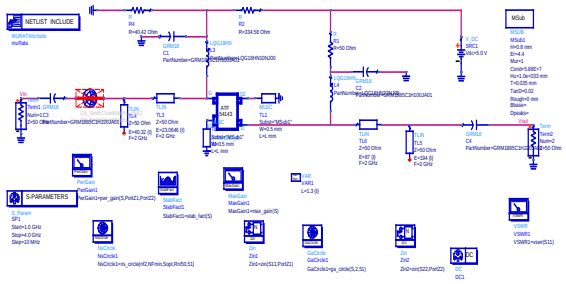

Fig. 11. Single Stage LNA schematic diagram.

After the simulation of the Single Stage circuit shown in Fig.11, which is simulated with ADS 2012. In the figure, the feedback inductor is replaced by Microstrip lines, because the inductor is too small which is difficultly designed. We choose RF4 substrate. It's relative dielectric constant Er= 3.48, board thickness h=20mil, tanδ=0.02, σ=5.8*107 Ω-1/m. Both of the input and output matching networks are composed of microstrip lines. The simulation results are shown in Fig.12, Fig.13, Fig.14 and Fig.15.

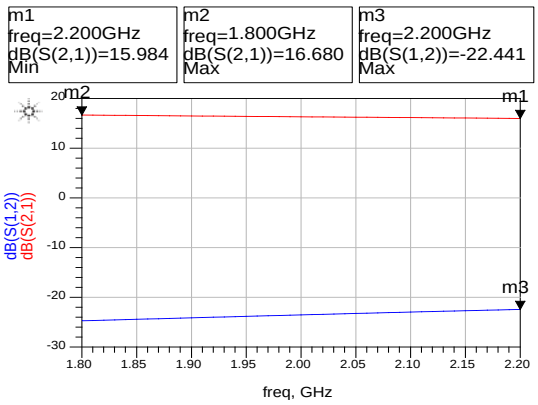

Fig. 12. S12,S21 VS freq for Single Stage LNA

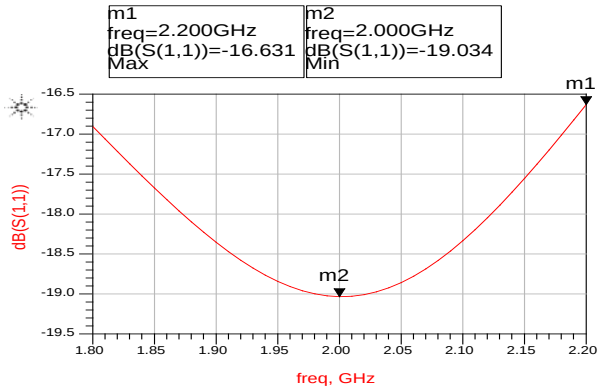

Fig. 13. S11 VS freq for Single Stage LNA.

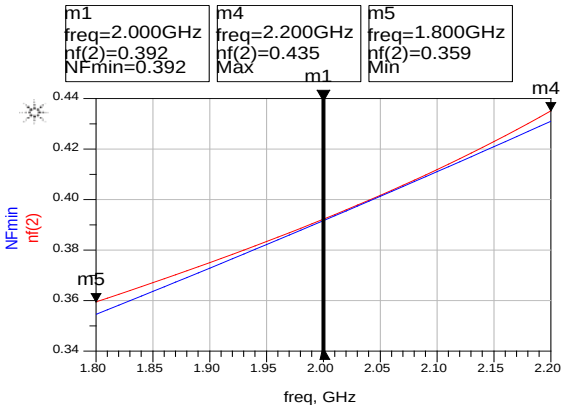

Fig. 14. Noise Factor VS freq for Single Stage LNA.

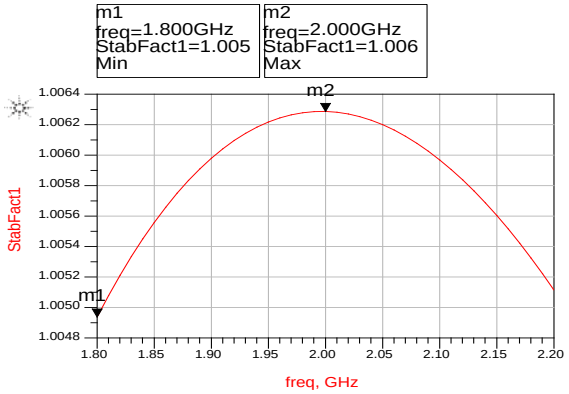

Fig. 15.Stability Factor VS freq for Single Stage LNA.

The simulation of the reverse isolation (S12) and the forward voltage gain (S21) were shown in Fig.12, the LNA exhibits almost S21 of 16.332± 0.348dB, and S12 less than -22.441dB. In Fig.13 we can know S11 are below -16.631dB which indicates that the circuit is well match at the input. The good matching at the input ensures a good noise figure performance. Fig.14 shows the NF of the proposed Single Stage LNA, we can know nf(2)=0.392 = NFmin, when the Single Stage LNA operating in 2.0 GHz, the NF is within 0.359-0.435dB.

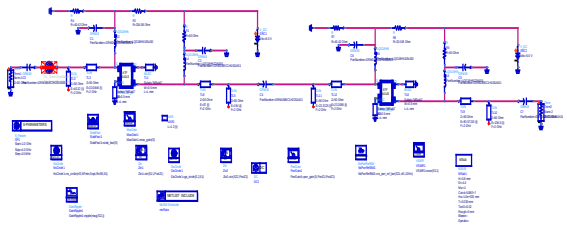

Fig. 16. Two Stage LNA schematic diagram

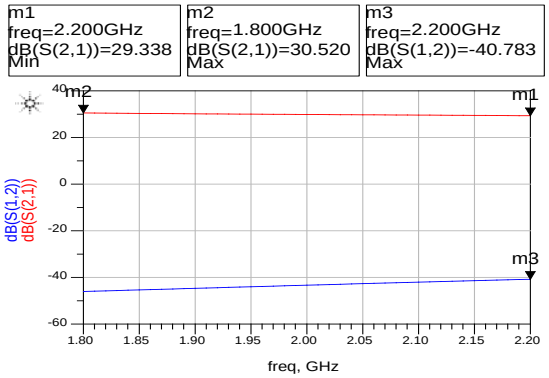

Fig. 17. S12,S21 VS freq for Two Stage LNA.

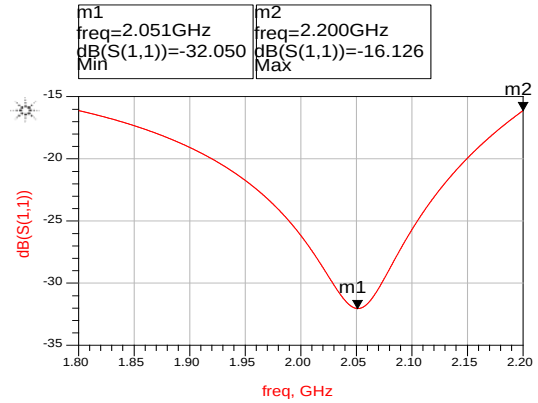

Fig. 18. S11 VS freq for Two Stage LNA.

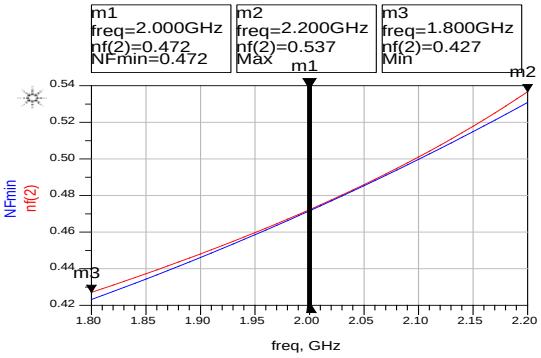

Fig. 19. Noise Factor VS freq for Two Stage LNA.

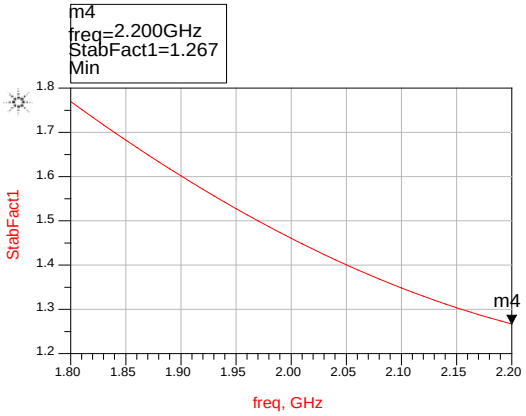

Table 1. Comparative Results of Single Stage LNA and Two Stage LNA

	Single Stage LNA	Two Stage LNA
	1.8GHz-2.2GHz	1.8GHz-2.2GHz
S11	-16.631-- -19.034	-16.126-- -32.05
S12(Max)	-22.441	-40.783
S21	15.984-16.68	29.338-30.52
NF	0.395-0.495	0.427-0.537

Table2. Performance comparison of the proposed Two Stage LNA with other previous LNAs

	BW(GHz)	S11(dB)(Min)	S21(dB)(Min)	S12(dB)(max)	NF(dB)(max)
This work	1.8-2.2	-32.05	29.338	-40.783	0.537
[7]	1.8-2.2	-28.92	16.68		1.25
[8]	1.85-2.48	<-5.5	16		1.77
[9]	1.9	-9.34	29.13	-43.02	0.44
[10]	1-2	<-12	15		<0.8
[11]	2	-9.842	15.87	-42.86	3.775

After the simulation of the Two Stage circuit shown in Fig.16, the input, interstage and output matching networks are composed of microstrip lines. The simulation results are shown in Fig.17, Fig.18, Fig.19 and Fig.20.

The simulation of S12 and S21 were shown in Fig.17, the LNA exhibits almost S21 of 29.929± 0.591dB, and S12 less than -40.783dB. In Fig.18 we can know S11 are below -16.126dB which indicates that the circuit is well match at the

input. The good matching at the input ensures a good noise figure performance. In Fig.19, we can know nf(2)=0.472 = NFmin, when the Two Stage LNA operating in 2.0 GHz.

In this paper, we compared Single Stage LNA with Two Stage LNA, the results are shown in Table1. The simulation results and a comparison with other published works are presented, the results are shown in Table 2.

As a comparison, the noise figure of Single Stage LNA is less than the noise figure of Two Stage LNA, the Power Gain of Two Stage LNA is more than the Gain of Single Stage LNA.

Conclusion

In this work, the LNA operating from 1.8 GHz to 2.2 GHz had been designed. Feedback technique has been employed in the LNA design in order to meet the design specification over the wide frequency ranges. The matching and biasing circuits are also carefully designed so that the design specifications are met with lowest count parts. Tuning and optimization of the circuit is very crucial to make sure that the LNA gives the best performance. The final Single Stage LNA and Two Stage LNA with Murata components and microstrip lines are designed with ATF-54143. The simulation results of the final Single Stage LNA show that the gain (S21) is above 16.332±0.348dB, the gain was almost flat over the whole band, the reverse gain (S12) less than -22.441dB, the input reflection coefficient (S11) below -16.631 dB, NF less than 0.495 dB. The final Two Stage LNA achieves S21 is 29.292 ±0.591 dB, the gain was almost flat over the whole band, S12 below -40.783, S11 below -16.126dB, NF was 0.427-0.537 dB within the entire band was exhibited.

We could choose proper structures according to our demands in practical circuit design. The proposed Single Stage and Two Stage LNA are good candidate for wireless applications due to its low NF and high gain.

4.Acknowledgment

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