Performance Analysis of Novel Domino XNOR Gate in Sub 45nm CMOS Technology

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Abstract: - In this paper, three new versions of domino XNOR gate circuits are proposed. The proposed circuits adopt mixed N and P type transistor in the pull-down network. All performance parameters are measured at 25°C and 110°C. In first proposed circuit, it lowers the total leakage power by 8% to 12%, PDP is reduced by 6% to 9% and A.C noise margin is enhanced by 7% as compared to standard n-type XNOR gate. Second proposed circuit having multiple threshold voltage, lowers the total leakage power by 47% to 57%, PDP is reduced by 80% to 86%, and A.C noise margin is enhanced by 33% as compared to standard n-type XNOR gate. Third proposed circuit having multiple power supply, lowers the total power consumption by 56% to 65%, PDP is reduced by 83% to 88% and A.C noise margin is enhanced by 58% as compared to standard n-type XNOR gate.

Key-Words: - domino logic, gate oxide leakage current, noise margin, multiple threshold voltage, subthreshold leakage current, XNOR gate.

1 Introduction

Domino circuits are applied in large application such as microprocessor to realize many complex and wide fan in logic function such as wide OR, XNOR gate due to superior speed and low area characteristics of domino CMOS circuits as compared to static CMOS circuits. This circuit is placed into the critical execution path. The XNOR gate is one of the fundamental arithmetic unit used in VLSI system. Inputs of the XNOR gate required two phase signal, one is original signal and other is inverted signal. The inverted signal requires additional gate. The extra inverter not only increases the power consumption but also effect the performance of the domino circuit. Domino XNOR gate with single phase input signal increases the performance of the domino circuit and also area is reduced [1], [17].

As technology is scaled down, supply voltages also scaled down to keep the dynamic power at acceptable levels, and at the same time threshold voltage (V_t) is also scaled down to meet the performance requirements [2], [19]. However, subthreshold leakage and gate oxide leakage currents are increased exponentially with the scaling of threshold voltage and gate oxide thickness (T_{ox}), hence power consumption increases and noise immunity decreases. To solve the problem of high subthreshold leakage current, many circuit level techniques have been implemented including body bias control [3], input vector control [4], transistor stack effect [5], dual V_t CMOS [6], sleep switch [7], [8], [9]. Dual V_t domino technique [6] is realized by using low V_t transistor in the evaluation path and high V_t transistor in the precharge path of the circuits. According to Kao, high clock and high inputs (CHIH) are preferable to reduce subthreshold leakage current in dual V_t footless domino gate.

Combination of subthreshold and gate oxide leakage current in footless domino circuit was carried out by Kursun [10], [11], [18]. Considering the major effect of gate oxide leakage current on the total leakage current, it shows that at low temperature clock high and input low (CHIL) state is preferable and at high temperature clock high and input high (CHIH) state is preferable in domino footless circuit. Sleep switch methods are efficient for reducing both subthreshold and gate oxide leakage current. High V_t nMOS switch is added to the dynamic node in domino footless circuit. High clock and active sleep switch suppress subthreshold leakage current but produces high output of domino

gate that places highest gate oxide leakage current to the fan out domino gate [7].By adding two sleep switch, one at dynamic node and other at output node, both subthtreshold and gate oxide leakage current are reduced[8],[9].

Combination of clock and inputs signal states is provided for footed domino circuits to optimize the total leakage current [12]. According to [12], subthreshold and gate oxide leakage current are not only function of inputs state but also clock signal state. If subthreshold is the dominant source then CHIH is the best choice. Similarly, if gate oxide leakage current is the dominant source then CLIL state is preferable.

Power dissipation of the domino circuit is divided into three components [13]:

$$P_{Total} = P_{Dynamic} + P_{Leakage} + P_{Short\ Circuit} \quad (1)$$

$P_{Dynamic}$ is the power consumed during capacitance charging and discharging, $P_{Leakage}$ is the total leakage power of the circuit and this power increases as the technology is scaled down, and $P_{Short\ Circuit}$ is the power dissipated when direct current flows from power supply to ground.

$$Pdynamic = C \times VDD^2 \times Fclk \quad (2)$$

C is the capacitive load at the evaluation node, F_{clk} is the clock frequency.

$$P_{Leakage} = I_{Leakage} \times VDD \quad (3)$$

where $I_{Leakage}$ is the combination of subthreshold and gate oxide leakage current.

$$P_{Short\ Circuit} = I_{SC} \times VDD \quad (4)$$

I_{SC} for domino logic gate is the contention current that flows between the evaluation network and pMOS keeper during evaluation mode. This power dissipation must be kept low for better operation of the domino circuit.

In this paper, we present three new versions of XNOR domino circuit, these circuits address the short-comings of standard n-type XNOR gate. First Proposed circuit has N and P type mixed transistor in the pull-down network and all transistors are low threshold voltage, second proposed circuit uses multiple threshold voltage transistor, and third proposed circuit has multiple power supply voltage with multiple threshold voltage. Proposed circuits improve circuit performances as compared to standard n-type XNOR gate. The remainder of this paper is organized as follows. Section 2 discusses leakage current characteristic of single transistor .In section 3 describe the operation of standard n-type XNOR domino circuit. In section 4, we describe the proposed XNOR circuits. In section 5, we present simulation results for comparing the circuit performance with the standard n-type XNOR circuit, and Section 6 concludes this paper.

2 Leakage currents analysis of single transistor

In CMOS technology, gate oxide leakage current is neglected for 180nm technology because gate oxide thickness (T_{ox}) is greater than 20Aº [14], [15]. As technology is scaled down to 45nm, both subthreshold and gate-oxide leakage currents increase. Thin oxide provides passage for direct tunneling of the electron and hole. Gate oxide and subthreshold leakage currents depends upon the voltage bias applied at the gate, drain and source are shown in Fig1.Maximum forward gate oxide leakage current flows when transistor is in active mode and potential difference between gate-source and gate-drain is maximum. Subthreshold leakage current is neglected because potential difference between drain and source is zero as shown in Fig1 (a). Fig1 (b) shows reverse edge gate oxide leakage current and subthreshold leakage current. To avoid both subthreshold and gate oxide leakage current, the entire terminal must have same potential as shown in Fig 1(c) and Fig 1(d).

Gate oxide leakage current of pMOS is very small as compared to nMOS because mobility of electron is higher than hole. High V_t transistor reduces both gate oxide and subthreshold leakage current at 25°C and 110°C as shown in Table 1. Here transistor length is 45nm, transistor width is 1µm, Low-V_{tn}=0.22V, Low-V_{tp}=-0.22V, High-V_{tn}=0.466V, High-V_{tp}=-0.4118V, VDD=0.8V. Subthreshold leakage current of low V_t nMOS transistor is 22.32 times higher than subthreshold leakage current of a high V_t pMOS transistor at 110°C [9].Similarly, Subthreshold leakage current of low V_t nMOS transistor is 3.7 times higher than subthreshold leakage current of a high V_t pMOS transistor at 25°C. At 110 Subthreshold leakage current of low V_t nMOS transistor is 22.32 times higher than subthreshold leakage current of a high V_t pMOS transistor at 110°C subthreshold leakage current of a low V_t transistor is 6.7 times higher than gate oxide leakage current of a low V_t nMOS transistor. At high temperature subthreshold leakage current is the dominant source of leakage current. Similarly, at 25°C, gate oxide leakage current of a

low V_t nMOS transistor is 2.5 times higher than subthreshold leakage current of a low V_t nMOS transistor. Gate oxide leakage current is the dominant source of leakage current at low temperature. At 110°C, gate oxide leakage current of a low V_t transistor is 1.1 times higher than gate-oxide leakage current at 25°C, it is weekly temperature dependent. Subthreshold and gate oxide leakage currents increase with the upsizing of the transistors width with temperature increases, keeping transistor length constant as shown in Fig.2 and Fig.3.

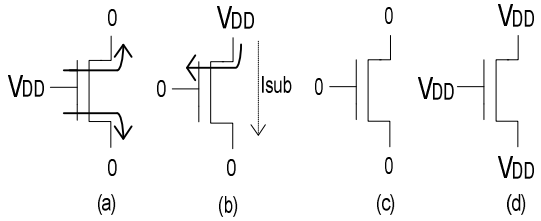

Fig 1. (a) Maximum gate-oxide leakage current state, (b) Maximum subthreshold leakage current state, (c) and (d) condition to avoid both subthreshold and gate oxide leakage current .

Table 1
Subthreshold and gate oxide leakage current at two different temperatures

Leakage current (nA)	NMOS		PMOS	
	Low-Vt	High-Vt	Low-Vt	High-Vt
Isub (110°C)	1733.4	198.36	1243.3	77.628
Igate(110°C)	256.33	3.8465	7.5415	26.26
Isub (25°C)	89.397	44.983	74.759	24.142
Igate (25°C)	225.97	3.7038	7.4768	26.243

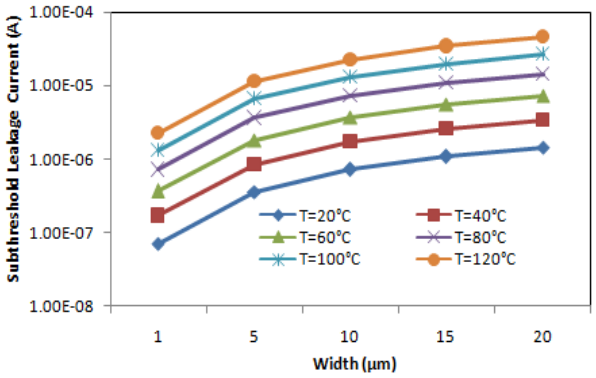

Fig 2. Variation of the subthreshold leakage current with temperature and width of transistor.

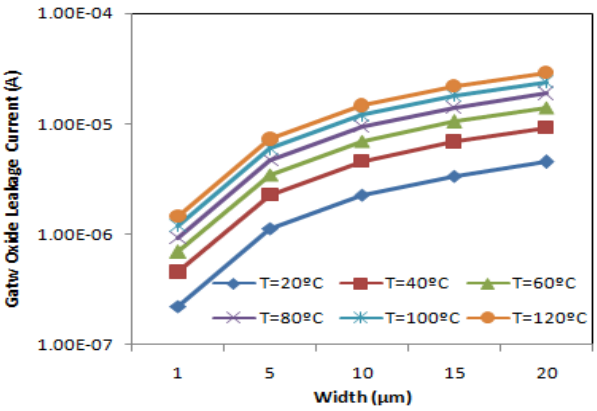

Fig 3. Variation of the gate-oxide leakage current with temperature and width of transistor.

3 Standard n-type XNOR gate

The standard n-type domino XNOR gate is shown in Fig 4. Here pull-down network consists of all n-type transistors. P–type domino XNOR gate has a great advantage as compare to n-type domino XNOR, it effectively suppress both subthreshold and gate oxide leakage current at the expense of speed. N-type domino circuit has higher speed and higher power consumption, and p-type domino circuit has lower speed and lower power consumption. Drawback standard n-type or p-type is that the input signals must be two phases, original and its inverted signals. Extra inverters must be added in the circuit to get inverted signal of original signal. Adding inverter increases the extra power consumption, propagation delay which extremely affects the performance of the domino XNOR gate.

The dynamic node also gives XNOR gate logic V_n=AʘB, dynamic node is connected to inner inverter to provide XOR gate logic V_p=A⊕B, V_p is directly connected to the output inverter to provide XNOR logic V=AʘB. The clock signal divides the circuit operation into two phases, precharge and evaluation phase. In precharge phase, CLK is low, dynamic node is charged to V_{DD} by pull-up transistor P1 and output is high, at that time transistor N5 is cut-off so no direct DC current flows from power supply to ground, transistor N5 avoids short circuit current in the circuit. In evaluation phase, when CLK is high, the pull-up transistor is cut-off and footer transistor N5 is ON. Depending upon the inputs in the pull-down network, a conditional path is established between the dynamic node and ground. If A=0, B= 1 or A=1, B= 0, dynamic node is discharged and output is low.

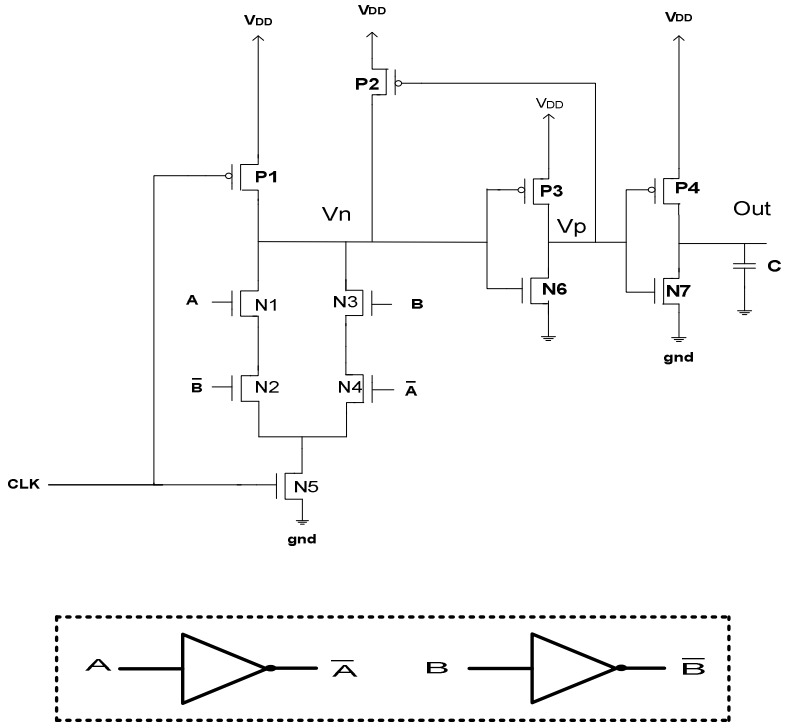

Fig 4. Standard domino XNOR gate.

Output remains high for rest of the inputs. Drawback of this circuit is that it requires two phase input signals and increases propagation delay.

4 Proposed XNOR gates

Focusing on the advantage of n-type device having high speed and p-type device having low power consumption, we proposed three version of domino XNOR circuit. These circuits reduce leakage currents, evaluation delay, dynamic power consumption, power delay product (PDP) and enhance A.C noise margin. First technique is low threshold voltage (LTV) XNOR gate, second technique is multiple threshold voltage (MTV) XNOR gate and third technique is multiple power supply and multiple threshold voltage (MPMT) XNOR gate.

4.1 Low threshold voltage (LTV) technique

This technique adopts N and P type mixed transistor in the pull-down network and all the transistors are low threshold voltage as shown in Fig 5.In this circuit,N1 and P4 are connected in parallel, and P5,N2 are also connected in parallel. Here we do not need any additional inverters to provide inverted input signals. During precharge phase, dynamic node is charged to V_{DD} and output is low. During evaluation phase, if inputs A=B=0 or A=B=1, dynamic node V_n is discharged and output is high. For other combination of inputs, dynamic node is high and output node is low. Here we get XNOR logic with single phase input signals and require small circuit area as compared to standard n-type domino XNOR gate. From the circuit, it is clear that inner inverter is removed hence power consumption is reduced. Drawback of this technique is that it has lower speed as compared to standard n-type domino XNOR gate.

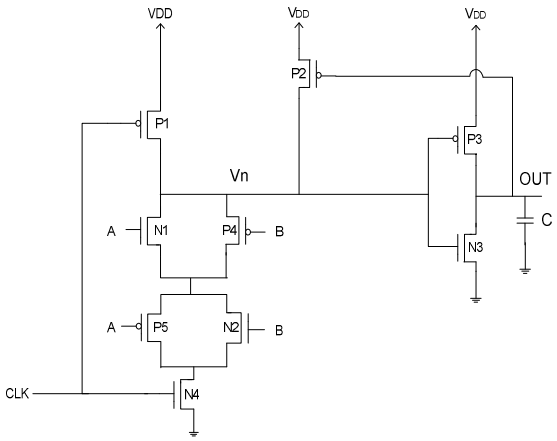

Fig 5. LTV domino XNOR gate.

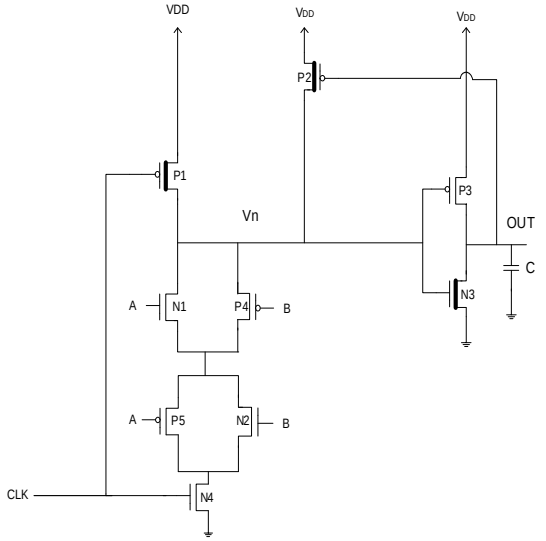

Fig 6. MVT domino XNOR gate.

4.2 Multiple threshold voltage (MTV) technique

Multiple threshold voltage domino XNOR gate is shown in Fig 6. Here, all transistors that can be activated during precharge phase have high-V_t and other have low-V_t that determine the speed of this circuit. Subthreshold and gate oxide leakage current of all high V_t transistor are lesser than low V_t transistor. In precharge mode, turning ON the high-V_t pull-up transistor. When CLK is high, operation of this circuit is similar to previous technique. The advantage of this circuit is lesser power consumption, higher speed, higher noise margin as compared to LTV XNOR gate and standard n-type XNOR gate.

4.3 Multiple power supply and multiple threshold voltage (MPMT) technique

In the proposed design, multiple power supply and multiple threshold voltages are utilized. First power supply (VDD=.8V) is applied to the pull-up transistor and the pMOS of the output inverter. Second, power supply (VDD1) is applied to the keeper power supply VDD1 is shown in Fig 7.Value of VDD1 is lesser than VDD. Using smaller keeper voltage has two significant advantages over standard n- type domino XNOR gate. First, total power consumption is reduced. Second, keeper power supply reduces contention current that flows between keeper transistor and the pull-down network during evaluation phase, this improves the speed of the circuit. If we keep the keeper supply voltage too small, the logic of the circuit will change and the noise immunity will be reduced. The characteristics of power consumption and evaluation delay for different value of VDD1 is shown in Fig 8. As the keeper voltage increases from 0.5V to 0.8V, evaluation delay increases but power consumption reduces upto the critical point (VDD1=.73V) and after that it starts increases.

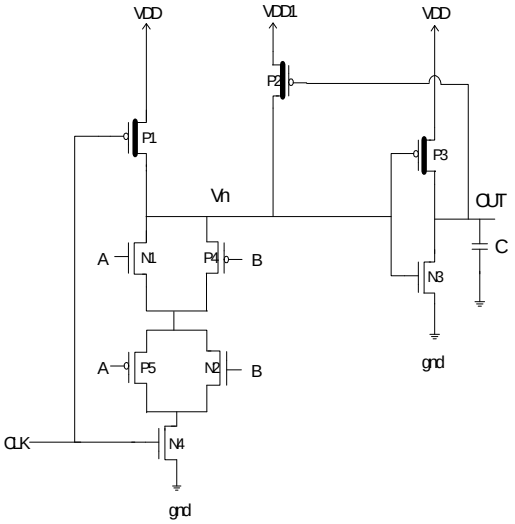

Fig 7. MTV Domino XNOR gate with dual power supply.

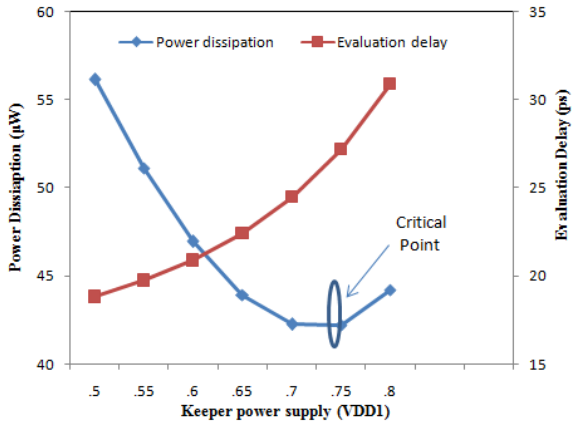

Fig 8. Evaluation delay and power dissipation of HVT domino XNOR gate with dual power supply.

If we apply some voltage at the source of footer transistor, the dynamic node will not discharge upto zero and the speed will increase. Based on this idea, we have applied a voltage of 0.13V at the source of footer transistor. Other advantage of applying voltage at source of footer transistor is that subthreshold leakage currents will reduce

hence power dissipation reduces and noise immunity increases. Hence the circuit proposed in Fig.9 has the ability to improve the overall performance of domino XNOR gate.

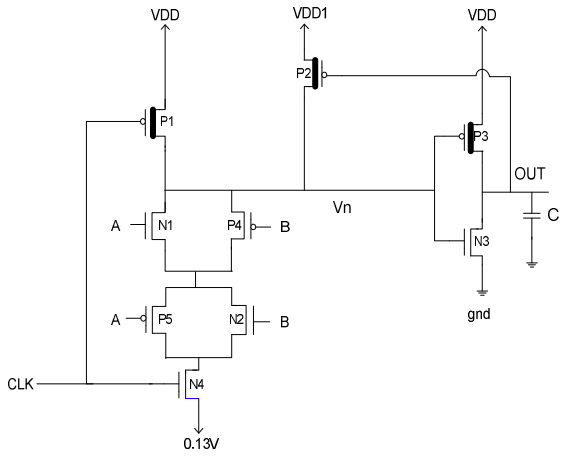

Fig 9. MPMT domino XNOR gate.

5 Simulation Results

We have simulated standard n-type XNOR and proposed XNOR circuit using 45nm CMOS technology. HSPICE [16] is used for calculation of performance parameter of the circuits. Table 2 shows the threshold voltages of different nMOS and pMOS transistors. The clock operating frequency is 1GHz. Performance parameters of proposed circuits are compared with standard n-type domino XNOR gate. We have used10fF capacitance load for all circuits, performance parameters are estimated at 25°C and at 110°C.

5.1 Performance parameters at 25°C

Different performance parameters such as leakage currents, evaluation delay, dynamic power consumption and A.C noise margin are measured at 25°C. Table 3 shows the leakage current of standard n-type XNOR and our proposed XNOR circuits for different input and clock combination. We can observe from table that our proposed circuits have lesser leakage current as compared to standard n-type XNOR gate. Our third technique MPMT XNOR gate has lowest leakage currents as compared to other techniques. From the table, it is clear that for input combination A=1, B=0, the leakage current is minimum.

Evaluation delay determines the speed of the domino circuits and it depends on the state of inputs. Table 4 shows the evaluation delay, power dissipation and PDP of standard n-type and our three proposed circuits .From the table, it is clear that MPMT XNOR gate has higher speed and lower PDP as compared to standard n-type XNOR. Dynamic power consumption of MPMT XNOR is reduced by 56%, in MTV XNOR it is reduced by 47%, and similarly in LTV XNOR, it is reduced by7% as compared to standard n-type XNOR gate as shown in Fig 10. A.C noise margin is defined as the level of noise signal for which output is reduced by 10% of its maximum value. We have calculated the A.C noise margin of standard and our proposed XNOR gate. For this we have applied a noise signal of frequency 1GHz with 60% duty cycle. MPMT XNOR has 58%, MTV XNOR has 50%, and LTV XNOR gate has 8% higher A.C noise margin as compared to standard n-type XNOR gate as shown in Fig 11.

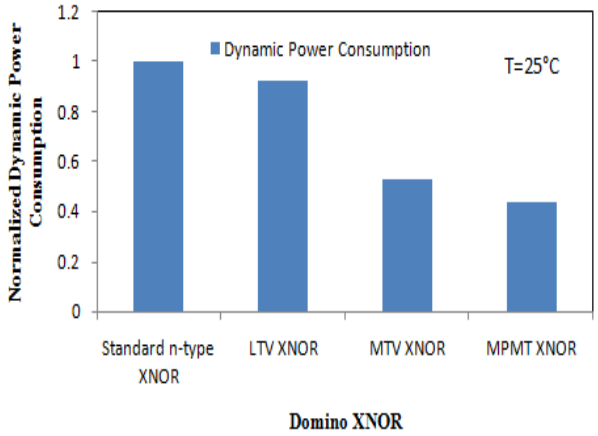

Fig10. Comparison of the dynamic power consumption with four techniques at 25°C.Dynamic power consumption is normalized by standard n-type XNOR for each circuit.

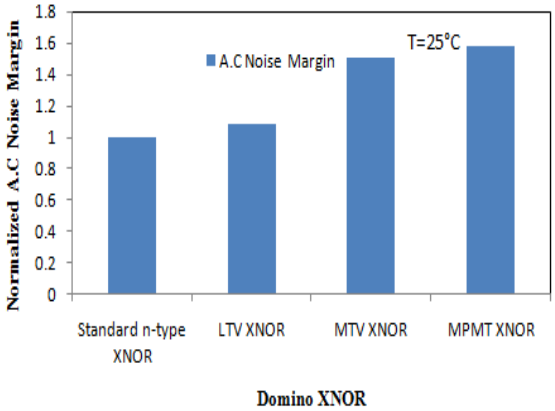

Fig 11. Comparison of the A.C noise margin with four techniques at 25°C. Dynamic power consumption is normalized by standard n-type XNOR for each circuit.

Table 2.
Threshold voltage of nMOS and pMOS transistors

Low Vt nMOS	Low Vt pMOS	High Vt nMOS	High Vt pMOS
0.22V	-0.22V	0.466V	-0.4118V

Table 3.
Leakage Current (μA) of standard n-type and three proposed XNOR Gates in Different Input States and Clock States at 25°C

	Standard n-type XNOR		LTV XNOR		MTV XNOR		MPMT XNOR	
(A,B)	CLK=0	CLK =1	CLK =0	CLK =1	CLK =0	CLK =1	CLK =0	CLK =1
(0,0)	1.44	2.79	1.74	2.32	1.47	1.69	1.0	1.61
(0,1)	1.79	3.02	0.785	1.92	0.51	1.52	0.27	1.12
(1,0)	1.79	3.02	0.54	1.70	0.28	1.48	0.24	1.02
(1,1)	1.44	2.53	0.96	2.25	0.69	1.80	0.36	1.75

Table 4.
Evaluation Delay, Power Dissipation and PDP of four XNOR Gates at 25°C

	Standard n-type XNOR	LVT XNOR	MTV XNOR	MPMT XNOR
Evaluation delay(ps)	83.6	85.6	30.9	29.0
Power dissipation(μW)	84.69	77.136	44.22	36.45
PDP (fJ)	7.08	6.6	1.36	1.1

5.2 Performance parameters at 110°C

All performance parameters (leakage currents, evaluation delay and dynamic power consumption) are measured at 110°C. Leakage currents of standard n-type and proposed circuits are listed in table 5. We can observe from the table that all proposed circuits have low leakage current as compared to standard n-type XNOR gate. From the table it is clear that for input combination A=B=0, the leakage current is minimum.

Table 6 shows the evaluation delay, power dissipation and power delay product of standard and our proposed three circuits. From the table, it is clear that MPMT XNOR gate has higher speed and lower PDP as compared to standard n-type XNOR and two proposed circuits. Dynamic power consumption of MPMT XNOR is reduced by63%, MTV XNOR by 60%, LTV XNOR by 9% as compared to standard n-type XNOR gate is shown in Fig 12.

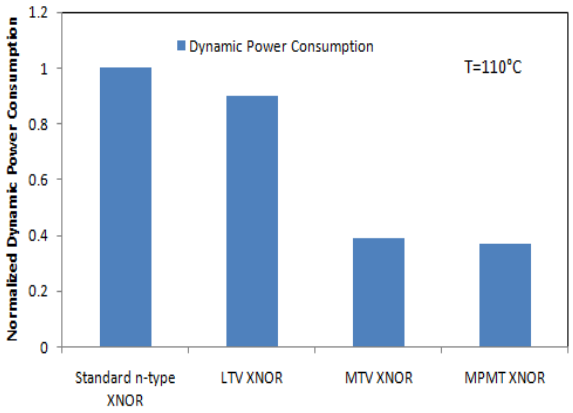

Fig 12. Comparison of the dynamic power consumption with four techniques at 110°C.Dynamic power consumption is normalized by standard n-type XNOR for each circuit.

Table 5.
Leakage Current (μA) of standard n-type and three proposed XNOR Gates in Different Input States and Clock States at 110°C

	Standard n-type XNOR		LTV XNOR		MTV XNOR		MPMG XNOR	
(A,B)	CLK=0	CLK=1	CLK=0	CLK=1	CLK=0	CLK=1	CLK=0	CLK=1
(0,0)	11.61	12.35	11.02	5.02	10.59	2.06	2.04	2.01
(0,1)	14.68	16.01	6.12	6.04	5.82	2.32	2.26	2.21
(1,0)	14.68	16.01	3.71	5.76	3.42	2.57	2.05	2.33
(1,1)	8.50	11.21	.96	11.15	9.40	2.47	2.29	2.09

Table 6.
Evaluation Delay,Power Dissipation and PDP of Four XNOR Gates at 110°C

	Standard n-type XNOR	LTV XNOR	MTV XNOR	MPMT XNOR
Evaluation delay(ps)	77.17	79.6	24.52	23
Power Dissipation (μW)	103.97	91.23	44.22	36.19
PDP (fJ)	8.02	7.26	1.08	.83

6 Conclusion

In this paper, three new domino XNOR circuits are proposed. We have compared the performance of our proposed circuits with standard n-type XNOR gate at 25°C and 110°C. It is found that our proposed circuits has lesser power consumption, lesser evaluation delay, lesser PDP and higher A.C noise margin as compared to standard n-type XNOR gate.

Our third proposed circuit (MPMT XNOR) has better performance as compared to standard n-type XNOR gate. Our simulation results show that proposed circuits have minimum leakage currents at 25°C when the input combination is A=1,B=0.Similarly at 110°C, proposed circuits have minimum leakage currents when input combination is A=0,B=0.

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